Reconfigurable three-terminal logic devices using phase-change materials

Submitted by Ammar Adel Hasan Al-shahrablee to the University of Exeter

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Abstract

Conventional solid-state and mass storage memories (such as SRAM, DRAM and the hard disk drive HDD) are facing many technological challenges to meet the ever-increasing demand for fast, low power and cheap data storage solutions. This is compounded by the current conventional computer architectures (such as the von Neumann architecture) with separate processing and storage functionalities and hence data transfer bottlenecks and increased silicon footprint. Beyond the von Neumann computer architecture, the combination of arithmetic-logic processing and (collocally) storage circuits provide a new and promising alternative for computer systems that overcome the many limitations of current technology. However, there are many technical challenges that face the implementation of universal blocks of both logic and memory functions using conventional silicon technology (transistor-transistor logic - TTL, and complementary metal oxide semiconductors - CMOS). Phase-change materials, such as $Ge_2Sb_2Te_5$ (GST), provide a potential complement or replacement to these technologies to provide both processing and, collocally, storage capability. Existing research in phase-change memory technologies focused on two-terminal non-volatile devices for different memory and logic applications due to their ability to achieve logic-resistive switching in nanosecond time scale, their scalability down to few nanometer-scale cells, and low power requirements. To perform logic functionality, current two-terminal phase-change logic devices need to be connected in series or parallel circuits, and require sequential inputs to perform the required logic function (such as NAND and NOR). In this research programme, three-terminal (3T) non-volatile phase-change memories are proposed and investigated as potential alternative logic cells with simultaneous inputs as reconfigurable, non-volatile logic devices.

A vertical 3T logic device structure is proposed in this work based on existing phase-change based memory cell architecture and original concept work by Ovshinsky. A comprehensive, multi-physics finite-element model of the vertical 3T device was constructed in Comsol Multiphysics. This model solves Laplace's equation for the electric potential due to the application of voltage sources. The calculated electric potential and fields provide the Joule heating source in the device, which is used to compute the temperature distribution through solution of the heat diffusion equation, which is necessary to activate the thermally-driven phase transition process. The physically realistic and computationally efficient nucleation-growth model was numerically implemented to model the phase change and resistance change in the $Ge_2Sb_2Te_5$ (GST) phase-change material in the device, which is combined with the finite-element model using the Matlab programming interface. The changes in electrical and thermal conductivities in the GST region are taken into account following the thermally activated phase transformations between the amorphous-crystalline states using effective medium theory.

To determine the appropriate voltage and temperature conditions for the SET and RESET operations, and to optimise the materials and thicknesses of the thermal and heating layers in the device, comprehensive steady-state parametric simulations were carried out using the finite-element multi-physics model. Simulations of transient cycles of writing (SET) and erasing (RESET) processes using appropriate voltage pulses were then carried out on the designed vertical 3T device to study the phase transformations for practical reconfigurable logic operations. The simulations indicated excellent resistance contrast between the logic 1 and 0 states, and successfully demonstrated the feasibility of programming the logic functions of NAND and NOR gates using this 3T configuration.

Appendices

Research Papers

(1) **A. Al-shahrablee**, M. M. Aziz and C. D. Wright, "Reconfigurable logic functionality of three-terminal vertical phase-change memory device", *manuscript in preparation.*

Attended Conferences

(1) **A. A Al-sharablee**, M. M. Aziz and C. D. Wright, "The effect of the temperature dependence of viscosity on modelling crystallization dynamics in phase-change materials", European Phase Change and Ovonics Symposium (EPCOS), Cambridge, UK. September 2016 (Poster presentation).

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List of Acronyms

Symbol	Designation
V	Electrical potential
σ	Electrical conductivity
∇	Denotes the gradient operator
Q	Heat source per unit volume
E	Electric field intensity
χ	Volume fraction of the crystalline material
σ_A	Electrical conductivity of amorphous phase
σ_C	Electrical conductivity of crystalline phase
q	Elementary charge
N_{T1} & N_{T2}	Trap concentration at different energy levels
E_C	mobility edge at the conduction
E_F	Fermi energy level
τ_0	Characteristic attempt-to-escape time for the trapped electron
T	Absolute temperature
Δz	inter trap distance between two traps
ρ	Material density
C_p	Specific heat capacity per unit mass
K_A	Thermal conductivity of amorphous phase
K_C	Thermal conductivity of crystalline phase
t	time
n	Avrami coefficient
K(T)	crystallisation rate constant depending on absolute temperature
$f(n,t)$	density of the clusters of size n
$g(n,t)$	Growth reaction rate
$d(n,t)$	Dissolution reaction rate
$f(1,t)$	Density of monomers at a given time

r	Cluster radius
λ	jump distance
γ^*	Molecular jump frequency at the interface between amorphous and crystalline phases
$\Delta G_{n\rightarrow n+1}$	Free energy differences between sizes *n* and *n+1*
ΔG	Bulk free energy difference per monomer
I_{hom}	Steady-state homogeneous nucleation rate
σ_{hom}	A pre-factor related to nucleation mode
E_{an}	activation energy related to nucleation mode
ΔG_{clust}	Excess free energy barrier to form stable homogenous nuclei
γ	Amorphous-crystalline interfacial energy and
Δg	Gibbs free energy difference between crystalline and amorphous phase
v_m	Volume of a phase-change material monomer
ΔH_f	Enthalpy difference of fusion at the melting point
θ	wetting angle
$f(\theta)$	Volume function as a function of the wetting angle
I_{het}	steady state nucleation rate for heterogeneous nucleation
V_g	crystal growth rate
v_0	Pre-factor related to the growth mode
E_{ag}	Activation energy related to the growth mode
PI_n	Probability of either homogeneous or heterogeneous
PV_g	Probability of growth via the growth process
Δ	Average/maximum tile length of the triangular tile
PI_n	Probability of nucleation
PV_g	Growth probability
Pc	Temperature dependent crystallization probability

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CHAPTER 1: Introduction and Motivation

Digital data, obtained from the digitization of various forms of information such as text, image or voice, and sound, plays a vital role in different aspects of our daily lives including business, education, entertainment and communication. All this data is used extensively in innovative products including social networks, smartphones and digital photo cameras. In the last few decades with the significant increase in digital data created, as shown in Table 1.1, the current hardware and software technologies started to lag behind the demand for faster, more powerful and, most importantly, cheaper storage and processing solutions. All these technologies require a vast amount of digital memory that needs to be continuously accessed for storing, retrieving and processing of digital data.

The very essence of a computer system architecture is the ability to perform any appropriate digital task to modify stored data without needing to redefine its location once a new operation is required. This ability is not just restricted to desktop PCs, most of modern embedded digital systems (like an mp3 player or an eBook reader for example) are programmable to include comfortable extended digital memory [5]. Storing digital data is thus a part of the operation of computer systems. In the semiconductor memory industry and academic research studies, there is a constant drive to develop faster, higher efficiency yet smaller memory devices for the increasing number of digital applications. Table 1.1 demonstrates the significant rise and corresponding demand for data storage and processing of data.

Table 1.1 Facts and figures of digital data created in 2012. (Reprinted from [5]).

Fact	From
300 times	The increment in the "Digital Universe" between 2005 and 2020.
40%	The increment in spending on IT infrastructure between 2012 and 2020.
24	Hours of videos uploaded every minute on Youtube
$4 \cdot 10^9$	Number of videos watched every day on Youtube.
18'000'000	Number of songs stored on ITunes servers.
450'000	Number of Google servers around the world.
700	Billion $, total capital of the 5 industrial leaders in data storage

1.1 Overview of Digital Memory Devices and Technologies

There are three main data storage technologies available in the market: optical storage, magnetic storage and solid-state memories [6]. Each technology has their own limits along with some differences in performance. So far, practically, no global storage medium exists, and all methods of storage have certain distinct characteristics. Hence, a computer system usually encompasses several kinds of storage technologies, and every one of them has its own functionality and performance. The current dominant storage technology is solid state memories on printed circuit board. These are distinguished from the traditional electro-mechanical memories such as magnetic (hard disk drive HDD) or optical memory, which contain spinning discs and movable write/read heads [7]. Solid-state memories, on the other hand, have compact size, high-speed, and are mostly used as the primary memories, while optical storage and magnetic systems are naturally used as the secondary drive in computer systems

1.2 Solid-State Memory Technologies

Solid-state memories can be categorized into volatile memory (VM) that needs power for storage, and non-volatile memory (NVM), which retain their data even during power off and the main focus of this thesis. Figure 1.1 shows the hierarchical solid-state memory systems (memory taxonomy), which are classified according to the performance-cost trade-off between low-cost data storage, high density, low power consumption and good size scalability. The static random-access memory (SRAM) and dynamic random-access memory (DRAM) are usual examples of the volatile memories, whereas flash memories (either NOR or NAND technologies) can be categorized as non-volatile memories. These types are technologically recognized as traditional memories [7] and [8]. However, ferroelectric random-access-memory (FeRAM), phase change memory (PCM), magnetic RAM (MRAM), and spin-transfer-torque RAM (STTRAM) are covered under the prototypical category for non-volatile memories and can be classified as emerging memory technologies.

The speed difference, between memory and logic processing requirements, has led to impose a certain architectural limitation related to system performance. In the general provision of von Neumann computer architecture, temporary or long-lasting data storage is important to be present in any computation processing and even in logic functions related to information processing system. So far, this provision has been achieved by spatially separating data processing units from memory devices. However, there are fundamental limits on scaling down the silicon layer in these memories and intensive energy consumption due to moving the data between two different locations. Consequently, an overview of the main solid-state memories, such as Flash, DRAM and SRAM), is provided next to highlight the fundamental limitations in conventional computer architectures.

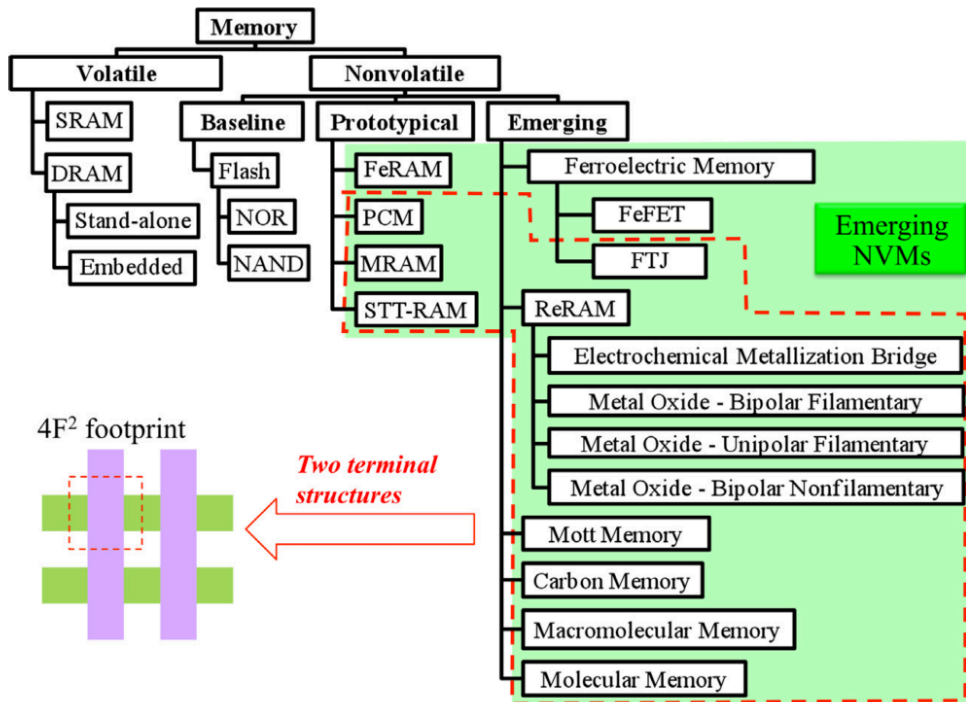


Figure 1.1 Hierarchical memory systems of both volatile and nonvolatile classifications, (reprinted from [9]).

1.3 Traditional Solid-State Memories

1.3.1 Static Random-Access Memory (SRAM)

Over several decades, the non-volatile magnetic core memory was swapped by the integrated static Random Access Memory (SRAM) with much higher density [6]. The word ‘static’ indicates that the data in the memory cell is held statically as long as its power is being supplied. It does not need to be refreshed or updated when its provided power is still on, as in the case of Dynamic Random-Access Memory (DRAM) that will be discussed in next section. Furthermore, the ‘random’ feature is available here, which means individual bits in the memory can be accessed rather than being processed sequentially. Thus, this feature provides faster access to data than the DRAM.

Typically, SRAM chips use a matrix of six transistors and no capacitors for each cell [5]. Each memory bit is usually stored in four transistors, and two additional transistors are used for accessing the storage cell during write and read operation, as shown in Figure 1.2(a). The matrix of transistors is embedded into an $84F^2$ single cell size with F being the smallest feature possible with a chosen lithographic technology. At present, SRAMs continue to be embedded in the central processor unit (CPU) in computers to support processing as high-performance level 1 (L1) and Level (L2) cache memories [7]. Because of the cell size, it is currently not clear if scaling beyond 16 nm node will be possible at all, which depends entirely on how far conventional photolithography can be boosted to develop this volatile memory technology.

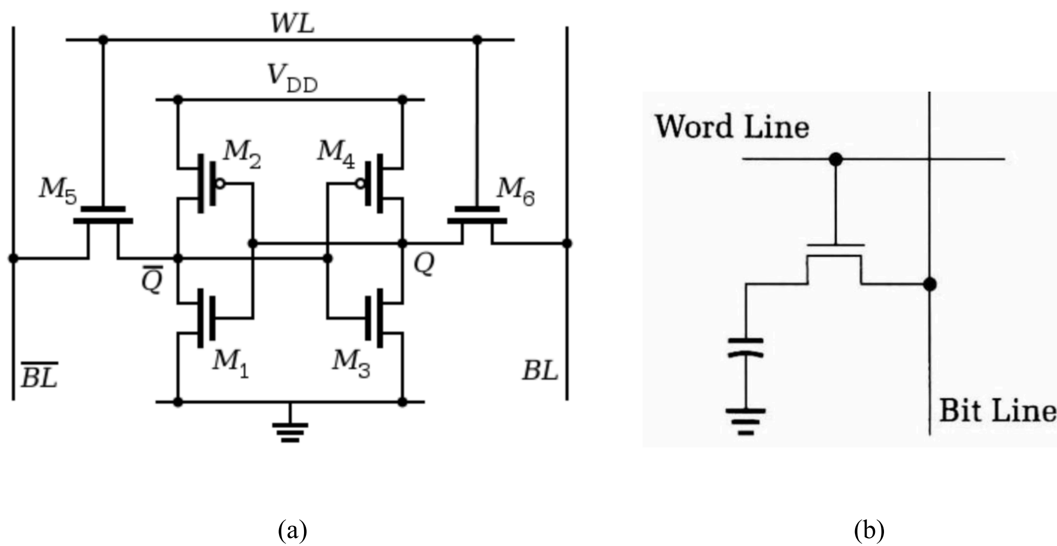


Figure 1.2 Schematic circuit diagrams of (a) A conventional 6T SRAM cell, and (b) DRAM cell. (Both are reprinted from [5]).

1.3.2 Dynamic Random-Access Memory (DRAM)

The second level of the traditional memory pyramid is dominated by Dynamic Random Access Memory (DRAM). The principle of storing each data bit in the DRAM relies on a capacitor embedded within the memory cell that is constantly charging and discharging to store logical ‘1’ and ‘0’ states. Because of current leakage, the capacitor must be periodically

refreshed by an external source, i.e. storage cell is refreshed dynamically every few milliseconds while the provided power is still on. Thus, the term "dynamic" is added to the memory cell to reveal the particular manner of this memory, in contrast with the SRAMs that do not need to be refreshed. However, the DRAM is also volatile, and data is not held when the power supply is interrupted or switched off.

DRAM cells consist of one capacitor and one transistor, as shown in Figure 1.2(b). The principle of DRAM memory operation relies on the storage of charge inside an integrated capacitor which can be accessed mainly by a single transistor, i.e. the transistor acts as a switch which enables the control circuitry on the memory chip to read the capacitor or change its state. With a single transistor being used for data storage in DRAM, the cell size of DRAMs is constantly reducing over time down to $6F^2$ or even $4F^2$, compared to the SRAM cell that requires 6 transistors. This reveals the simplicity of cell size fabrication. However, periodically refreshing to recharge the capacitor in DRAM leads to more power consumption and slower processing speeds than those in the SRAMs. Furthermore, it is also not clear whether future scaling of DRAM cells will be possible down beyond the 16nm node [5].

1.3.3 Flash Memory

Flash memory is a (solid-state) non-volatile memory that is based on standard semiconductor CMOS technology and first developed in the early 1980s. A Flash memory cell consists of a storage MOSFET transistor along with a control gate and a floating gate. Information storage relies on the charging/discharging of the floating gate through a process of transferring charge (electrons) to overcome a barrier either by application of a high electric field or hot electron injection that gains sufficient kinetic energy to break an interface state in

a dielectric surrounding the floating gate. Thus, the stored information can be kept at detectable levels for up to 10 years in the floating gate.

Typically, regarding the logic functionality, there are two existing types of Flash technologies: NOR and NAND technology. NAND Flash technology tends to be widely used and dominant type in different digital electronic devices, such as digital still camera (DSC), universal serial bus (USB) and memory cards, due to its benefits of better scaling potential for high cell densities compared with the NOR Flash technology. Whereas, NOR Flash has a lower cell capacity, but easy access and fast read speeds compared with the NAND Flash, so it is often used for code storage [7][10]. Consequently, Flash memories can have many compact forms with high capacity, however the significant current concerns of both Flash memory types are scaling limitations. It is still not clear if Flash memory scaling will be possible beyond the 16 nm node technologies [7]. That is related to future scalability to find a new more scalable memory solution with the same advantages of Flash memory, and may allow the use of binary or non-binary computations during data storage.

1.4 Emerging Solid-State Memories

Emerging non-volatile memory (NVM) technologies have been proposed to complement or even replace conventional NAND and NOR Flash memories. Novel mechanisms and materials are often involved within the NVMs that are different from those of traditional memories based on CMOS [8]. These materials, such as transitional metal oxides, ferromagnetic metals and dielectrics, carbon materials and chalcogenides, have switching mechanisms that extend beyond classical electronic processes of the traditional memory technologies. Some of these non-volatile memories include magnetic RAM (MRAM) [11] [12], spin-transfer torque RAM [13] [14], ferroelectric RAM [15] [16], phase-change RAM (PCRAM)[17]–[19], and resistive RAM (RRAM) [20]–[22]. These alternatives or emerging

memories are being investigated in detail to overcome or compensate the limitations of Flash memory technology. The following discussion demonstrates and compares some desired characteristics of the promising NVM technologies in use today.

1.4.1 (FeRAM) Ferroelectric RAM

Ferroelectric memory (FeRAM) is a type of NVM with a similar conceptual circuit to DRAM, i.e. a single transistor and a single capacitor, but it also uses the ferroelectric layer in the cell capacitor instead of the dielectric layer for storing data in charge forms [7]. Figure 1.3(a) illustrates the main cell structure of a single FeRAM. The stored charges in the ferroelectric capacitor form a dipole in the ferroelectric material under application of an external electric field. Here, the capacitor is charged or discharged according to the polarization state of the ferroelectric material that can be used to store the logic bits 1 and 0 in terms of the positive and negative polarizations respectively. The changes in the ferroelectric polarization states can cause shifts in the locations of the atoms within the original crystal structure and then change in the electronic charge distribution. A read operation is performed then, depending on the charge polarization forms of the ferroelectric material, by applying a current spike on the output terminal that allows the prior polarization to be determined as binary state 1 or 0.

FeRAMs have advantages over DRAM and Flash, such as lower power consumption, which is the most attractive feature of FeRAM compared with the other types of NVMs. The FeRAM memoirs require neither a refresh process nor the transfer of the charges (electrons) across a high-energy barrier, as in the case of DRAM or Flash memory respectively. Thus, FeRAM is influenced by a voltage application of less than 2V during the writing process, in contrast to NAND Flash that requires erasing/writing voltages of approximately 20V [23]. Due

to this advantage, the FeRAM has realized a write speed of a few nanoseconds compared to a few milliseconds in Flash memory.

However, the scalability of the FeRAM cells are restricted to further technology nodes. This is mainly due to the issue of using very thin ferroelectric layer which decreases the charge accumulated in the FeRAM capacitor and affects the storage and switching functions of the device and its endurance [7]. These factors have contributed to the relatively slow development in FeRAM storage density compared with that of Flash memory. Currently, the maximum capacity of FeRAM at the laboratory level and industry are 128 Mb and 4 Mb respectively [24] and [25].

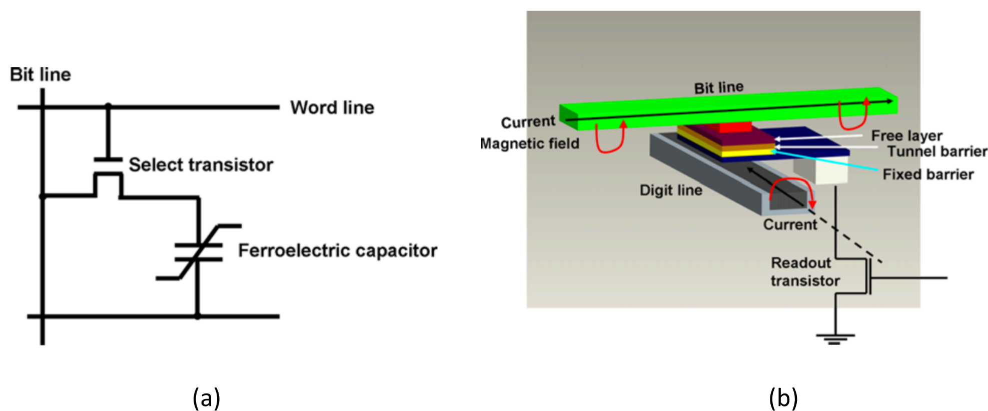


Figure 1.3 (a) Cell structure of FeRAM, and (b) Cell structure of MRAM. (Reprinted from [5]).

1.4.2 Magnetic RAM (MRAM) and Spin-Transfer Torque MRAM (STT-MRAM)

Magnetic RAM is another type of non-volatile memory that has been under development over the last three decades. MRAM uses magnetic charge in a ferromagnetic material to store data instead of electric charge used in DRAM and SRAM technologies. MRAMs include a magnetic-tunnel junction (MTJ) that is made from a thin insulating layer sandwiched by 2 ferromagnetic layers, as shown in Figure 1.3(b). The data storage in the MRAM is achieved by

applying an external magnetic field resulting in changing its resistive state between a high resistance (OFF state or logical 0) state and a low resistance state (ON state or logical 1), depending on the parallel or anti-parallel alignment of the fixed and free layers, which gives the high and low resistance states.

The use of ferromagnetic elements as memory cells in MRAM provides the advantages of non-volatility, higher operational speeds (< 20 ns) and a greater endurance (10^{12} - 10^{16} cycles) [5][19]–[22]. Nevertheless, like FeRAM technology, further scaling down is a serious limitation that prevents to create a large-scale integrated memory of MRAM in the semiconductor storage market. Besides, an inverse relationship between the switching field and the cell size indicated that an additional scaling down of the MRAM elements requires a larger magnetic field [30], i.e. an additional portion of power consumption and potential unreliable integration arising from electron-migration phenomenon in metal lines when a short distance is available between two adjacent MRAM cells.

Based on the above considerations, recent advances in microelectronics and optoelectronics have been given for creating resistive switching devices based on magnetic materials, such as spin-torque transfer (STT) MRAM which uses conduction spin currents for switching without the need for an external magnetic field. That can make them suitable for integration with CMOS in high performance logic chips instead of using the conventional memories, such as SRAM or DRAM [31]. The STT-MRAM structure is demonstrated in Figure 1.4 [32]. A fixed and a free layer are arranged in the same direction to give a low resistance state. Whereas, an opposed spin arrangement between these two layers can cause high resistance state. Switching between these states is achieved through passing a current through the MTJ.

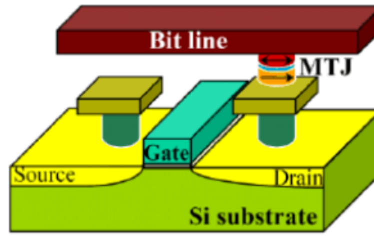


Figure 1.4 STT-MRAM cell Schematic. (Reprinted from[32]).

With a cell technology at 65 and 45 nm nodes, the STT-MRAM production can be a potential replacement for existing memory technologies [7]. Furthermore, the STT-MRAM has high endurance (around10^{12}- 10^{15} predicted), with write/read switching energies in the range of 3 pJ and switching speeds better than 10 ns [33]. Nevertheless, one of the key limitations is the short data retention when the cell size is scaling in a range of 20 nm at temperatures higher than 85°C [34]. The major challenge in the STT-MRAM cell technology that is difficult to continue downscaling the contact-access of the MTJ with the overall cell size, to be similar to the ReRAM cell size, and hence further scaling down is a serious limitation influenced by the size of the MTJ.

1.4.3 Resistive Memory Devices

An alternative to non-volatile magnetic memory devices is the resistive memory device, such as resistive random-access memory RRAM and phase-change memory PCM that is usually referred to as phase change random access memory (PCRAM). These two resistive type memory devices are based on resistance switching mechanisms to store data via the switching between two distinct resistances (a high and low resistances) under electrical voltage applications. In other words, a dynamic resistance value based resistive switching behaviour determines the memory state of the device.

1.4.3.1 Resistive Random-Access Memory (RRAM)

In the conventional RRAM device, a typical cell contains a resistive layer sandwiched between two metal oxide electrodes, such as NiOx, TiOx, and TaOx as shown in Figure 1.5(a), to form metal-insulator switching cell. The switching of the cell resistance is achieved by applying controlled current or voltage pulses between these electrodes. Typically, a conductive switching channel of certain oxygen anions is formed in a section of the insulated area under application of positive pulses. The application of negative current or voltage pulses reverses the switching process where the oxygen anions return to their original positions making the switching channel an insulator again [32]. Recent studies indicated that oxide layer-based RRAMs are favourable competitors in the NVM market through achieving ultra-high switching speeds with good stability when the cells are downscaled to less than 20 nm. However, this type of resistive memories used oxide layer that makes the RRAM as an emerging technology needed more research for the device fabrication challenges to control the reversible switching characteristic inside the resistive material.

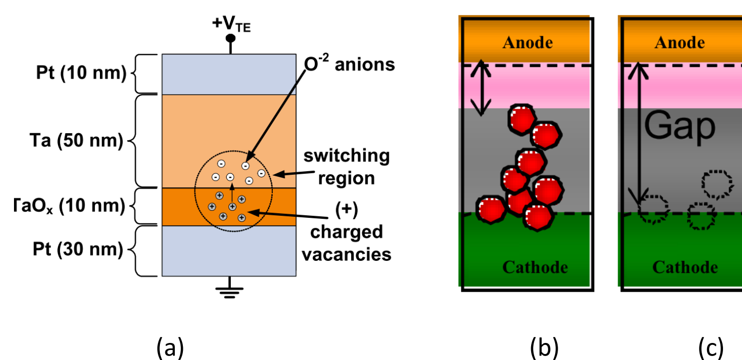


Figure 1.5 (a) ReRAM cell Schematic with the cell performance when subject to a positive bias on the top electrode, (b) Schematic of ECM or CB-RAM cell subjected to a positive and negative biases respectively .((a) and (b) reprinted from[32] and [132] respectively).

Another type of the physical switching process also used in resistive RAMs is known as an electrochemical change mechanism (ECM) or Conducting Bridge RAM (CB-RAM) [7]. This

type of resistive memory involves the use of phase-change materials, such as chalcogenides: GeSe and Cu_2S [35]–[37], for resistance switching. The resistance switching behaviour of ECM involves forming and destroying a conductive bridge of conductive filaments in the switching layer, as shown in Figure 1.5(b). The electrochemical process is induced by adding or removing metal atoms from the surface of a metallic electrode. In other words, one or more filaments can be formed over the cathode when a positive voltage pulse is applied to the anode. Eventually, the metallic filaments grow faster to create the conductive bridge through experiencing higher electric field. Nevertheless, CB-RAM technology suffers some drawbacks in the form of a trade-off between stability and programming power. This places a main concern about the leakage current effects on forming conductive filaments that can produce a low on/off resistance ratio.

1.4.3.2 Graphene Resistive Random Memory (GRRM)

Graphene resistive random memory (GRRM) is a new promising field of resistive memory research that has strong potential for advanced functionality and cost-effectiveness to develop alternative nonvolatile logic devices compared with conventional RRAM [38][39]. GRRAMs can be divided into three main types: graphene-inserted electrode RRAM (G-RRAM), gate-controlled graphene-electrode RRAM (GC-GRRAM) and the laser-scribed technology (LSG-RRAM) [38].

The G-RRAM device sample consists of a single layer of graphene material integrated into a basic structure of metal oxide RRAM, as shown in Figure 1.6(a). A reduction in the RESET current and programming power consumption of around 22 times and 47 times respectively was observed by inserting a thin graphene layer at the electrode/oxide interface compared with other RRAM devices without the graphene material. Beside this, a reasonable resistance switching performance for producing a 2-bit storage capability was realized by using another

GRRAM device, which is named LSG-GRRAM as shown in Figure 1.6(b). In this case, laser scribing technology is used for heating and formation of cation conductive filaments, which leads to changes in the device resistance. A third device structure of the GRRAMs, which is the GC-GRRAM, is used to realize gate-tunable RRAM devices by placing a single-crystal of bilayer graphene (BLG) layer grown under a chemical vapour deposition (CVD) on to the Si/SiO_2 substrate, as shown in Figure 1.6(c). These three graphene-based RRAM devices show the potential of graphene material, beyond the silicon age, to change the whole landscape of combining data processing and memory storage integrated into a single device. However, the device fabrication challenges to control the reversible switching characteristic inside the graphene material itself, need further efforts to be done in this research direction.

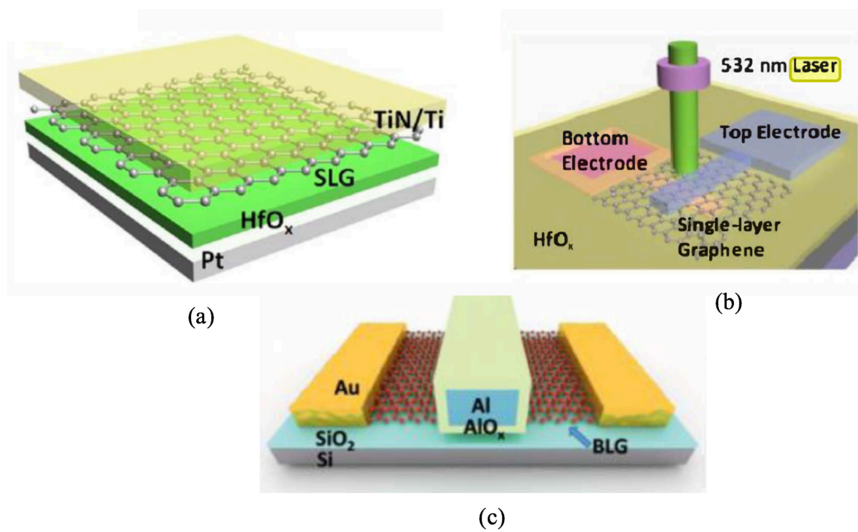


Figure 1.6 The structure device of (a) the G-RRAM (b LSG-RRAM, and (c) The GC-GRRAM (reprinted from [38]).

1.4.3.3 Phase Change Random Access Memory (PCRAM)

PCRAM has been actively researched over the last 10 years and recognised as the most promising memory technology for the next generation of nonvolatile solid-state memory systems. Their most attractive features are excellent scalability, low power consumption, long retention time and fast random read/write access speeds [40]. These features also enable the use of PCRAM devices as logic elements compatible with CMOS technology [41]. Thus, many significant advances in PCRAM performance have been made recently by leading companies (such as Intel, Samsung, IBM, Micron etc.) that can be summarized and compared with other solid-state memories Table 1.2 [42]

The first practical demonstration of phase change memory was reported by Intel in 2001 when an Ovonic amorphous semiconductor switching device integrated in series with a silicon p-n junction diode [43]. After that, two PCRAM devices have been manufactured by Samsung [2] and Micron [44] to demonstrate the high scalability where the PCRAM cell size was scaled down to 20 nm technology node. Adopting PCRAM as a main memory having logic functionality needs to overcome its write issues, such as long write latency and high write power [45].

The ability to perform multiple resistive switching by using different resistance forms of phase-change memory does not only provide the opportunity for memory storage but also enables the possibility for more advanced functions and applications of phase-change materials, that goes beyond the PCMs as memory cells. Some of these functions are briefly presented in the following subsections to reflect the ability of phase-change materials to perform both logic and memory functions as building units for future extensive parallel computing beyond von Neumann architecture.

Table 1.2 Comparison of Performances between PCRAM and other memory devices. (Reprinted from[42]).

	SRAM	DRAM	FeRAM	STT-MRAM	RRAM	PCRAM
Cell size (F^2)	140	6	22	20	8	4
Cell type	6T/ 4T	1T1C	1T1C	1(2)T1R	1T1R	1T(D)1R
Volatility	V	V	NV	NV	NV	NV
Write/ Erase time (ns)	0.2	<10	65	35	10	10/100
Data retention time	Long	64ms	10yrs	>10yrs	>1yrs	>10yrs
CMOS logic compatibility	Good	Bad	Ok, but High V need	Ok	Ok	Good

1.5 PCM Beyond Von-Neumann Computing Architecture

In 1945, the basis of modern computer architecture, such as the concept of using either mechanical or electrical relay components in the core architectures according to the John Von Neumann provision was reported by the Electronic Discrete Variable Automatic Computer (EDVAC) [5]. In this architecture, data processing is spatially separated from memory storage. This introduces a high energy consumption (i.e. transferring information from one location to another) as well as being time-consuming, which is one of the key concerns in CMOS logic circuits. This led to researchers investigating the potential of having data processing (binary or non-binary) and memory storage integrated into a single chip, which would reduce both chip footprint and interconnect delay (i.e. savings in energy and computing time). This is not possible to achieve with the limitations of the von Neumann computer architecture (in Silicon-based devices). However, this is possible with PCM cells by using the non-volatile feature of the chalcogenide phase-change material to accumulate and store information as structural phase changes in the material.

One of the key advances in PCM technologies is the use of phase-change material itself. The pronounced optical or even electrical contrast between the amorphous and crystalline states of the material provides an ideal mechanism for reading information in resistance forms. The best phase-change compositions for commercial products in terms of speed and stability are ternary Ge-Sb-Te and quaternary Ag-In-Sb-Te alloys [1], [46], [47]. The most frequently used alloy is metastable rock salt (glass-like structure) which contains one or more elements from Group VIA of the periodic table, in particular Tellurium (Te). $Ge_2Sb_2Te_5$, which is simply referred to (GST or GST-225), is used extensively for both optical and electrical phase-change memories and devices and therefore used in all the modelling and simulation work in this thesis.

Usually, the phase transitions are realised by either a laser or electrical pulse to act as a heat source to induce the required temperatures for crystallization and amorphization [48]. The readout signal is the difference in the electrical resistance between the crystalline (low resistance) and amorphous phases (high resistance). Typically, the amorphous state is obtained from an initial crystalline phase by applying high electrical power, short-duration pulse to heat the crystalline material up to its melting temperature (T_m), followed by rapid cooling and quenching of the material into its disordered (amorphous) state, as shown in Figure 1.7(b). The crystalline state on the other hand is obtained by applying a lower amplitude pulse for a sufficient time to raise the temperature in the amorphous material to temperatures above crystallization temperature (T_x), and below its melting temperature (T_m) to crystallize the material. Figure 1.7(c) shows a typical current-voltage (I-V) characteristics of the Reset and Set states of a PCM cell. At the point of the threshold voltage V_T, the output resistance is suddenly switched from the high to the low state as the material transforms from the amorphous to the crystalline phase. Here, the threshold switching point, which is determined by the material properties and the crystallization kinetics of the phase-change materials, plays a

pivotal role in determining phase-transition concepts, and then allows a high current flow in the amorphous state without applying large writing voltages. Consequently, this concept of the phase-transition is used in this study to perform different logic functions based on producing multiple resistance states.

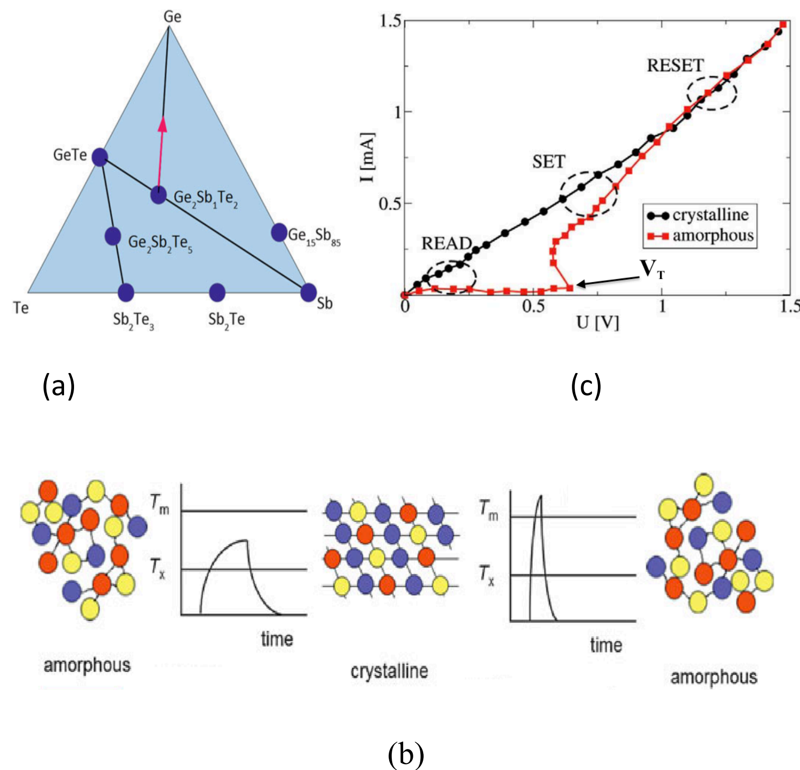


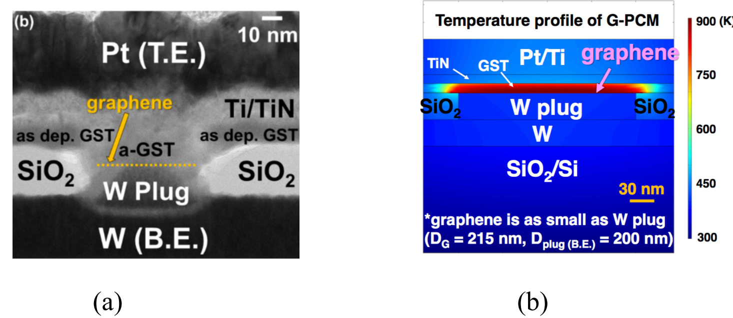
Figure 1.7 (a) The Tertiary Ge-Sb-Te phase-change diagram with some highlighted alloys, the red arrow indicates the trend of adding Ge to $Ge_2Sb_1Te_2$ alloys. (b) Principle of phase transitions: amorphous-crystalline and crystalline-amorphous. (c) current-voltage (I-V) curve of the Reset and Set states of a PCM cell. ((a) and (b) reprinted from [133], (c) reprinted from [134]).

1.6 Graphene-PCM (G-PCM) Device Technologies

The phase-transition between the crystalline and amorphous states in the chalcogenide phase-change materials have been briefly discussed in the preceding section. This section considers the possibility of emerging PCM device structure with a nanoscale volume of the chalcogenide materials, that faces a critical challenge to develop feasible device structures with a reduction in the switching volume. A nanoscale switching volume of the phase change material can physically decrease the current flow being used for switching between amorphous

and crystalline phases, and then switching speeds increase. However, due to present lithographic technology and material restrictions, there are fundamental limits on how possible downscale the PCM devices can be made with effective functionality. Recently, various emerging device structures have been proposed in the literature, such as graphene-based PCM (G-PCM) cells, to overcome these limits and help to confine the generated heat inside the active PCM volume.

The use of graphene layer with the phase-change materials has been found to be a promising candidate for improving the energy efficiency of certain PCM devices [49][50]. A thin interfacial thermal layer of graphene between the phase-change material and a bottom electrode (Tungsten), as shown in Figure 1.8, could result in less atomic migration and decreasing heat loss escaping through the bottom electrode. Ahn et al. [49] discussed that the PCM devices with a thin layer of graphene, as an effective thermal barrier, consume less programming current of ~ 40% compared with those devices without involving graphene layer. Graphene-inserted PCM devices achieved high programming endurance of up to 10^5 cycles and resistance distributions with on/off switching ratio up to ∼100. Nevertheless, the G-PCM devices depend on fabrication variability and reliability of the interfacial graphene layer with the phase-change materials. Thus, such devices must be particularly improved by providing further research on device structure optimization, and controlling the thermal efficiency of the interfacing layer between the phase-change materials with the substrate to increase thermal boundary resistance (TBR) and reduce heat loss from the devices.



(a) (b)

Figure 1.8 (a) A thin layer of thermal graphene barrier enables an energy-efficient PCM design. (b) The temperature profile of the G-PCM device, shows the hottest region when the graphene is patterned as small as the bottom electrode (Tungsten) heater (reprinted from [49]).

1.7 Memory Logic Operations Using Multilevel Resistance States

Another distinctive feature of PCM technology is the multi-level cell (MLC) functionality for increasing the PCM storage capacity [51]. By the implementation of multilevel PCM cell via a series of partially amorphous or crystalline states, multi-bit storage can be provided in a single bit cells. The capability of programming the phase-change material into multiple resistance levels also enables the use of PCM cells for realizing multi-bit logic operations. Thus, much more data can be stored with the same cell size through creating many intermediate crystalline or amorphous states.

There are two alternative approaches for programming multilevel storage PCM cells. The first approach is through creating a mushroom volume of amorphous region in a crystalline material, and then crystalline filaments are created and modulated through applying different amplitudes of SET pulses, as shown in Figure 1.9(b). Here, the formation of different volumes of crystalline filaments produces intermediate levels of resistance states for multi-level applications. In the second approach, the cell is partially programmed through creating amorphous regions of different sizes in an initially crystalline phase. The amorphous area is formed by applying RESET pulses of different amplitudes to melt and then quench different sizes of the amorphous regions, as shown in to achieve better controlFigure 1.9(a). The former is often used for producing intermediate resistance states for multi-bit logic functions, i.e. to

achieve better control over obtaining ultra-multiple-level storage (UMLS) based Multiplexers (Muxs) [41] [52]. More details of these two approaches will be discussed in the following chapters of this thesis as main bases for the choice of the initial state to program the three-terminal reconfigurable logic devices.

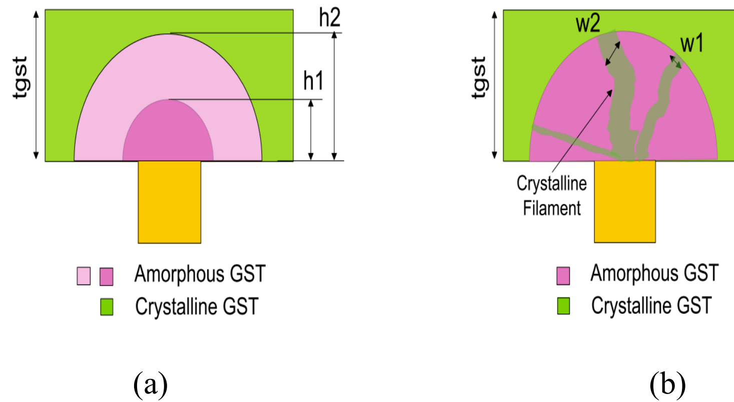


Figure 1.9 (a) Increasing amorphous region (thickness of the GST material t_{gst} , h1 corresponds to resistance R1, h2 corresponds to resistance R2 , h2>h1 => R2>R1). (b) Increasing crystalline filaments (w1 corresponds to resistance R1, w2 corresponds to resistance R2 , w2>w1 => R2<R1). (Both reprinted from [53]).

1.8 Research Aims and Objectives

Phase-change memories (PCMs) are one of the current most promising technology for future non-volatile logic devices. Different structures of a two-terminal logic device based on PCM technology were proposed and inspired by Ovshinsky et al. [54][55]. Then, a conceptual design of two-terminal logic devices was explored theoretically by Wright et al. [56][57], to suggest an approach for performing various arithmetic-logic computations, such as addition and subtraction , using the accumulating energy effects during the phase-transition processes. However, the logic states of the arithmetic computations were proposed to perform all in a sequential manner using the simple two-terminal PCM devices, such as the studies by Lacaita el.at. 2004 [58], and Redaelli el. at. [59]. A three-terminal (3T) phase-change logic device is an alternative approach to perform a reconfigurable logic functionality in a simultaneous manner using appropriate phase-change materials. Thus, the main focus of this research is to

investigate the feasibility, potential and performance of proposed three-terminal reconfigurable logic devices using phase-change materials. The logic functionality has been investigated and implemented using 3T device models to produce standard logic functions such as the NAND and NOR gates. A further physical insight into the nucleation and growth behaviour, to modelling the processes of crystallization and amorphization during the phase-change processes, is also provided by comparing the results with both previous studies by Senkader el. at. [2] and Blyuss el. at. [3]. Consequently, this study concerns characterizing crystallization dynamics of the GST materials in the 3T logic cell.

The variations of some physical parameters affecting the phase transformation, such as the cluster estimation in both nucleation and growth rates (i.e. temperatures and activation energy for both the nucleation and growth behaviour) and crystallite size distributions, are considered by comparing simulation results with experiments. Consequently, all these parameters are considered here to provide a real thermodynamical approach to realistically simulate the phase switching phenomenon in the 3T phase-change cell working as a reconfigurable logic cell.

The objectives of this research include:

- The design and optimization of a three-terminal PCM device structure having a capability of providing a reconfigurable logic functionality for performing universal logic functions (i.e. NAND and NOR logic gates), and multi-bit logic functions (i.e. multiplexers based ultra-multilevel storage).
- Carrying out extensive literature search and review of modelling crystallization in phase-change materials. This is necessary for the development of a physically realistic computation model for the simulations of the phase transformations (crystallization/amorphization) processes.

- Development of a multi-physics numerical simulation model that includes electrical, thermal and phase-change processes for the design and study of three-terminal, phase-change logic devices.
- Carrying out various steady-state parametric simulations to study and determine the optimum temperature-voltage characteristics for the writing and erasing simulation operations.
- Carrying out transient dynamic simulations of the erase and readout processes of the designed three-terminal logic devices and evaluate their performance logic functionality.

1.9 Thesis Outline

- In **chapter 1,** a review and comparison of various traditional and emerging memory technologies is provided is. The focus was on introducing phase-change memory as a promising technology for reconfigurable logic and for offering advanced storage and processing capabilities beyond the von-Neumann computer architecture.
- In **chapter 2,** details and reviews about the feasible current developments of the phase-change materials (as chalcogenide), in phase-change memories and in particular their application as logic devices, are presented for future perspective trends. The digital PCM applications realized through using various configurations of amorphous and crystalline regions within the material to place the memory cell or device into multiple resistance states. The volumes of both amorphous and crystalline states within the material with the main concepts of the cell or device geometry determined the electro-thermal interaction between the phase change material with the surrounding materials within the memory cell to insert the phase-

change logic devices geometrically into one of two main categories: contact-minimized and volume-minimized cells.

- **Chapter 3**, provides a detailed description of the numerical electro-thermal model implemented in Comsol Multiphysics and the governing physics. This chapter also presents an overview of phase-change models such as the JMAK model, rate equation method and classical nucleation theory and justification of the used of the nucleation and growth model in this research in modelling phase change materials.
- In **chapter 4**, the details of modelling multi-physics nucleation and growth approach in a realistic three-terminal PCM device design is presented. This modelling approach consists of the combination of three essential sub-models, i.e. an electrical model (based on the Laplace equation), thermal model (based on the heat-transfer equation), and phase change model (the nucleation and growth theory). Creating custom mesh and validation of crystallization model in a three-terminal PCM device for simulations is considered.
- In **chapter 5**, parametric simulations of the proposed 3T vertical device are carried out to determine the appropriate temperature-voltage characteristics and then resistance-voltage characteristics for transient simulations.
- **Chapter 6**, transient simulations of a vertical 3T PCM device model having a reconfigurable logic functionality are presented. The use of a single 3T PCM device to realize and perform essential logic gate functions, such as NAND and NOR gates, are discussed through controlling the logic relationship is between the output resistance states and effective input voltage applications, according to the truth table of each logic gates.
- In **chapter 7,** the main findings of this thesis are summarized, and outlines of possible directions for further research are discussed.

CHAPTER 2: Background and Review of Logic Functionality in Phase Change Memory Devices

It was identified in the previous chapter that current silicon-based memory and digital logic integrated circuits are experiencing significant challenges in scaling, power consumption and data rates. Regarding the explosive developing of electronics and computers for Complementary Metal-Oxide-Semiconductor (CMOS) integrated circuits, the formulation of Moore's Law in 1965 predicted that the number of components, such as transistors per chip, would increase approximately double every around two years [60], [61]. Thus, phase-change materials and devices offer the potential for small memory devices operating at low power and high speed, and shift in conventional computer architecture towards simultaneous data processing and storage within individual functional elements of phase-change devices. This chapter will review the current development lines in phase-change memories and particularly their application as logic devices, their important characteristics, and future perspective trends.

The main focus of this chapter is the review of the relevant literature on using PC memory as a reconfigurable logic element, starting with brief descriptions of fundamentals and construction of conventional digital logic circuits, and then the possible use of Phase Change memories for unified devices with the logic functionality and memory. Next, the nature of resistive switching in the phase-change memories for digital applications, such as threshold logic switching, and multiple resistance states will be discussed. Finally, logic functionality of traditional and emerging phase-change memories under different cell and device structures will be reviewed.

2.1 Digital System Basics

Digital systems are components or elements that deal with a set of two distinct signal states {0,1} [6]. Physically, these distinct states can represent voltages, currents, charge patterns, or other physical phenomena that can adequately be arranged into two unique states, called 0 and 1. A simple NOT gate or inverter implemented using CMOS transistors is shown in Figure 2.1. This CMOS inverter produces an output voltage V_{out} with either a logic 0 or logic 1 state when the input voltage V_{in} is at an appropriate level. V_{th} is the threshold voltage used to distinguish between two digital voltage states 0 and 1. More complex logic circuits can be constructed, in different logic networks, by combining a number of fundamental logic gates such as AND, OR, NOT ... etc. [62]. Thus, the same threshold switching approach for producing digital states can be used in phase change memory cells or devices based on phase-change materials for various logic memory applications, such as logic functions of NAND and NOR gates.

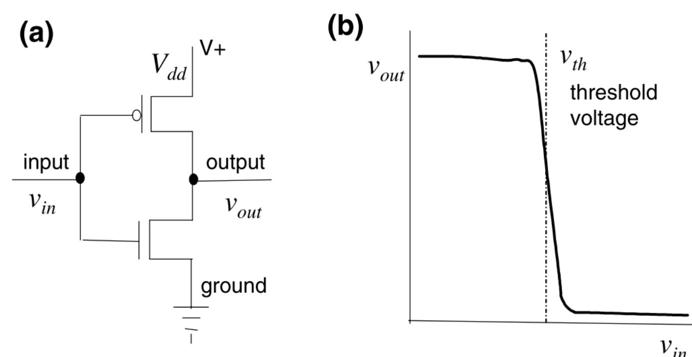


Figure 2.1 (a) Schematic of Complementary metal-oxide-semiconductor, (CMOS) inverter, and (b) Transfer characteristic. (Reprinted from [6]).

However, conventional combinational logic networks of silicon-based logic gates and circuits are volatile, and the stored information will be lost if the voltage supply is interrupted or turned off. In order to store the computed outputs of logic gates, conventional computer

systems use memory registers to hold these outputs for further processing. These registers consume a significant amount of power even without operation. Figure 2.2 [6] shows a generalized structure of a sequential logic circuit where the output of a combinational logic block is stored in a memory element (flip-flop) for processing. Here, the computed outputs (Y_c and Y_d) are a function of the combinational logic circuit with inputs ($X_a$and X_b), and an array of flip-flops (registers) is used to hold all output values. In this case, the output of this sequential logic circuit is dependent not only on the present inputs but the previous states of the output through the feedback in the circuit. The output states of the flip-flop array latch the outputs of the combinational Boolean circuit in synchronization with a clock, freezing both state and outputs between clock pulses. Consequently, more chip space occupation and multiple steps with longer operation time are needed to perform a complete logic function.

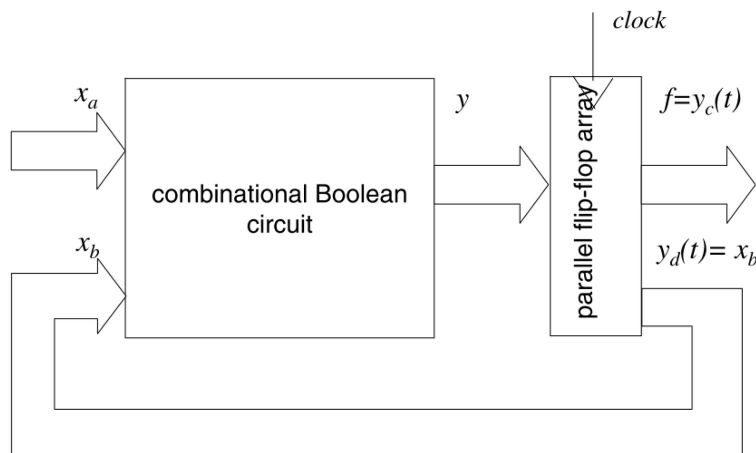


Figure 2.2 Generalized representation of clocked-mode sequential digital circuit (with single clock-domain). (Reprinted from [6]).

A potential alternative to the conventional refresh and volatile storage of sequential logic elements is a unified memory technology with Boolean functionality based on the reversible resistive switching of phase-change (PC) material between the amorphous and crystalline

phases. The electrical switching in the PC materials (such as chalcogenides) dates back to 1968 when S. Ovshinsky proved for the first time the reversible switching mechanism in the phase-change materials [63]. This switching process is non-volatile in behaviour, very fast and works even in small volumes, as discussed in the preceding chapter. Thus, by using these materials, a unified logic-memory technology can be developed to implement various primitive Boolean functions, such as NAND and NOR logic gates, without using further storage as registers, which is the focus of this research.

2.2 Threshold Logic Switching in PCM

The threshold logic switching in the conventional logic networks of silicon-based logic gates, is discussed in the preceding section through using a threshold voltage for distinguishing logic states 1 and 0. In phase-change materials, threshold logic switching is a general feature in the resistive switching behaviour of chalcogenide materials when the material conductivity changes from the amorphous (high resistivity) state to the conductive crystalline (low resistivity) phase. The most widely used chalcogenide material is $Ge_2Sb_2Te_5$ (denoted as GST). The GST alloy exhibits higher electrical stability and reversibility between the amorphous and crystalline phases for storing information in different digital forms [3][8][9]. The phase transition is thermally activated by applying optical or electrical pulses to cause Joule-heating that changes the structure of the material and hence its electrical and optical properties [67]. The resistivity of the crystalline GST phase is about three-order of magnitude lower than that for the amorphous phase [1][66][67].

The earlier concept of the GST phase transition between two different phases: the ordered (crystalline) and disordered (amorphous) structures, was discussed by Ovshinsky in 1968 [68]. Although many other studies disclosed the non-volatile ability of the phase-change memories to implement different memory operations such as read, write and store data, it is only since the late twentieth century that PCMs were considered and implemented to store and retain

digital information in resistive memory forms. This feature was considered when PCM applications were compared with conventional technologies like flash memory and DRAM [69]–[71]. In the last two decades, the ability of phase-change devices to switch electrically between the high and low resistance states, according to amorphous and crystalline phases respectively, is exploited to expand the functionalities of microelectronic systems through developing digital and non-digital functionalities in an integrated system based on the PCMs such as Compact Disk (CD), digital versatile disc-rewritable (DVD-RW and Rewritable Compact Disk (CD-RW) [65].

The transition from the amorphous to the crystalline phase in phase-change memories occurs through the application of a voltage across the devices. At a particular applied voltage, denoted as the threshold voltage, the transition from the high resistivity amorphous phase to the low resistivity crystalline phase occurs, as indicated by the current-voltage (I-V) curve shown in Fig. 4.2. This threshold voltage (V_T) thus can be used to define the boundary between the voltage ranges for reading, writing and erasing of the phase-change memory cells, as will be detailed later in chapter 6 of this thesis. Thus, understanding and modelling the threshold voltage is vital for controlling the voltage-logic characteristic in non-volatile PC memory cells. The threshold voltage is a function of the temperature, electric field and electron transport properties of the phase-change material. In chalcogenide materials including GST, threshold switching was attributed to an electrical instability due to charged carrier excitation at high electric fields, resulting in the movement from the equilibrium distribution to nonequilibrium distribution of carriers [72]–[75]. The conduction instability mechanism at a threshold switching point can be explained by the electrical injection effects at high-field energy-gain processes, as shown in Figure 2.3.

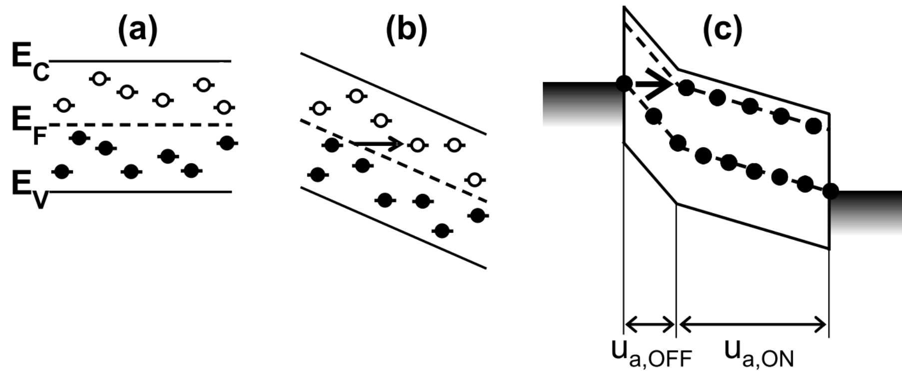


Figure 2.3 Threshold switching mechanism in the amorphous chalcogenide material shown charged carrier excitation under electric field effects (a) at high field, resulting in a non- equilibrium electron distribution, (b) Increase charged carrier mobility due to the presence of a dead space for electron energy gain, (c) Finite distance (OFF space $ua_{,OFF}$), resulting change in chalcogenide conductivity. (Reprinted from [76]).

As observed from Figure 2.3(a), an equilibrium distribution of electrons is controlled by Fermi level E_F, namely a Fermi-Dirac distribution, and maintained under a low voltage (low electric field). For higher electric fields, trapped electrons can gain a significant energy as a result of the electric field that can be modelled as a transition of electrons from low energy to high energy trap states, as shown in Figure 2.3(b) [6][76]. An increase of electron energy, which assumes to be adequate above V_T under the applied field, it would increase the electrical conductivity of chalcogenide-amorphous glass, denoted as 'OFF' layer, and thus reduce the voltage across the 'ON' layer, resulting in the rise in the snapback along the measured I-V curve, as shown in Figure 2.4 [6][76]. The resulting change in conductivity along the chalcogenide thickness leads to a non-uniform field to sustain the continuous mobility of electrons. The electric field has to be large in the low conductivity, OFF region denoted as u_a(OFF), where the energy distribution of electrons is close to equilibrium, whereas small in the high conductivity, ON region u_a(ON), where electrons have large average energy. The high and low electrical conductivities of the crystalline and amorphous phases in phase-change

material, which are corresponding to the logic states '1' and '0' respectively, reflect the ON and OFF switching states. The switching time of these switching states estimated to be in the range of nanoseconds, that represents ultimately the limit for higher switching speed in threshold switches based on the phase-change material principles [73]. Consequently, the electrical conductivity of the chalcogenide glass (amorphous region) in the threshold switching regime is dependent on electric field effects that will be discussed with more detail in the next theoretical chapter.

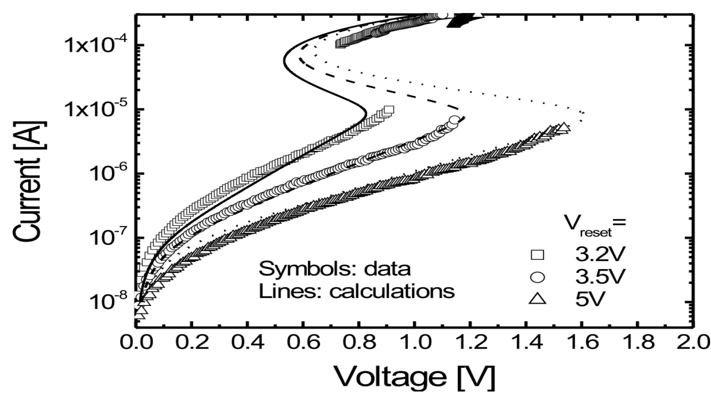


Figure 2.4 I-V curves for a PCM cell programmed at different thickness of the amorphous region in the cell and under various voltage applications. (Reprinted from [76]).

2.3 Programming Strategy in the Two-Terminal PCM Devices

Wright et. al. [51] exploited a typical structure, so-called vertical "mushroom-cell", for a two-terminal phase-change memory cell as shown in Figure 2.5. In the mushroom cell structure, the phase-change material is deposited on top of a TiN heater, which in turn is connected to a bottom metal electrode. Geometrically, the heater dimensions determine (along with the voltage/current applications) the size of the active region (switching volume) of the phase-change layer to switch between the amorphous and crystalline states. Thus, binary switching can be achieved in two-terminal PCM devices through reversible phase switching of the active volume, and hence resistance switching between amorphous and crystalline states.

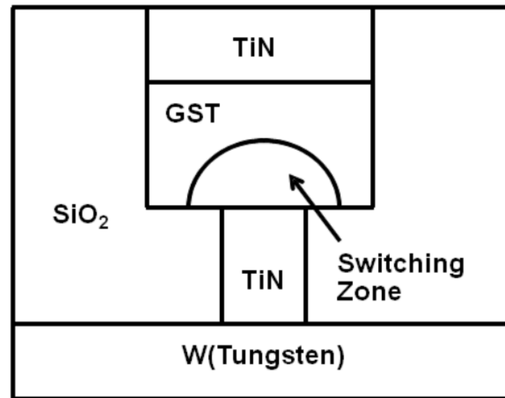


Figure 2.5 A typical Schematic of a two-terminal PCM 'mushroom' cell design showing the active switching region in the GST layer. (Reprinted from [51]).

Papandreou et. al. [77] reported that there are two alternative approaches to program the PCM cell: SET to RESET and RESET to SET programming processes. Both can be performed by understanding and controlling the relationship between cell resistance levels and programming current, as shown in Figure 2.6. In the RESET to SET programming approach, the PCM cell starts with a RESET programming current to produce completely high resistance (amorphous) material. Then, various amplitudes of SET programming are sequentially applied to crystallize partially the amorphous material into lower intermediate resistance states for various application of logic levels. Under these amplitudes, the resistance of the cell may only be decreased by increasing the crystalline volume. Thus, for going back to the high resistance state, sufficient voltage is applied to induce melting and quenching of the crystalline region for re-amorphization. The crystallisation process is used here to modulate the multiple crystalline volumes in the amorphous (mushroom) programming region. This leads to achieve distinct configurations of amorphous and crystalline regions, and then place the cell in different resistance states corresponding to distinct voltage applications that can be used for digital data storage. The lower intermediate resistance states are realized mainly through the gradual enlargement of the crystallisation region induced by current-driven Joule heating processes and then the output logic states, ‘1’ and ‘0’, are decided by determining a threshold voltage

switching, discussed in previous sections. However, it was found that this approach invariably leads to the formation of a crystalline ‘halo’ (ring) surrounding the active programming region during the crystallization process, which can have severe consequences on the achievable storage density in real devices [78].

Alternatively, in the SET to RESET programming approach, the initial phase of the GST material can be completely crystalline, i.e. programming starts with a SET pulse. Partial amorphous regions are then created by applying different amplitudes of the RESET programming pulses for various logic applications. The reset pulses with an appropriate amplitude may induce higher temperatures in the active GST area that exceeds the melting temperature leaving no time for crystallisation due to rapid quenching. This technique causes the resistance of the amorphous and crystalline GST zones to be in series with each other as shown in Figure 2.7. The size of the amorphous dome is controlled to place the cell in multiple resistance states, i.e. amorphous area with height h_2 has more volume than that with height h_1. A higher volume of amorphous material places the cell in a higher resistance level. This approach can be more appropriate since “halo” effects will not create during the erasing processes [78]. Consequently, in this research program the focus is mainly on using the second approach as a programming stagey to achieve a better control over the higher resistance states for producing distinct digital patterns, i.e. staircase programming for different resistance forms regarding various binary logic functions to implement logic gate functionality as will discuss later in chapter 6.

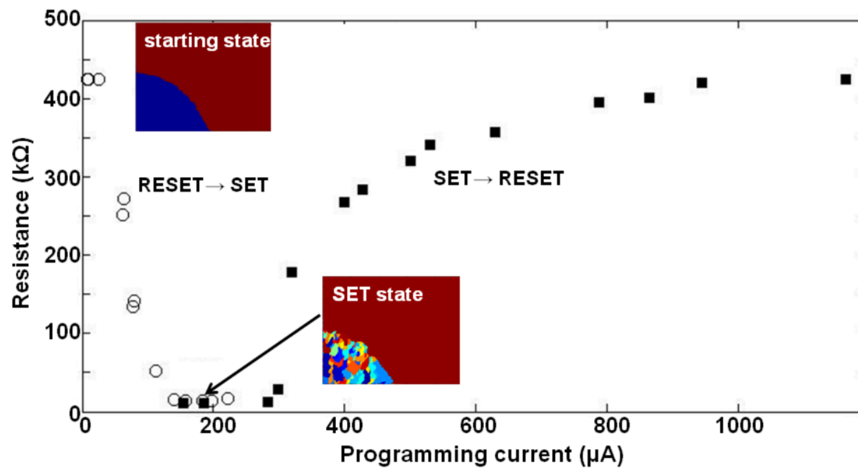


Figure 2.6. the characteristic resistance-current 'U' curve, in this case for a PCM cell of the type shown in Figure 2.5. The amorphous (reset) state (blue region) corresponding to the far left of the U curve, and the fully re-crystallised (set) state (different color corresponds to a different crystallite grain). (Reprinted from [51])

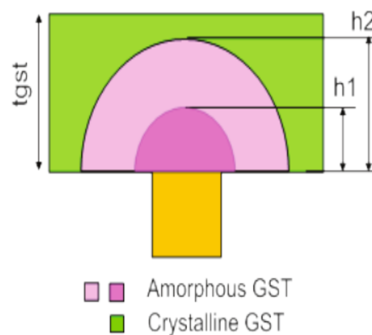


Figure 2.7. The height of the amorphous regions in a crystalline background material (h1 → resistance R1, h2 → resistance R2, h2>h1 => R2>R1). Reprinted from [53].

2.4 Two-Terminal PCM Cell Structure Concepts

In a two-terminal PCM cell, the region between the two electrodes might crystallize/amorphize entirely or only partially with a specific design of the cell. Even a relatively small active area of the phase-change material can be programmed by small amplitude pulses. The temperature increases to a few hundred degrees, in the active area, can be controlled by applying a staircase pulses under a known phenomenon, named Joule heating

that will be enough for the material to crystallize or amorphize from an initial background phase.

The main requirements on a logic memory cell are fast read and write times, low set and reset currents, a high number of read and write cycles, long data retention and high scalability [79]. All of these requirements depend on the essential properties of the chosen chalcogenide phase change material, as discussed in section 2.2, and also on the cell or device geometry through the interaction between the surrounding materials with the phase change material. Depending on standard lithographic structuring, PCM device geometries can be classified into one of two main categories: contact-minimised, or mushroom PCM cell, and volume-minimised cell, which is also known as a confined or Pillar PCM cell. In the contact-minimised cell structure, the cross-section area of the metal contacts (heater) is scaled to confine the current flow for increasing temperature in the phase-change material and then producing enough Joule heating effect for phase transitions. In the volume-minimised approach, a region of the phase-change material, which is in contact with the metal heater, is confined and highly scaled to achieve a highest current density for the Joule heating phenomenon [34][37]. Consequently, the following discussion will review basic structural and material design considerations of both main categories beginning with the commonly available structures, as a good starting point to inform and guide the design of the three-terminal device structure proposed in this work, aimed at both reducing the programming current and increasing the controllability and manufacturability of the structure.

2.4.1 Volume-Minimised PCM Cell

Volume-minimised PCM cell is formed of a narrow channel of phase-change material placed between two electrodes to govern the current flow for heating a part of the material, as shown in Figure 2.8. The most obvious structure in this category is the pillar or the pore cell. The volume-minimised cell structures are designed to be more thermally efficient, with lower

RESET current requirements though successfully confining the switching volume of the phase change material within the cell geometry [81]. Significant research efforts have been spent exploring a variety of volume-minimised cell structures, focusing on electrical switching and scaling characteristics for low programming energy. For instant, in the pore cell structure, the size of the switching volume is mostly determined by the pore size that confines the switching volume of the phase change material in order to create a small cross-section of a heated volume within the phase-change materials for programming as shown in Figure 2.8(b). This reduction in heated volume consequently leads to reduce the switching current and energy as shown in Figure 2.8(c).

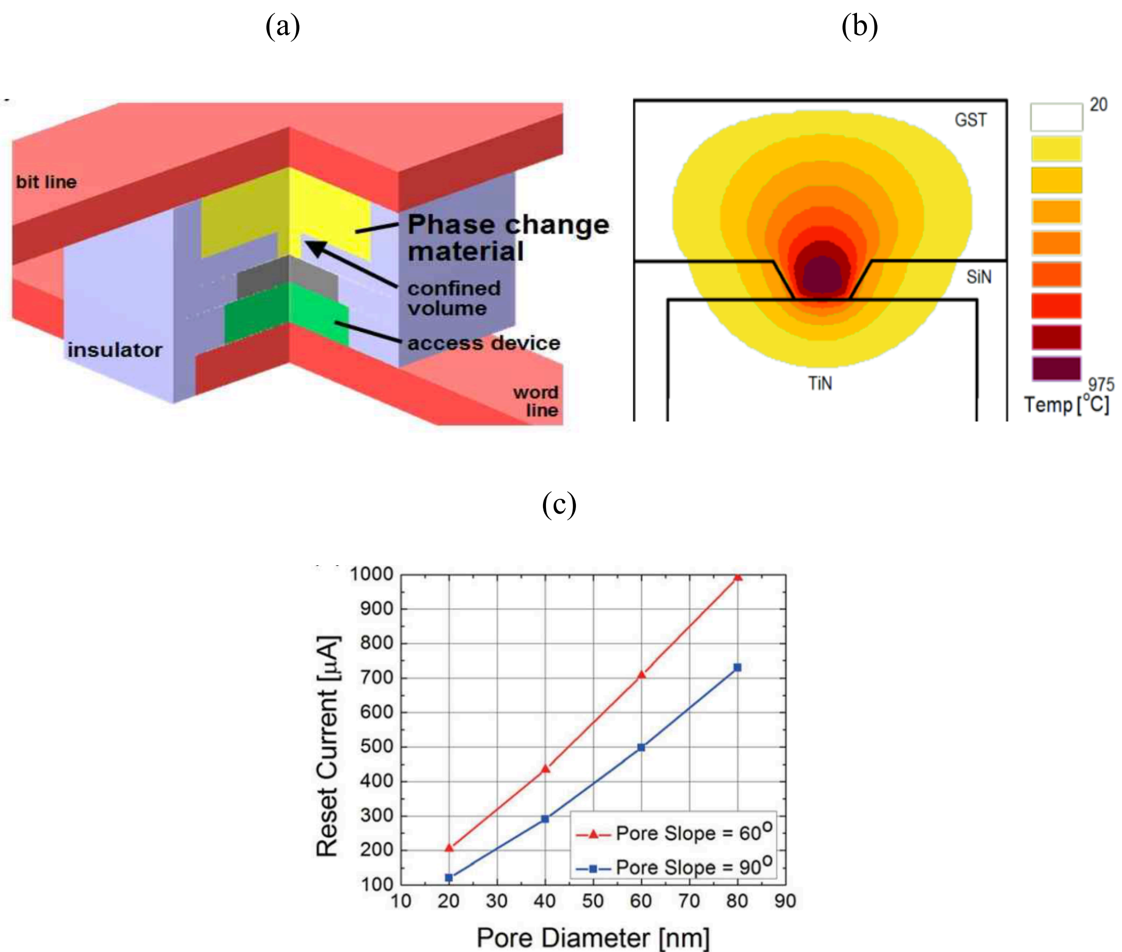


Figure 2.8 A typical volume-minimised cell with (a) a pillar cell design, or (b) a pore cell design, that confined volume of the phase change material in order to create a small cross-section within the PCM device, and then (c) reduction in the RESET current under the effect of pore diameter. (Reprinted from [82]).

However, the fabrication of such volume-minimised structures offers significant challenges. A filling of nanoscale holes with high aspect ratio is difficult using standard techniques, such as Physical Vapor Deposition (PVD) or Chemical Vapor Deposition (CVD) sputter deposition technique [82]. A development of such a volume-minimised cell fabrication for phase change materials will be necessary to enable continued scaling of pore cell devices for lower RESET switching current and achieve a highly scaled pillar-GST interface [80].

2.4.2 Contact-Minimised PCM Cell

Contact-minimised (or vertical) PCM cell is formed of a narrow cylindrical metal electrode, to act as a heater, contacting a thin film area of phase change material. The most common contact-minimised cell structure is the mushroom cell as shown in Figure 2.5. A metal heater confines the current to heat a partial area of the phase change material, the area in the vicinity of the heater, to become crystalline or amorphous for multiple resistance states. In a two-terminal mushroom cell, it is most common to see that one of the metal contacts, typically the Bottom Electrode Contact (BEC), made of TiN with the smallest and thus most imperative dimension in order to reduce the programming current consumption, and provide the most efficient work when the heating is mostly generated in the phase change material at the top of the BEC [76]. Hence, it is beneficial to keep the switching volume as contained as possible within the phase-change material and thus away from the room temperature boundaries.

On the other hand, the switching volume occurs when a large expanse of phase-change material meets an electrode contact via a narrow heater that leads to concentrate the current flow for a higher Joule heating effect. So, the current density reaches its highest value at the material-heater interface when the contact area between the phase-change material and the heater is scaled down. Furthermore, heat loss is reduced in both directions. In one direction, heat loss is low because of the inherently low thermal conductivity of the phase-change material. In the other direction, heat loss is low because the small cross-section of the electrode

helps keep the overall thermal resistance high despite its high thermal conductivity. Thus, the vast majority of contact-minimised cells closely resemble the mushroom cells that offer the advantage of a potentially lower RESET current requirements to erase the switching volume (small aperture formed within the material) than the whole material layer.

The above review and discussion will be later used in this study for the efficient design of three-terminal logic devices. This will include investigation of scaling effect on switching current requirements, especially for producing distinct resistance states from SET (or melting) and Reset (or erasing) currents. The switching speed is another important parameter to review and consider in this work. The amorphization process is fast as the active region is heated up to the melting temperature and cooled down at very fast rates, within a range typically (10 – 40) $K.ns^{-1}$, in order to freeze into the amorphous phase instead of re-crystallising [78]. On the other hand, the rate of crystallisation is determined by the crystal nucleation rate and the crystal growth rate (both of which are of course functions of temperature). Hence the smaller volume of the amorphized material that is required to be re-crystallised in a cell, the quicker the re-crystallisation process will be (assuming that volume contains or can generate sufficient crystal nuclei during the crystallisation process and/or borders a region that is already crystallised and can grow into the amorphous volume).

2.5. Phase-Change Logic Devices

As discussed early in this chapter, the logic operation in the PCM cells is based on programming cycles of storing and erasing binary data in distinct resistance states under application of different voltage levels. These voltages are applied across the cell terminals to achieve partially resistive switching dynamics in the active volume within the phase-change material layer that is in contact with these terminals. However, logic functionality can be achieved through governing the relationship between the applied input signals (voltage or current) and the readout resistance levels within the PCM cells, discussed in section 2.4. This

has been previously performed using the conventional two-terminal phase-change memory cells connected in series or in parallel to provide logic functionality. This will be reviewed next.

One of the first theoretical studies about the concepts of distinct logic levels-based chalcogenide phase-change materials was proposed by Ovshinsky et. al.[54]. This study was reported that the concept of utilizing a Josephson junction switches (silicon transistors) for implementing Josephson circuit devices, such as memory cell, logic gate or shift register, could be replaced by a more compact nonvolatile memory element named chalcogenide Ovonic threshold switches (OTSs). Using the OTSs, the logic family implementation was also discussed in this study by employing a plurality of two-terminal chalcogenide switches in different configurations to build logic gates, such as NOT gate, as shown in Figure 2.9(a). Furthermore, the two-terminal switches were used to perform sequential logic operations of multi-phase clocking such as four-phase clocking cycle, each subsequent clock signal is 90 degrees out of phase from the previous clock signal, as shown in Figure 2.9(b). Thus, in this study, the use of nonvolatile chalcogenide material was considered within a sequential operation that allowed the logical output of a logic circuit to be stored and then passed to the next logic circuit in a logic chain, without affecting other logic circuits in the logic chain. In the 1990s, Ovonics Energy Conversion Devices company, by Ovshinsky et. al. [83], increased the research efforts on developing the phase-change technology for data storage by involving a thermally activated phase transition of the chalcogenide alloy in two-terminal switches, which known as Ovonic memory switching (OMS) elements. It should be noted that the OMS mechanism was discovered in some chalcogenide compounds such as Ge_2 Sb_2 Te_5 (GST) composition by electrically induced structural change, and then used to store binary information in a non-volatile two-terminal memory device, where the bits “1” and “0” are corresponding to the conductive and insulating states respectively.

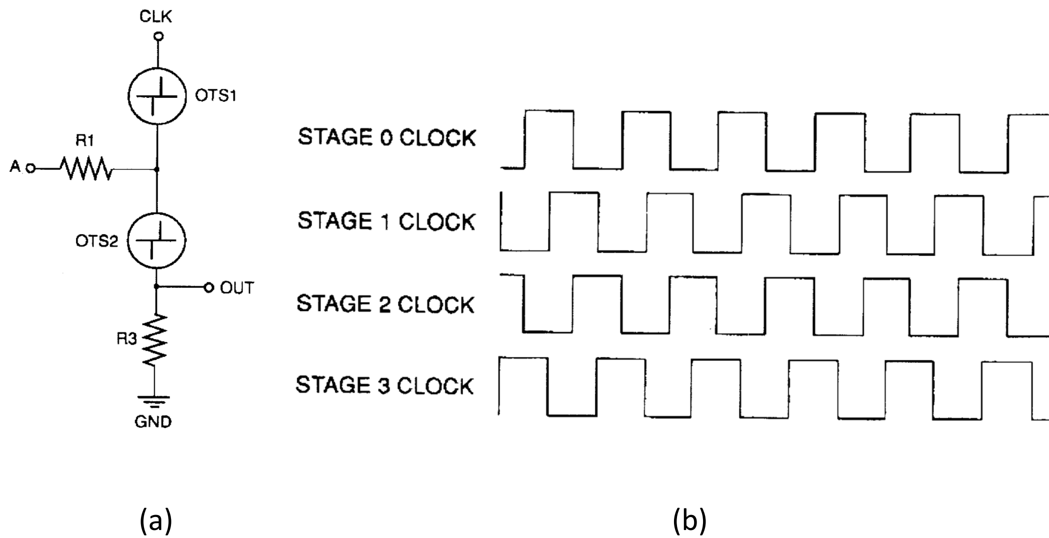


Figure 2.9 (a) A single logic gate depicts a single output inverting buffer by inverting the input, (b) The power cycling of a four-phase clocking cycle for instituting two terminal logic. (Reprinted from [54]).

In the mainstream of using non-volatile memory technology, the partial phase transformation in the chalcogenide materials was also investigated in two-terminal phase-change cells or devices to illustrate the ability of using PCMs for two main purposes. Firstly, they were used to build different binary components for arithmetic and logic computations: addition and subtraction that are based on phase accumulation effects [65] [78] [84]. Secondly, they were used as switches arranged in a configurable array of electrical interconnections to build different nonvolatile logic gates [64]. However, the two-terminal PC elements are used under certain circumstances of either applying a series of pulses of input voltages between the two terminals in sequential operations, which requires a longer time to complete a single logic operation, or integrating a configurable array of two-terminal phase-change cells as multiple switches to complete a particular logic operation under higher chip space density, which

requires a high integration densities for connecting the switches in series or parallel to provide a primitive logic functionality, such as the set functions of the logic gates.

In 2014, Desmond Loke et al. [84] proposed an approach to perform Boolean algebraic functions via applying a double-pulse (priming and switching) in sequential operations (i.e. multiple steps with longer operation time) because of the simple two-terminal feature of the PCM cells, as shown in Figure 2.10. These operations were sequentially performed via control of the switching from crystalline to glassy states to exhibit combinations of electrical-resistance levels, as output logic levels, that could compare with a reference resistance level to assign the logical states '0' or '1'.

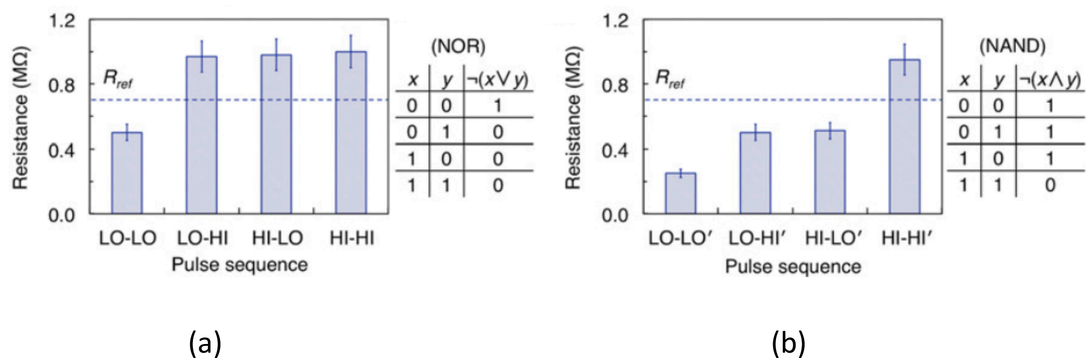
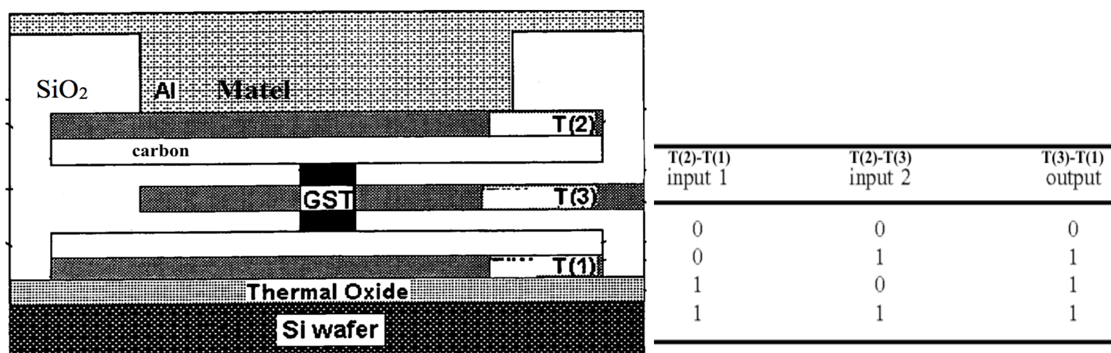


Figure 2.10 Multiple Boolean algebraic (logic) operations in a two-terminal PCM cell: (a)(x∨y)/NOR and (b) :(x∧y)/NAND operations. (Reprinted from[84]).

To overcome the sequential and scaling limitations of using two-terminal PC logic cells for implementing various logic operations, one study, by Ovshinsky in 2004 [66], provided a conceptual design of a three-terminal chalcogenide device to perform multiple bit data storage capability, as shown in Figure 2.11(a). A brief description of the three-terminal cell structure was demonstrated in this study by using a volume of chalcogenide material contained in the pore region of the device, and this pore was enveloped by three terminals (separated by an

insulating material) that are in contact with the chalcogenide material. Ovshinsky was theoretically offered, in Ref. [66] for the first time, the capability of applying independent input signals between different pairs of the three terminals (see Figure 2.11(a)), and the output could produce then from another pair of terminals. Such study opened up the possibility to develop and find a practical cell design of the three-terminal phase-change device instead of the two-terminal device for implementing different logic functions.



T(2)-T(1) input 1	T(2)-T(3) input 2	T(3)-T(1) output
0	0	0
0	1	1
1	0	1
1	1	1

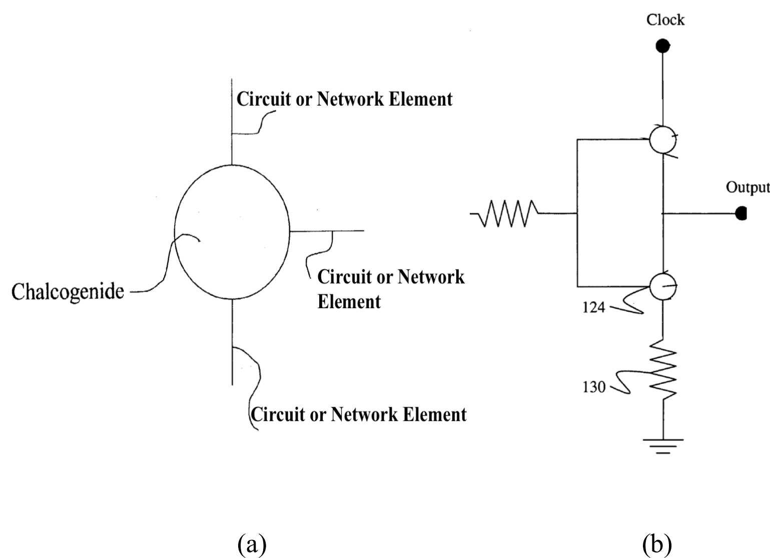
(a) (b)

Figure. 2.11 (a) A schematic structure of a three-terminal phase-change device: T(1), T(2) and T(3) are the bottom, top and side terminals, and (b) concepts of performing logic truth table of OR gate using the three-terminal phase-change device. (Reprinted from [85]).

In 2007 up to 2011, as a continuation-in-part of previous phase-change studies, Ovshinsky continued to study several different conceptual structures and configurations of the three-terminal chalcogenide devices to provide some operating principles for enabling various applications of logic computing environments based in whole or in part on the chalcogenide alloy or other phase change materials, as a viable complement or alternative to silicon-based technologies. In 2007, Ovshinsky et.al. [85], also reported a valuable theoretical approach to use a single three-terminal device for performing some primitive logic gate operations, such as OR gates in Figure 2.12(b). In 2011, the use of one or more three-terminal chalcogenide devices in various configurations of electrical interconnections, were discussed by T. Lowrey et al.

[86]. In this study, a number of three-terminal chalcogenide devices were used in series and parallel configurations to perform different primitive logic gates. For example, two elements of the three-terminal device were used in one configuration to perform the inverter logic function, as shown in Figure 2.12(b).

Although Ovshinsky and others offered valuable theoretical studies of the chalcogenide logic functionality based on three-terminal phase-change devices there were still some practical challenges that required addressing such as further details of a reliable design and structure, voltage conditions, material parameters and detailed simulations, to realize primitive logic gates, such as NAND or NOR, based a single configuration of a particular three-terminal cell or device having logic functionality.



(a) (b)

Figure 2.12 (a) Utilization of a three-terminal chalcogenide device as an interconnection device between two circuit or network elements, (b) Schematic of a logic inverter circuit through using three-terminal switching devices. (Reprinted from [86]).

2.6 Chapter Summary

It is clear from the discussion in this chapter that we have come a long way towards answering many of the key questions in terms of how far phase change (PC) materials and memory (PCM) devices, which can be structured and designed for particular nonvolatile logic functions. For logic operation purposes, It was found that the data storage could be performed by programming a partial area of the GST material for different resistance levels. In particular, the phase switching between the amorphous and crystalline states was observed to be influenced by the size, position and active area of the switching volume within the phase-change layer. Therefore, two main configurations of phase-change memory devices were reviewed: the contact-minimised (or mushroom) cell, and the volume-minimised (or also known as a confined or Pillar) cell. Detailed reviews and comparison of the traditional and emerging logic functionality of various PCM devices were discussed based on the aspects of performing sequential and parallel logic operations using two and three terminal devices respectively. However, it was found that a longer time is required to complete a single logic operation using two-terminal devices. That makes possible the use of three-terminal PCM devices even more feasible and practical for performing different logic functions, regarding occupied device area and operation time. In addition, some key challenges related to the nonvolatile logic data storage in PCM devices for intensive applications remain unaddressed, such as the effect of crystallization and amorphization behaviours which are influenced by the electrical and physical switching characteristics of the phase-change material in the devices. To address these challenges, the following chapters in this thesis provide valuable insight in using physically realistic and sophisticated Multiphysics modelling approaches, which combine the modelling of electro-thermal models with a practical phase-change model to study the feasibility of modelling three-terminal PCM logic devices having a deep description of mathematical models and modelling methodology.

CHAPTER 3: Electro-thermal and Crystallisation Models

Phase-change (PC) materials have been described in chapters 1 and 2 for their technological importance in data storage applications, and for their immense potential for unified data processing-memory device architectures and digital logic functionality. In particular, the potential of using three-terminal logic devices faces critical challenges to match or overcome the performance and logic operation of two-terminal phase-change devices. The operation of phase-change devices generally involves a number of complex and interacting electrical, thermal and phase-change processes. To understand the physical operations of phase switching dynamics in these devices, there is a need for mathematical models that describe the transient electrical, thermal and switching behaviour in phase-change materials between amorphous and crystalline states due to the application of electrical signals. The switching process from the crystalline to the amorphous state is denoted by amorphization, while the switching from the amorphous to the crystalline phase is denoted by crystallization. The amorphization process is performed by raising the temperature in the phase-change material above the melting point (900 K), and followed by quenching the same volume into the amorphous state with a very fast cooling rate, as indicated in chapter 2. Crystallization involves heating the initially amorphous phase-change materials to temperatures greater than the characteristic crystallization temperature, leading to nucleation and growth processes to irreversibly form the crystalline material after removal of the heat source. Thus, these processes need physically realistic-mathematical models to describe the electric potential and fields inside the devices, the corresponding temperature distribution resulting from Joule heating not only in the phase-change layer but adjacent layers for thermal design, and the crystallization dynamics within the phase-change layer.

Consequently, this chapter presents the main mathematical models describing the electro-thermal and phase-change models to enable the design, optimisation, and simulation of three-terminal phase-change logic devices and investigate their performance and feasibility.

3.1. Multiphysics PCM Model Concepts

According to the operation concepts of phase-change memories (PCMs) and devices, the phase-change materials within memory cells in different programming states are subjected to different electrical and thermal conditions. Hence, a fully coupled electro-thermal and phase change model is needed to physically describe the device operation. These three models are needed to understand the changes in the fundamental physics, and in order to develop a practical design and optimize the PCM cell for future applications. Figure (3.1) illustrates the effective thermodynamic parameters for the phase-change memory materials that have a direct effect on producing crystalline-amorphous phase transitions. Details on each model are provided next.

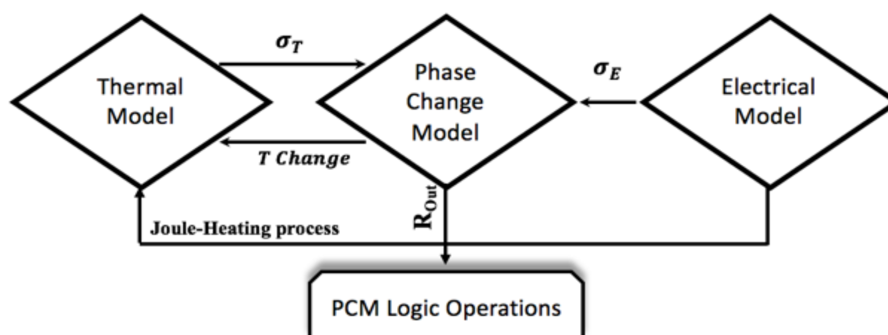


Figure. 3.1 Schematic of mathematical models of phase-change devices and their inter-relation.

3.2 Electrical Model

In the electrical model, a pulse of electrical source (voltage or current) is applied across the cell terminals to inject a sufficient current into the phase-change layer. This current is the source of Joule heating in the phase-change layer to produce the required temperatures for amorphization and crystallisation. Hence, the electrical model used in this work is well known by Laplace's equation, as described in Eq. (3.1) [87][88], that can be solved to evaluate the electric potential and then model current density distribution inside the phase change material.

$$\nabla(\sigma.\nabla.\mathrm{V}) = 0 \quad (3.1)$$

where V is the electrical potential, σ is the electrical conductivity and ∇ denotes the gradient operator.

Equation (3.1) clearly indicates that the scalar potential and hence the corresponding electric field E distribution in the devices are directly influenced by the spatial distribution of the electrical conductivity in the structure.[1]. The changes in the electrical conductivity, coupled with the crystalline and amorphous states, has a direct impact on the currents in the phase-change layer required for Joule heating. The heat source per unit volume (Q) generated inside the phase-change material is subsequently determined from the computed potential or electric field by the relationship:

$$Q = \sigma\,|\nabla V|^2 = \sigma\,|E|^2 \quad (3.2)$$

Consequently, the heat source is in turn used to calculate the temperature distribution in the PC layer during the phase transformation process as will be described later.

For modelling the change in the electrical conductivity with the material phase between the crystalline and amorphous states, the Bruggeman effective medium approximation (EMA) is

used for a mixture of two different conductivities[89][90]. This approach describes the effective relationship between the electrical conductivity and the fraction of the transformed crystalline material in the phase-change layer, which can be given by:

$$\sigma = \sigma_A (1 - \chi) + \sigma_C \chi \tag{3.3}$$

σ_A and σ_C are the electrical conductivities of amorphous and crystalline phases respectively, and χ is the volume fraction of the crystalline material in the mixture, which is associated with the phase transformation process that will be described in detail in section 3.4. The change in electrical conductivity in (3.3) is typically in the range of (2-2770) Ω^{-1} m^{-1} at room temperature [5][6], and is associated with the irreversible change in the volume fraction of the crystalline material, which is mainly a thermally driven process. To produce a more physically realistic model for simulating the logic functionality in a three-terminal PCM device, the electron transport and the electric field dependence of electrical conductivity need to be taken into account. Ielmini et.al. [76] proposed an electrical model using sub-threshold conduction regime to study the phase transformations in the amorphous chalcogenide material. Their model considered the electric field dependence of the amorphous phase electrical conductivity σ_A, which is given by equation (3.4), to obtain trap-limited conduction model with considering a voltage dependent activation energy, as discussed in preceding chapter. Thus, a quantitatively accurate prediction of the voltage dependence of subthreshold current for electrical transport in amorphous chalcogenide in amorphous phase chalcogenides can used for simulating realistic model of a particular logic functionality in a three-terminal PCM device.

$$\sigma_A = E^{-1} . 2q\,(N_{T1} + N_{T2}) \frac{\Delta z}{\tau_0}\; e^{\frac{E_C - E_F}{K_B T}} \;\; \sinh\left(\frac{qE}{K_B T}\frac{\Delta z}{2}\right) \tag{3.4}$$

where, q is the elementary charge, N_{T1} and N_{T2} are the trap concentrations at different energy levels, E_C and E_F are the mobility edge at the conduction band and the Fermi energy

respectively, τ_0 is the characteristic attempt-to-escape time for the trapped electron, T is the absolute temperature, and Δz is the inter trap distance between two traps. Typical values for these parameters for the phase-change material GST are listed in Table 3.1.

TABLE 3.1 The physical parameters of various materials formed the PC cell [76]

Parameters	Values
N_{T1}+ N_{T2}	1×10^{25} m^{-3}
N_{T1}	0.5×10^{25} m^{-3}
τ_0	1×10^{-15} s
Δz	2.5×10^{-9} m
E_C-E_F	0.35 ev
q	1.6×10^{-19} C
K_B	1.38×10^{-23} J. k^{-1}

3.3 Thermal Model

During the phase transformations, the variations in the electrical characteristics have a direct effect on inducing local heating in the PC material. The passage of electrical current through the material leads to Joule heating which raises the temperature inside the material. By using the heat source power density Q derived from the electrical model, the temperature distribution (T) of the whole material can be calculated by solving the heat conduction equation [66][99][100], which is given by:

$$\rho\, C_p \left(\frac{\partial T}{\partial t}\right) - \nabla.(K\nabla T) = Q \tag{3.5}$$

where ρ is the material density, C_p is the specific heat capacity per unit mass, K is the thermal conductivity, and Q is the heat source obtained from the electrical model.

Since the amorphous and crystalline phases have different thermal conductivities, the changes in thermal conductivity of the material during the phase transformation can also be modelled using the Bruggeman effective medium approximation (EMA) [89][90], which is given by:

$$K = K_A (1 - \chi) + K_C \chi \tag{3.6}$$

where K_A and K_C are the thermal conductivities of amorphous and crystalline phases respectively, and χ is the volume fraction of the crystalline material in this mixture.

In general, the variations in the thermal characteristics of the GST phase-change materials are directly dependent on resulting temperature distribution. At room temperature, the thermal conductivities of the crystalline and amorphous GST material are in the range of (0.46-0.57) W/m.K and (0.19 to 3.5) W/m.K respectively, as reported in [90] [94]–[98]. The specific heat capacity of the GST was reported between 202 and 210 J/kg.K [96] [99][100]. The density of GST was reported between 6150to6200 kg/m3[9][15][17][20]. Hence, the proposed values of the thermal parameters in this study will be discussed in the next chapter.

3.4 Phase-Change Models

A phase change model is a physical description for the phase switching characteristics inside the phase-change material. The set and reset processes in the PCM cell, which represent here in this study the write and erase operations of a particular logic operation, are mainly associated with the amorphization and crystallization mechanisms of the phase transformation in the GST materials. The physical behaviour of both amorphization and crystallization dynamics is mainly based on the temperature distribution obtained from the electrical and thermal models. As mentioned in previous sections in this chapter, the reversible phase transitions between amorphous and crystalline states are realized by injecting a sufficient current-induced Joule

heating for either crystallization by heating the GST material below the melting temperature and allowing crystallization of the amorphous material, or amorphization by heating the GST material above the melting temperature and then followed by a fast cooling process to quench into the amorphous phase [12][16][17]. In case of the amorphization process, if the rate of the cooling process is very slow, this can potentially lead to recrystallization of the melted material by allowing some nuclei to form during the cooling process [78][99]. Ignoring the melting and cooling thermodynamics for simplicity, the melting and cooling processes can be easily modelled by assuming that each location of the phase-change material that exceeds the melting temperature threshold will cool down to the amorphous phase. Crystallization on the other hand, is a complex process that involves nucleation and growth. There are a number of studies that described various crystallization models with varying complexities [16][17][2]. These studies investigated fundamental models such as (1) JMAK theory, (2) rate equation method and (3) classical nucleation and growth theory, which are discussed in detail next.

3.4.1 Johnson-Mehl-Avrami-Kolmogorov (JMAK) Model

One of the most common models used in many studies to describe the volume fraction of crystallized material in a phase-change material as a function of temperature and time is Johnson-Mehl-Avrami-Kolmogorov (JMAK) model. The JMAK model provides approximate calculations of the volume fraction of crystallized material as a function of time $\chi(t)$ under isothermal (constant, uniform temperature) annealing conditions [100]–[102], which is given by:

$$x(t) = 1 - \exp[-k_B\, t]^n \qquad (3.7)$$

Where t is time, n is the Avrami coefficient ($0 < n < 1$), k_B is the Boltzmann constant, and k is the crystallisation rate constant depending on temperature through Arrhenius equation that given by:

$$k(T) = v \exp(\frac{E_A}{-k_B T}) \quad (3.8)$$

where ν is the attempt frequency factor, E_A is the activation energy for crystallization (including both nucleation and growth), which was reported previously to be within the range (1-2.26) eV for the GST material according to Kissinger analysis [2][103], T is the absolute temperature and k_B is the Boltzmann constant.

Although several studies of crystallization kinetics of phase change materials use the JMAK equation, this model is only valid under specific conditions. In this model, the nucleation is assumed to be random and uniform everywhere, and the nucleation rate is independent of time. This simplified model is used as a trade-off between complexity and computational efficiency. Finally, in this model it, is assumed that growth is interface controlled with a rate independent of cluster size (i.e. homogeneous) [2] [104]. There is experimental evidence, however, showing that the crystallization in GST starts on surfaces, at interfaces with the other substrates (i.e. heterogeneous nucleation[105] [106]). In addition, the occurrence of an incubation time before starting the crystallization process, provides evidence that the nucleation rate cannot be considered as a time-independent during the whole crystallization process [107]. Hence, the JMAK approach is not particularly the most physically realistic model to use to simulate the phase transformation processes in phase-change materials and devices.

3.4.2 Rate Equation-Reaction Method

Another approach, using chemical rate equations, has been used by several studies to describe the volume fraction of crystalline clusters during the nucleation and growth processes in a phase-change material. The reaction rates of forming crystalline clusters are calculated by assuming that the crystalline cluster can shrink or enlarge by loss or addition of one molecule. In a real system, there are particular interactions between the crystalline clusters which are distributed with different sizes to describe the behaviour of the crystallization process [2][108]. Hence, this approach considers clusters of different sizes and their interaction in an amorphous material in terms of reaction rates between clusters of different sizes. The attachment and detachment of monomers (a single molecule that may combine together to form nuclei) to an existing crystal cluster is used to describe the decay and growth of clusters respectively. A set of simultaneous differential equations for the different cluster sizes is used to model the reaction kinetics of growing or decaying crystalline clusters of individual GST molecules. A kinetic reaction through the rate equation describes the development of the density of the clusters *f(n,t),* of size n by:

$$\frac{\partial f}{\partial t} = g(n-1,t)f(n-1,t) - d(n,t)f(n,t) - g(n,t)f(n,t) + d(n+1,t)f(n+1,t) \quad (3.9)$$

with $n \geq 2$, *g(n,t) and d(n,t)* are growth and dissolution reaction rates respectively of a cluster of size n. In order to solve the above equation, the growth and dissolution rates are determined by reaction rate theory [109], which are given by:

$$g(n,t) = 4\pi r^2 \lambda f(1,t) \gamma \exp\left(-\frac{\Delta G_{n\to n+1}}{2K_B T}\right) \quad (3.10)$$

$$d(n+1,t) = 4\pi r^2\, \lambda\, f(1,t)\, \gamma^*\, \exp\left(-\frac{\Delta G_{n+1\to n}}{2K_B T}\right) \tag{3.11}$$

where *f(1,t)* is the density of monomers at a given time, *r* is the cluster radius, λ is the jump distance, and γ^* is the molecular jump frequency at the interface between amorphous and crystalline phases. The free energy differences between sizes *n* and *n+1* is given by:

$$\Delta G_{n\to n+1} = \Delta G(n+1,t) - \Delta G(n,t) \tag{3.12}$$

where ΔG is the bulk free energy difference per monomer. Hence, during the phase transformation, the size distribution of crystalline clusters at any instant of time can be evaluated by solving the rate equation (3.8).

A successful simulation of crystallization in $Ge_2Sb_2Te_5$ by Senkader et. al.[2] was carried out based on the rate equation model. In their study, the volume fraction of the crystalline material was computed by integrating the size distribution function over the different cluster sizes and compared with experiments as shown in figure 3.2.

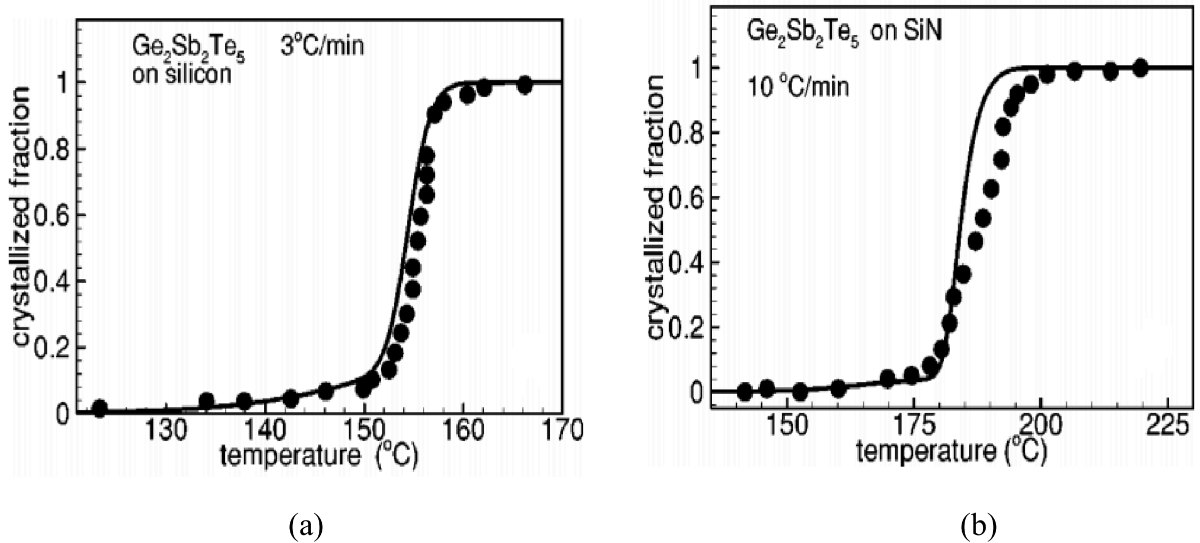


Figure 3.2 Experimental [1] and simulation results of crystalline fraction volume in a $Ge_2Sb_2Te_5$ alloy, shown in (dots) and (lines) respectively, as a function of temperature ramp rate of 3,C/min for (a) GST on silicon and (b) GST on SiN. (Reprinted from [2]).

Although the rate equation method can describe crystalline cluster dynamics during the crystallization, it uses a series of differential equations for each cluster size to describe time-dependent density changes. Hence, the crystallization modelling approach based on rate equation method is more computationally intensive and complex to implement, especially when the crystalline volume fraction is computed at every time step and calculating for each grid location in the model physical model.

3.4.3 Classic Nucleation-Growth Theory

This common method is based on the classical nucleation and growth theory [109]. The crystallization behaviour based on this theory has been discussed well and covered previously in more details by Gibbs et al. [6]. Based on the assumptions of this theory, the main driving force for the crystallization process during the phase transformations is from the difference in the Gibbs free energy between the amorphous and crystalline phases in the phase-change materials. In this theory, the crystallization process starts with creating small and unstable crystallite clusters [31][33][34]. Once the crystallites reach a critical size, then they become stable with the ability to grow rather than decay. This method can take into account the two main different nucleation types: homogeneous nucleation when the nucleation occurs in any region of the bulk of the GST material, without involving other substances, or heterogeneously when the nucleation occurs around impurities, surfaces and at the external boundaries of the GST material when the material phase is in contact with other substances[2][112].

3.4.3.1 Homogeneous Nucleation

According to the classical nucleation theory, the steady-state homogeneous nucleation rate I_{hom} (i.e. the number of newly formed nuclei per unit time and volume) is given by [31][113]:

$$I_{hom} = \sigma_{hom}.\exp\left(-\frac{E_{an}}{K_B T}\right).\exp\left(-\frac{\Delta G_{Clust}}{K_B T}\right) \tag{3.13}$$

$$\Delta G_{Clust} = \frac{16\pi\gamma^3}{3\Delta g^2} \tag{3.14}$$

where σ_{hom} and E_{an} are a pre-factor and the activation energy related to nucleation mode, ΔG_{clust} is the excess free energy barrier (critical free energy) to form stable homogenous nuclei, γ is the amorphous-crystalline interfacial energy and Δg is the Gibbs free energy difference between the crystalline and the amorphous phase. The temperature dependence of the Gibbs free energy Δg is the driving force of the crystallization process, which can be calculated using the melting temperature (approximately 900 K for GST) and the latent heat of fusion at the melting point of the phase-change material [2][114]:

$$\frac{\Delta g}{v_m} = \Delta H_f \frac{T_m - T}{T_m}\left[\frac{7T}{T_m + 6T}\right] \tag{3.15}$$

where v_m is the volume of a phase-change material monomer, which can be easily estimated from the material density and the molar weight of the material ($v_m = 2.9\times10^{22}$ cm^3, for GST), ΔH_f is the enthalpy difference of fusion at the melting point (ranges from 610 to 625 J/cm^3 , for GST) [2], and T is the absolute temperature.

3.4.3.2 Heterogeneous Nucleation

In reality, it is difficult to expect that the nucleation process in the phase-change material to occur with equal probability in all parts of the whole amorphous volume. It is thus important to take into account the effects of imperfections in the material and surrounding surfaces in the phase-change material as nucleation sites. Hence, the occurrence of heterogeneities is very difficult to ignore during the crystallization process. A simple and popular approach to include

heterogeneous nucleation was introduced by Volmer based on the Gibbs model, using a flat substrate acting as a heterogeneous nucleation site [112][69][115]. Under the assumption of isotropic phases, the crystalline cluster nucleates on the heterogeneous surface, interfacing with either the amorphous parent phase or the heterogeneous substrate, with a spherical cap of radius (r), as shown in Figure 3.3. This spherical cap can be completely described by calculating the exposed volume function *f(θ),* ($1 \leq f(\theta) \geq 0$) as a function of the wetting angle θ, given by:

$$f(\theta) = \frac{(2+\cos\theta)(1-\cos\theta)^2}{4} \tag{3.16}$$

where, the wetting angle $\theta = 180$, $f = 1$

In this case, the Gibbs free energy required for the formation of a heterogeneous cluster will be influenced by the presence of foreign substances in contact with the amorphous material during the crystallization process. If there is no heterogeneous cluster (homogeneous nucleation site), the wetting angle will be θ =180° and $f = 1$. Then the free energy barrier for heterogeneous cluster formation ΔG_{het} is influenced by the impurity nucleation sites, and will be significantly lower than the free energy barrier for the homogeneous cluster by [112][69]:

$$\Delta G_{het} = \Delta G_{clust} \cdot f(\theta) \tag{3.17}$$

The steady state nucleation rate for heterogeneous nucleation and diffusion-limited kinetics is given by [69]:

$$I_{het} = \sigma_{het} . \exp\left(-\frac{E_{an}}{K_B T}\right) . \exp\left(-\frac{\Delta G_{het}}{K_B T}\right) \tag{3.18}$$

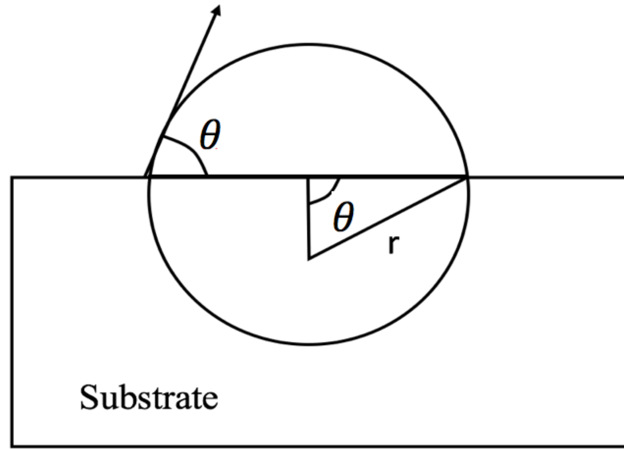


Figure 3.3 heterogeneous cluster formation based on Volmer's spherical cap mode, whose volume is $f(\theta) \times \frac{4}{3} \pi r^3$. (Reprinted from [69]).

3.4.3.3 Crystal Growth

The nucleation theory described above can be used to model the formation of stable nuclei in the parent amorphous phase. Once small crystalline nuclei are formed, crystalline clusters are assumed to change sizes by the attachment and detachment processes with other monomers, and by transporting across the interface from one phase to the other under another thermodynamic driving force for this process as well. Hence, it is more likely that the size of nuclei will continue to grow at a constant speed (V_g) rather than shrink by adding monomers to the crystalline clusters. To understand the fundamental mechanisms of the growth velocity, the formula of the crystal growth rate was proposed by Meinders et. al. [116] as follows:

$$V_g = v_0 \,.\, \exp\left(-\frac{E_{ag}}{K_B T}\right).\,(1 - \exp\,(-\frac{\Delta g}{K_B T}) \tag{3.19}$$

where, v_0 and E_{ag} are the pre-factor and the activation energy related to the growth mode [117].

According to equation 3.18, the crystal growth rate is a temperature dependent, hence the classic nucleation theory provides a valuable estimation of the cluster nucleation and growth

rate based on the crystallite size distribution. However, some basic assumptions and limitations of using classical nucleation model are summarized as follows:

- Nuclei are assumed to grow rather than dissociate when their size exceeding the critical size. This is only true when the size of the nuclei is larger than the critical size. The nuclei with sizes near to the critical size are possibly involved by a dissolution process, and that is not governed by the classic nucleation theory.
- Nucleation theory deals with the nucleation and growth rates of the crystal clusters, which are temperature dependent, therefore this theory is based on steady-state crystallization and does not directly involve transient subcritical cluster formation.
- The crystallization process manages the balance between the loss and formation of old and new clusters respectively. However, this balance is true at the early stage of the process when the nucleation rate increases then decreases at the later stages.

3.5 Review and Comparison of the Phase-Change Models

As discussed early in this chapter, there are three common approaches that could be used to study and understand the crystallization dynamics in phase-change materials, and each approach has inevitable limitations. The crystallization dynamics has a direct effect on the electrical resistance in phase-change materials that determines the operation of non-volatile logic-memory applications. Modelling changes in the material resistance as influenced by the changes in the physical parameters of the GST phase-change materials, such as the electrical and thermal conductivities, provides a physically realistic model of the crystallization process of the chalcogenide materials under different temperature histories.

The crystallization process has been modelled and simulated using different approaches in the literature. The JMAK model describes nucleation in a random and uniform process under isothermal annealing conditions. Also, the nucleation rate is assumed constant for the entire crystallization process for different cluster sizes [118]. Despite these limitations, this model is very fast due to its simplicity. However, this model may not be applicable to use in crystallization process in phase-change material of this work and under electrical applications, as it is not feasible to simulate a constant nucleation for the whole crystallization process under different voltage levels [107].

Hence, we used the classical nucleation-growth model to provide a compromise in terms of speed and sufficient physical details between the computational complexity of the rate equation approach and simplicity of the JMAK approach. Although this approach does not involve direct transient calculations and non-equilibrium crystallization (i.e. it works on steady-steady nucleation/growth rate calculations), it is still faster than the rate equation approach, and physically more accurate than the simplified JMAK approach. Also, this approach can take into account the separate evaluations of both nucleation and growth rates which control the crystallization process and able to predict the volume fraction of the crystalline material as a function of time and space for the phase-change material subjected to the temperature distribution under various electrical applications. Consequently, the simulations of the crystallization process for the work in this thesis is performed by calculating the nucleation and growth rates separately based on the classical nucleation theory, as will be discussed in following chapters. The simulation will base on the implementation of coupling the phase-change model with the electrical and thermal models.

3.6 Chapter Summary

It is clear from the discussions in this chapter that it is essential to develop physically realistic electro-thermal/phase change models to understand the fundamental physics of the phase change processes under different voltage levels. It was found that modelling changes of the crystallization events in the phase-change memory devices provides a realistic model of using the three-terminal devices for particular logic functions, such as performing a set of logic gates including NAND and NOR logic functions. The mathematical models of electro-thermal and phase-change behaviours have been presented to enable the design, optimisation, and simulation of three-terminal phase-change logic devices and investigate their performance and feasibility. At the start of the chapter, a description of the electrical model was presented by using the Laplace equation, and then the thermal modelling was discussed based on the heat-transfer equation. It was highlighted that the electrical and thermal characteristics (i.e. electrical and thermal conductivities) have a direct mathematical relationship with the variations in the crystalline volume fraction of the phase-change material. A detailed review of a number of studies that described various crystallization models with varying complexities for calculating the crystalline volume fraction, was presented to find a physically-realistic modelling changes in the electrical and thermal conductivities of the GST phase-change materials. Review of the three common phase-change modelling approaches: JMAK, rate equation and classical nucleation and growth approaches, showed that the use of the classical nucleation-growth approach for the simulation of the 3T modelling devices could successfully approach to provide some confidence in the programming device. This model is more accurate than the simplified JMAK approach and faster than the rate equation approach, as it does not involve direct transient calculations, as will be further described in the next chapter.

CHAPTER 4: Design and Numerical Implementation of A Vertical 3T Logic Device

For the purposes of modelling a realistic three-terminal PCM device for future cell structure design and optimization, it is essential to develop a physical model to use for the device simulations. The model should be able to track the changes in the crystallization dynamics during phase transitions. In the preceding chapter, the summary and comparison of different phase-change models for simulations have been discussed and reviewed along with the other main sub-models of electrical and thermal characteristics. This chapter presents advanced modelling of multi-physics numerical approach to use in a realistic three-terminal PCM device design. The use of a practical multi-physics numerical approach provides valuable insight into the physical processes that involve successful use of different logic applications-based phase change materials for electrical data storage. The classical nucleation and growth approach, which was discussed in the previous chapter, is implemented here in finite-elements to realistically model the write, erase and read processes in phase-change logic devices. The use of the nucleation and growth model improves the transient numerical calculations of creating stable crystalline nuclei and their subsequent growth following the thermal history in the phase-change material during phase switching processes.

The following sections in this chapter will discuss the proposed three-terminal PCM cell design and a simulation methodology including the implementation details of the classical nucleation and growth model. The simulation methodology section concerns more efficient design of two-dimensional (2D) finite-element model in the multi-physics implementation in Comsol to simulate the write and erase processes for practicable three-terminal phase-change logic devices.

4.1 Three-Terminal Cell Structure Concepts

In the mid of 2000s, a conceptual three-terminal GST device structure for logic functionality was proposed by Ovshinsky et. al.[119], as shown in Figure. 4.1. In their study, they pointed out that a standard three-terminal device formed of a pore filled with a chalcogenide material in the central portion of a three-terminal device and surrounded by three metal terminals as electrical contacts; bottom, top and side electrical terminals, which labelled in Figure. 4.1 by T(l), T(2), and T(3). An insulating or dielectric material was used in the device to separate electrically the three terminals. The pore of the device could be cylindrical or non-cylindrical in shape. If the pore was created cylindrically, the side terminal would be preferably circular in shape, it could be circumferential in shape if the pore was non-cylindrical. The three terminals could be formed of a high electrical conductivity material, such as of a titanium-tungsten (TiW) or titanium nitride (TiN) layer, while the chalcogenide and the dielectric materials were a typical used material of a $Ge_2Te_2Sb_5$ composition, labelled GST in Figure 4.2, and Silicon Dioxide (SiO_2), respectively.

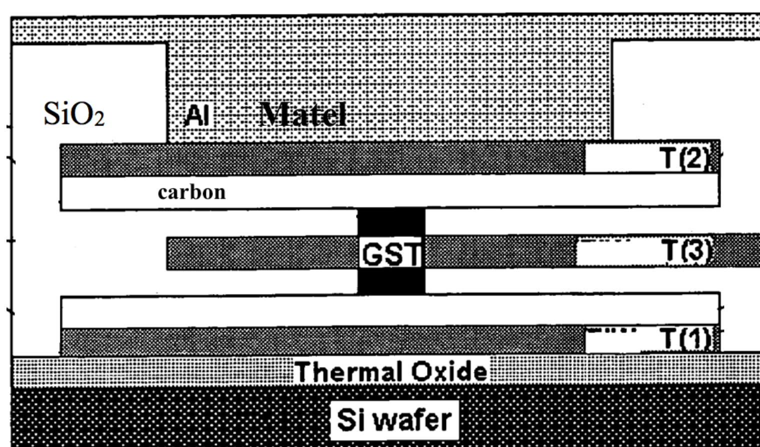


Figure. 4.1 A schematic structure of a three-terminal phase-change device: T(1), T(2) and T(3) are the bottom, top and side terminals respectively. (Reprinted from [119]).

Beyond the conventional structure of the three-terminal phase-change device shown in Figure. 4.1, geometry optimization (i.e. dimensions and thicknesses of the layers in the device) along with high energy efficiency (through the selection of the insulating materials surrounding the phase change cell to obtain the appropriate thermal transients and history in the device) must be considered for the development of practical three-terminal phase-change device structures. Furthermore, the electrical communication between the terminals, in the three-terminal PCM device, must occur when the electrical current can flow through the chalcogenide material and via a short electrical pathway, as discussed in chapter 2, to control cell resistance levels. Hence, to explore the above limitations of the design, fabrication, and achieve applicable prototype of three-terminal PCM device, the focus of this research and simulations in this thesis is based on the vertical structure of three-terminal logic devices, due to its existing fundamental roots and understanding in PCMs, and therefore capability of manufacturing or experimental testing where possible. Nevertheless, the lateral three-terminals cell structure will be briefly discussed in chapter 7 of this thesis for future work because it has a higher chip space density than the vertical cell structure[6]. That may be more reliable for achieving multilevel storage density, binary or non-binary storage data.

The vertical three-terminal PCM device structure, or also known as the mushroom cell structure as explained in chapter 2, is structurally classified as a contact-minimized cell structure through scaling the cross-sectional area of a contact heater with the phase change material. Hence, the vertical three-terminal cell structure is expected to provide the opportunity to be used in the future commercially-viable cell structures of PCM technologies i.e. easy to fabricate and integrate with a nanoscale size of the device materials compared with complementary metal-oxide semiconductor (CMOS) technologies, and of current interest in investigations for both academic research and industrial PCM applications (e.g. phase-change memory and logic applications). In this research programme, the general three-terminal vertical

device structure concept indicated Figure 4.2 is proposed and consists of an active phase-change material, such as a GST, surrounded by three metal terminals, which are structurally inserted to realize logic/memory three-terminal vertical cell, and surrounded by insulating dielectric material (insulator), as shown in Figure. 4.2. The proposed cell architecture here is used to investigate and predict the switching processes in the PCM alloy based on different voltage applications for reconfigurable logic-gate functionality. The three metal terminals (top, side and bottom terminals) are in electrical contact with the chalcogenide alloy. Thus, different voltages can be applied simultaneously across different pairs of cell terminals (with respect to ground on the third terminal) for writing and erasure, and for measurement of resistances during readout as will be discussed later in detail.

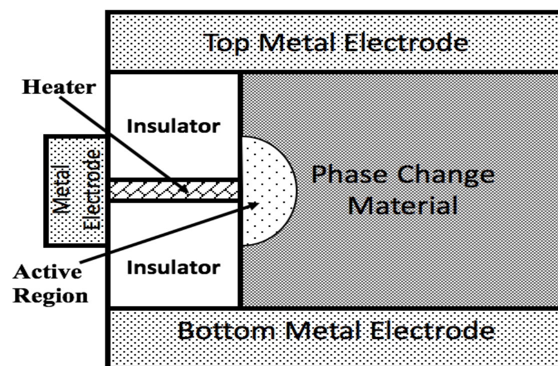


Figure. 4.2 A general schematic of three-terminal PCM 'mushroom' cell.

According to above discussion, the proposed cell structure of a vertical three-terminal element for the simulations of the logic functions is based mainly, in design, on the contact-minimized (mushroom) type. Thus, it can control the structural state of the whole or portions of the phase-change material within the vertical three-terminal PCM device during the programming processes. Partial programming approach can be achieved in the vertical cell structure if the structural volume of the resistive shielding (amorphous dome) is like cap or mushroom region within a crystalline material. If the amorphous region occurs across the

heater, in Figure 4.2, in such a way with a desired size and shape, like cap or mushroom, as discussed in chapter 2, the current flow can preclude to or from a particular terminal through a crystalline conductive pathway to the ground terminal. The current flow to or from the ground terminal will occur at least through an amorphous mushroom region, so that, the output cell resistance between the ground terminal, through the heater, and any other terminal is higher than it would be if a continuous crystalline current pathway was available.

Consequently, two of the three terminals are used as active terminals to apply appropriate voltages to create enough amorphous dome across the third terminal to control current flow and therefore resistance that develops across the different terminals of the device. The two terminals for the active voltages are set here to the top and bottom terminals of the cell, while the side terminal is set as a ground terminal. The pivotal role of this idea is to achieve control over the volumes of the amorphous and crystalline regions within the phase-change material, as will be discussed with more details in the next section. The third terminal, which is already resistively shielded by an amorphous dome, is connected to a ground electrode, as shown above in Figure. 4.2. So, the desired region of the phase-change material, which is in contact with the third (side) terminal, works as an active region during the programming processes.

4.2 Three-Terminal Logic Device Structure Considerations

As discussed in the preceding sections of this chapter, it is essential to develop a practical structure of the three-terminal (3T) PCM device for feasible device simulations. This is necessary to understand the electro-thermal behaviour involved within the chalcogenide-phase change materials for logic data storage, and then to design and optimize future PCM devices having a logic functionality. This section presents a detailed structure of physical layers and positions of the electrical terminals for the 3T vertical PCM cell that is proposed, as a physical structure, for reconfigurable logic device simulations.

4.2.1 Influence of Terminals

As discussed earlier in chapter 2, to produce resistive switching between high and low resistance levels, the desired size and shape of the active region in a vertical 3T-PCM cell must cove the heater-ground contact. Thus, the phase-switching process (between crystalline and amorphous) in the active region is mainly influenced by the materials, positions and contact areas of the electrical (top, side and bottom) contacts with the phase-change layer. Furthermore, some factors like geometry of the three terminals and cell layer structuring have pivotal roles in determining a lower amount of current flowing in the active region of the 3T-PCM device for high resistive switching performance. The high resistive switching performance is achieved when high temperature concentrations for phase switching processes shift to be in the active region. As a result, the programming current of high resistive switching performance can mainly be reduced by either accurate optimization of the cell geometry and materials, or by scaling the cell structure.

To design a practicable three-terminal PCM device having vertical (mushroom) cell structure with high resistive switching performance based lower programming current, a simple analytical study, reported by Ielmini et. al. [120] considered cell geometry optimization. The study revealed that the programming current for creating a sufficient resistive shielding for mushroom-style device geometries cell can be optimized by finding the cell geometry. Typically, the cell geometry is determined by three significant factors: the metal contact diameter φ, the heater length L_h and the chalcogenide thickness L_c, as shown in Figure 4.3(a). By maintaining the same value of readout resistance, L_h is increased when L_c is decreased, as shown in Figure 4.3(b). Here, the temperature profile is determined in the phase-change layer, and the hot-spot position shifts between the chalcogenide and the heater. However, it should be noted that we cannot allow L_c and L_h to take on arbitrary values just so as to reduce the programming current. Both manufacturing limitations and the changes in the L_c and L_h, have

a significant effect on the resistance of the PCM cell, shown in Figure 4.3(b). Thus, the cell geometry optimization is considered here in this study-based on main concepts of cell design reported in [120], regarding the effect of cell geometry and especially the size and position of the heater-ground contact to achieve the hot-spot close to the heater/phase change layer interface.

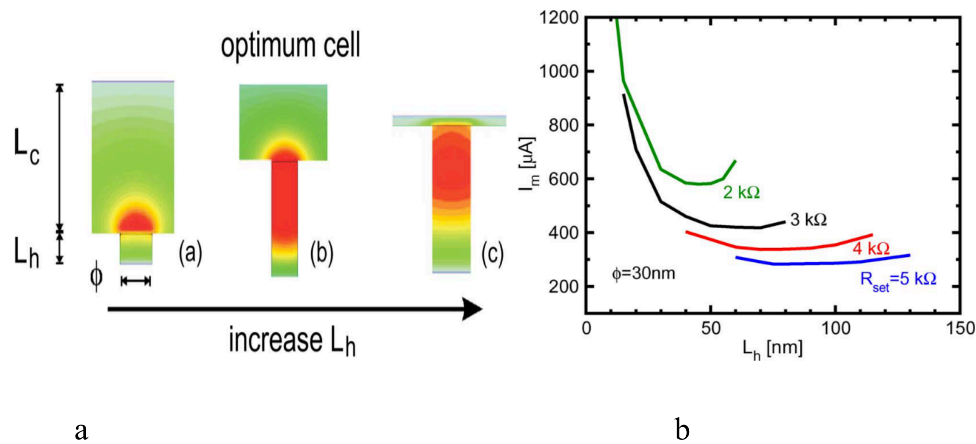


Figure. 4.3(a) Simulated temperature profile in mushroom-type PCM cells with different L_c and L_h sizes, subjected to different melting currents, (b) minimum melting current as a function of heater length L_h with different values of SET resistance, R_{SET}. Both reprinted from [120].

4.2.2 Proposed Logic Cell Structure

Following the general proposed three-terminal phase-change logic device concept indicated in Figure 4.2 and the understanding of the requirement for achieving high resistive switching performance-based device design, the device structure in Figure 4.4 is proposed as a practicable three-terminal PCM device having vertical architecture and foundation for optimization studies. By considering cell layer dimensions in previous studies [119][120], the proposed cell layer dimensions have typically been chosen and optimized as a good starting point for our scaling study. In this structure, both low heat loss in the phase-change layer and reduced leakage current between the ground terminal and the others are taken into account by

connecting the side ground terminal indirectly to the phase-change material (GST material of thickness 100nm) via a metallic heater contact of titanium nitride (TiN) with thickness of 10nm. By using a 10 nm heater thickness, the maximum temperature of the GST is reduced from 1719 K to 1263 K shrinking hot-spot to be far from the cold-metal top and bottom electrodes with a constant current of 100 μA, as reported in [121]. Furthermore, the use of an independent heater also helped to keep the resistive shielding in the active phase-change region in contact with the heater with a cap (mushroom) shape, as discussed by Ielmini et al. [120]. The other two (top and bottom) terminals are directly connected to the 100 nm GST material in the proposed vertical design via metal contacts of a tungsten (W). The GST material and both contacts, top and bottom, are set up with thicknesses of 100nm, 50 nm and 150 nm respectively, regarding the general concepts of the three-terminal phase-change logic device, as discussed in section 4.1. The tungsten (W) was chosen because it has a higher electrical and thermal conductivities compared to other metals, such as aluminium and titanium, which lead for quickly removing the thermal energy from the other untransformed regions of the GST layer and allows for escaping through high thermal conductivity insulating layers/substrate. The insulating layers are typically of silicon dioxide (SiO_2), whereas a thermal layer of a titanium nitride (TiN) is used under the bottom contact to keep the GST layer thermally insulated and control heat dissipation to the Silicon (Si) substrate (not shown in Figure 4.4). The SiO_2 surrounds all boundaries of the GST material except the boundaries with the metal contacts to electrically and thermally insulate the GST material, and reduce the leakage current between the heater and the other metal contacts. The electro-thermal material parameters used for the proposed vertical three-terminal PCM device are listed in Table 4.1, and the phase change modelling parameters are equivalent to those presented in [97][98].

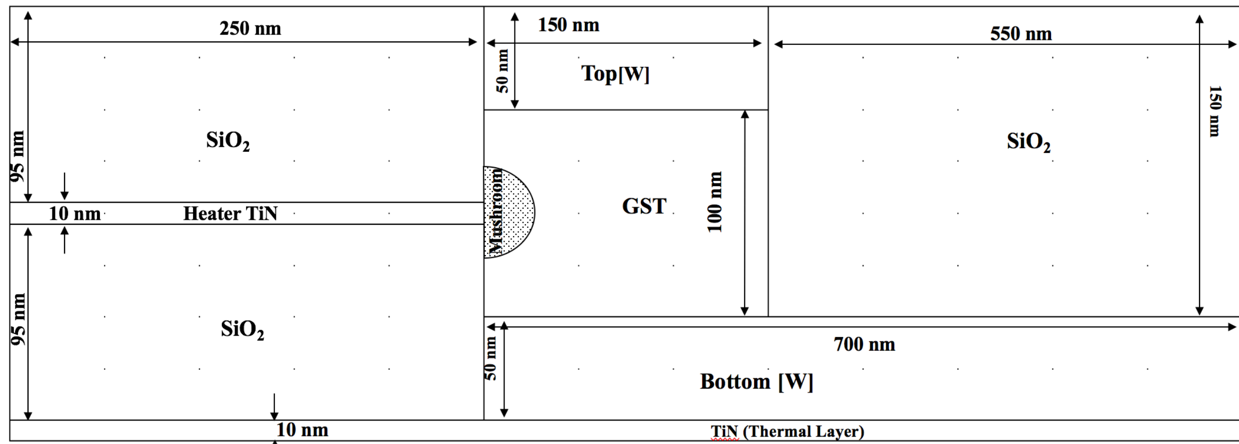


Figure. 4.4 Schematic diagram showing the modelling of the three-terminal vertical phase-change memory element.

Table 4.1 The physical parameters of various materials formed the PC cell [97] [98].

Parameters	GST Amor./Cryst.	W	TiN thermal & Heater	SiO_2
σ $[\Omega^{-1}\ m^{-1}]$	Equ.3.3 / 2770	18×10^{6} [a]	1×10^{5}	1.4
K $[W\ m^{-1}\ k^{-1}]$	0.2 / 0.5	175 [a]	0.44	1×10^{-14}
C $(J\ kg^{-1}\ K^{-1})$	202	132	784	1330

[a] see [122]

4.3 Numerical Implementation

The phase-change modelling is mainly based on the direct interaction between the coupled electro-thermal model and the phase-change model. So, the modelling approach consists of combining the three sub-models, as described in proceeding chapter; i.e. an electrical model

(based on the Laplace equation), a thermal model (based on the heat-transfer equation), and a phase change model (based on the classical nucleation and growth approach). The electrical and thermal models are numerically implemented using the finite-element (FE) method which is provided by the solver in (COMSOL^{TM}) that solves the Laplace and heat-transfer equations simultaneously. The nucleation and growth algorithm code for the crystallization model (entirely written in Matlab) is interfaced together with the electro-thermal model (entirely written in Comsol) using the Comsol with Matlab interface. Thus, the next sections give a complete description for the cognitive strategies of the numerical calculations for the phase-change switching processes using the Comsol with Matlab interface. Then, this model will be used to show the switching manners in the three-terminal phase-change cells.

4.3.1 Multiphysics Finite Element Implementation

To provide a comprehensive understanding of the phase switching mechanism in the GST layer of the vertical three-terminal PCM device for reconfigurable logic operations, both electrical and thermal phenomena must be included in the finite element modelling. As previously indicated, the electrical and thermal models are implemented in Comsol Multiphysics and solved by the finite element method (FEM). Firstly, two-dimensional geometry of the proposed vertical cell structure, as explained in 4.2.2, along with the cell layer dimensions are implemented in Comsol's user interface. The electrical model (Laplace's equation for the electric potential, section 3.2.1) and the thermal model (the heat transfer equation, section 3.2.2) are implemented in Comsol's user interface through specifying the values of the coefficients of their partial differential equations which are related to the physical properties of the different types of materials within the device structure.

Secondly, electrically and thermally insulated boundary conditions were specified for the external device boundaries, except for those in contact with the cell metal terminals which are set as electrical circuit terminals, as will discuss later in next section. Moreover, the lower

boundary of the TiN thermal layer was set to room temperature (300 K) to model the high thermal conductivity (heat sink) Silicon (Si) substrate layer (with thickness much greater than the other layers in the device structure). The overall implementation space was terminated with thermally and electrically insulated boundaries which were positioned at distances sufficiently far from the device structure so as not to affect the simulation solutions in the active domains. The inner boundaries within the device structure were automatically satisfied continuity of potentials, temperatures and fluxes.

The geometry layers are then described in different mesh sizes of triangular elements [123]. To trade-off between computational complexity and available computer resources, a fine triangular mesh with a maximum dimension of 2.5 nm was used for the GST layer, as a comparable dimension to the critical size of the nuclei [2]. The other layers are also used mesh elements with dimensions of [2.5-125] nm for distribution of different sized clusters, as shown in Figure 4.5. The distribution of the different sized clusters is important to achieve the interaction between the fine (critical cluster size) and coarse clusters for crystallization progresses [2]. Thus, the use fine mesh elements with a dimension of (2.5 nm) provides an accurate solution of both the electrical and thermal calculations and integration with Matlab for the correct and self-consistent solution of the nucleation and growth model.

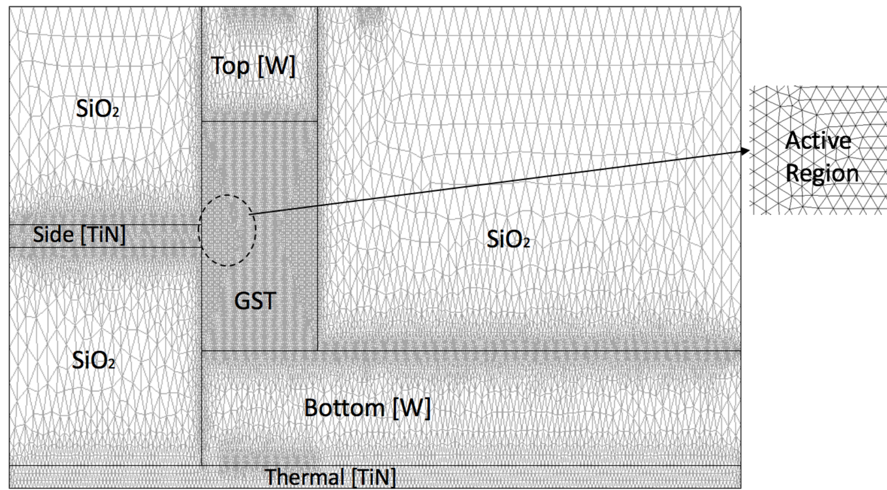


Figure 4.5 Schematic of the 3T-PCM cell used for the device simulations. The phase change region contains smaller triangular elements since this is the layer where phase transformations occur.

4.3.2 SPICE Circuit Implementation

As discussed in the previous section, the vertical geometry of the proposed three-terminal PCM device is created in the COMSOL graphical user interface (GUI) and the layer material parameters for the device domains, such as the electrical and thermal conductivities, then the boundary conditions are also specified. The following step considers of the electrical pulse applications using the SPICE Circuit Editor within COMSOL. This step is essential for applying various signal shapes (e.g. triangular and trapezoidal) with varying amplitudes and durations during device simulations of writing, erasing and reading processes, as will be discussed later with more details in the next chapter.

The electrical SPICE modelling capability within Comsol Multiphysics is used to mimic physical external circuit components such as voltage/current sources, resistors and capacitors to connect to specified ports in the finite element, physics-based structure within the modelling space [98]. Figure 4.6 shows an electrical circuit schematic of a SPICE model implementation for a general three-terminal phase-change device model in finite elements. The electrical test

circuit was implemented by the SPICE model to apply different voltage conditions via the electrical ports Pt, Ps and G for the three terminals top, bottom and side respectively. V1 and V2 were used to apply two simultaneous voltage applications of different logic-voltage patterns via an external series resistance (R), typically with a range (1-10 kΩ) as will be discussed later in chapter 6. The integration between the electrical circuit elements and physics-based model allowed the computation of measured quantities such as currents, voltages and resistances through and across terminals much more easily than using microscopic quantities such current densities and electrical conductivities. Consequently, by including the SPICE model with the physics-based models (electrical, thermal and phase-change), the model can successfully mimic the physical behaviour and study the electrical and thermal performances of complete vertical three-terminal PCM cell, in Figure 4.4, under practical operating conditions.

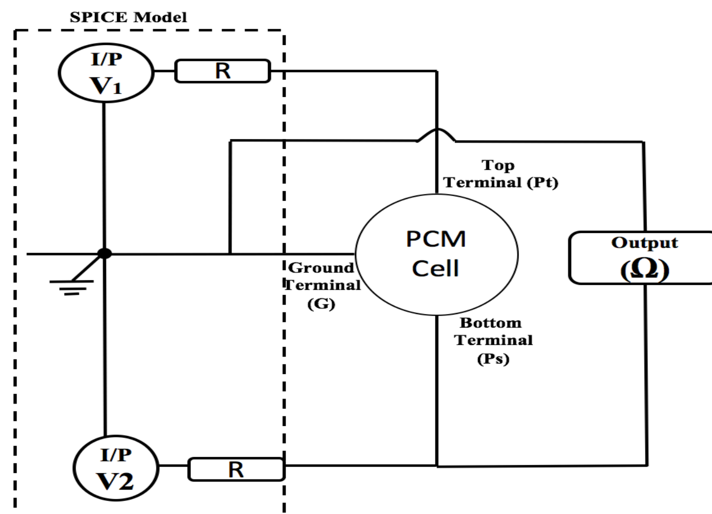


Figure 4.6 Schematic of the 3T-PCM device details, SPICE model with the PCM cell.

To determine the appropriate SPICE model parameters (such as required voltage levels, pulse duration, series resistance values) with a methodology of producing realistic write, erase and read simulations of logic device behaviour (electrical, thermal and phase change), the following considerations must be taken into account:

- The resistance of the device is normally low in the RESET (crystalline) starting state of several kilo ohms, and as high as several Mega ohms when the material in the SET (amorphous resistive shield) state. Hence, the circuit model must be configured to enable the simulations to recognize these two very different states accurately with a series resistance of value no more than the value of the lower level of the device resistance, i.e. to produce no effect on the programming processes.
- The shorter pulses are applied in the SET process, which are usually several 10 ns in duration, so the time step in the simulation should be in the nanosecond range to be able to sufficiently sample the sharp rise and fall edges of the melting and quenching processes.
- The longer pulses are applied in the RESET process to re-crystallize the amorphous programming material returning back to the crystalline state, so the pulse amplitudes and durations should be appropriate for the crystallization processes.

A simulation strategy of a feasible SPICE model for the vertical three-terminal PCM device is proposed according to the above considerations. Various voltage differences are applied across different pairs of the vertical three-terminal PCM device by using the SPICE model voltage to perform the write, read and erase processes and determine the optimum voltage conditions for these processes in the next chapter.

4.3.3 Phase-Change Model Implementation

The theoretical background of the phase-change model is discussed previously in chapter 3 to show that the classical nucleation and growth model is one the most advanced and physically-realistic modelling approaches available today for the simulation of phase-change devices, and therefore is the model of choice for the work in this thesis. This section presents

the implementation of this model for nucleation and growth simulations of the vertical three-terminal PCM device, regarding the proposed device structure in Figure 4.4, using Comsol Multiphysics with Matlab interface. Briefly, the mesh generated by Comsol for the device structure, and in particular for the phase-change layer is exported to Matlab providing an auxiliary mesh with the same coordinates as the electro-thermal model, but now used for the phase transition model in Matlab. Moreover, the calculated temperature distribution at each time step from the electro-thermal model in Comsol is also exported to Matlab to compute the corresponding, thermally activated crystalline volume fraction, as shown in Figure 4.7.

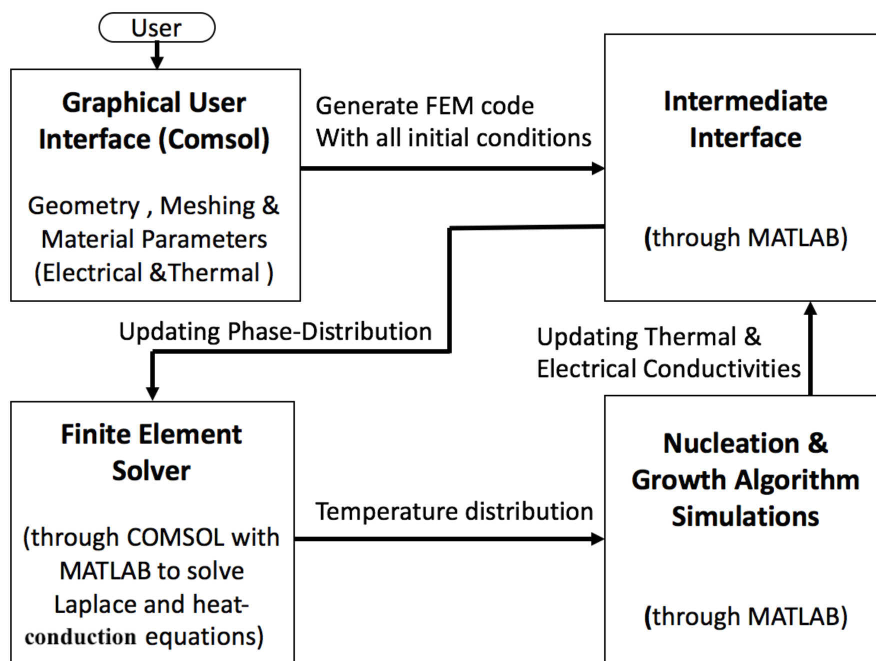


Figure. 4.7 Block diagram showing fully description of implementation process Steps for simulations the fully coupled Multiphysics Nucleation and Growth approach of the vertical three-terminal phase-change device modelling using Comsol with Matlab interface.

The Multiphysics Comsol finite-element model initially produces the temperature distribution within the modelled structure from Joule heating due to the application of terminal voltages, using existing (starting phase) phase-change material properties. Due to the

complexity of modelling the phase transition process, the classical nucleation and growth model is implemented in Matlab using an auxiliary mesh for the phase-change layer only. The phase transition model in Matlab is programmed to link with Comsol by acquiring the generated temperature distribution at a given time step as input, which is then used to calculate (using classical nucleation and growth theory) the resulting crystalline volume fraction within the phase-change layer. The crystalline volume fraction calculated in Matlab is then used to update the spatial distribution of the electrical and thermal conductivities in Comsol, leading to an updated temperature distribution at the next time step which is then used as an input into the phase change model in Matlab to update the crystalline fraction. This process is iterated at each time step to progress the electrical, thermal and phase transition models in a self-consistent and stable manner, until the specified simulation time is completed or the temperature in the phase-change layer reaches room temperature.

4.3.3.1 Creating Custom Mesh

Although many studies, such as Wang [124] and Kim et al. [125], described the electrical and thermal distributions for the phase-change simulations at each time step using a Comsol-Matlab interface, the temperature calculations of the GST region were extracted directly from COMSOL grid elements followed by interpolation into a new phase-change grid. The new grid of the phase-change model in Matlab was different from the grid that was used for the finite element model within Comsol. This difference in mesh elements size and shape, often produced an effect on solution results of the phase-change model due to interpolation errors [123]. Thus, to preserve consistency, compatibility and resolution with the finite-element Comsol grid, the same grid elements (triangular lattice) have been used in this work in Matlab instead of the rectangular lattice that was used by Wang [124]. The use of the same mesh in

both platforms also produced much fewer calculations and more accurate results as will be shown in the simulation results in the following chapter.

Consequently, by calculating the temperature distribution of the GST layer within Comsol Multiphysics, the temperatures of the tiles (or mesh elements) are extracted numerically corresponding to the coordinates of the triangular mesh elements that are used for the finite element model within Comsol, i.e. with maximum tile dimension of 2.5 nm, as shown in Figure 4.8. Then, each tile provides local temperature information at each time step that could be used in the phase-change model for nucleation and growth calculations, as will be discussed in the next section.

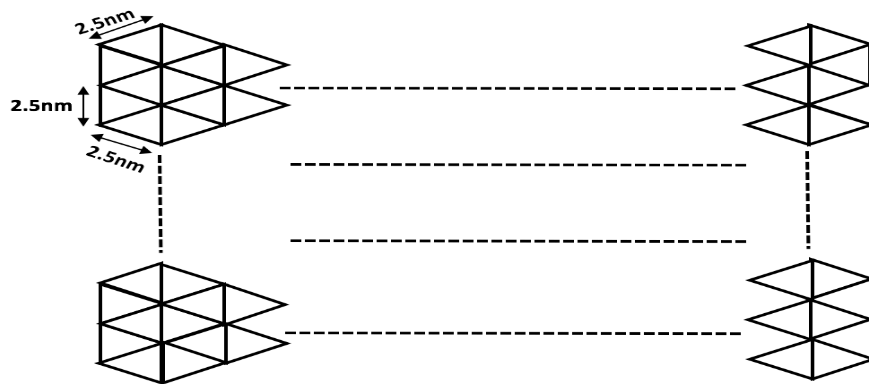


Figure 4.8 Geometry of the GST layer arranged into triangular mesh elements for the nucleation-growth model.

4.3.3.2 Mesh Element Calculations for Nucleation and Growth Model

The phase transformation process of the nucleation and growth model is numerically considered in Matlab through a mathematical reaction mechanism to calculate accurate crystal nucleation and growth rates based on the classical nucleation theory. Numerically, nucleation occurs by either nucleation of the amorphous tiles to the critical size or by subsequent growth of stable crystallites at the boundary of the amorphous region due to temperature effects. At this point, the creation of critical size of the crystal nucleus is considered here by estimating

that the size of the tile (i.e. 2.5 nm) similar to the critical size of nuclei. The temperature effects for growing stable crystallites are taken into account by calculating the temperature dependent nucleation and growth rates, as explained in section 3.2.3.3. As both (nucleation and growth) reactions are dependent on the temperatures resulting from the finite element (FE) solver during the simulation, the probability of either homogeneous or heterogeneous (PI_n) nucleation of one amorphous grid to become a crystalline nucleus during the time interval (dt) is given by [124]:

$$PI_n = \begin{cases} I_n * \Delta V * dt & \text{For homogeneous} \\ I_n * \Delta A * dt & \text{For heterogeneous} \end{cases} \tag{4.1}$$

Otherwise, the grid has a probability of growth via an adjacent crystallized grid during the growth process, which is given by:

$$PV_g = \frac{V_g}{\Delta} * dt \tag{4.2}$$

where, I_n is the steady-state nucleation rate for homogeneous (I_{hom}) or heterogeneous (I_{het}) nucleation, respectively. In (4.1) and (4.2) dt is the time interval or time step during the simulation, and ΔV and ΔA are the volume and surface area of the tile, respectively. V_g and Δ are the crystal growth rate and the average/maximum tile length of the triangular tile respectively. The I_{hom}, I_{het} and V_g are calculated using equations 3.13, 3.18 and 3.19 respectively, to present the thermodynamic terms in the nucleation and growth kinetics. The other kinetic parameters of the thermodynamic process are defined with their values for GST in Table 4.2.

Table 4.2 Numerical values of the kinetics parameters of GST [2]

Symbol	Definition	Value	Unit
v_m	Monomer volume	2.9×10^{-22}	m^{-3}
γ	Interfacial energy	0.1	sec
ΔH	Enthalpy of fusion at melting point	625	sec
E_1	Activation energy for nucleation	1.8	eV
E_2	Activation energy for diffusion of atom	2	eV
Tm	The melting temperature	900	K

The statistical model of nucleation and growth probabilities was used by Peng et. al. [126] to model crystallization process in phase-change storage disks, and their approach was later developed by Kim et. al. [125]. Peng et. al. reported that the probability of crystallization kinetics at a particular point in a spatial location in the medium was subject to a specific threshold temperature, glass transition temperature, to change the phase of the tiles in the PC layer. Whereas, Kim et al. [125] discussed an alternative approach to determine the crystalline probabilities of the GST grids depending on percolation behaviour to involve energy-accumulation effects during the crystallization process based on a finite difference method (FDM). In this work, a more realistic computer model is adopted to describe the nucleation and growth processes of the phase-transition model based on a kinetic approach that was used by Kim et. al. [125]. Therefore, we considered the temporally and spatially resolved kinetics of GST temperature distribution based the electrical field-dependence of the electrical conductivity (using Ielmini's analytical model discussed in chapter 3). Then, the temperature distribution was used to calculate the probabilities of both nucleation and growth reactions. By comparing the simulation results with that experimental data reported previously in refs. [2][3],

as shown in the preceding chapter in Figure 3.3, the maximum probability of the nucleation and growth is associated on where the maximum nucleation and growth rates occur (i.e. at the onset of crystallization). As reported in the literature and shown in Figure 4.9, the crystallization onset occurs at temperature of about 428-453 K. The calculations of the statistical model of the nucleation and growth probabilities are calibrated to provide a more accurate evaluation of crystalline volume fraction by matching the simulation results and experimental observations, as will discuss in section 4.4.

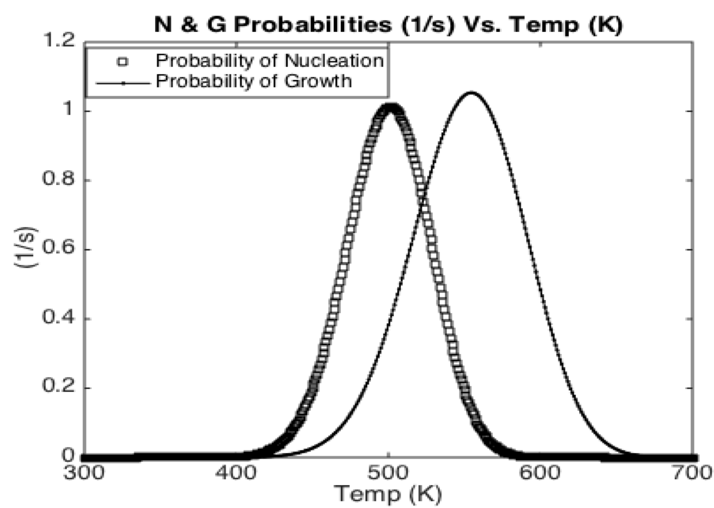


Figure 4.9 The occurrence of the maximum nucleation and growth rates at the onset of crystallization,

4.3.3.3 Crystalline Volume Fraction Computation

The temperature calculations resulting from the multi-physics finite-element calculations in Comsol are then used in Matlab to calculate crystallization probability mesh along with volume fraction of crystalline material in the vertical three-terminal PCM device. An adaptive approach, based on using an energy-accumulation process along with percolation effect by Kim et al. [125], is used to calculate the crystallization probability grids and then evaluate the crystalline volume fraction of only the GST layer in the vertical device. At each time step (i.e. from [t−1]→ [t]) and based on the assumptions of the nucleation and growth theory, the

temperature dependent crystallization probability (Pc) of a simulation grid is updated as follows: the considered tile has a probability of nucleation PI_n (i.e. homogeneous in the GST bulk or heterogeneous at the surface) if none of the neighbouring tiles is in crystalline phase. In contrast, this tile has growth probability PV_g if it is neighboured by a crystalline tile, as shown in Figure 4.10. Thus, when the amorphous material is still heating up, the nucleation and growth reactions can happen simultaneously, and then the probabilities of both reactions are accumulated subsequently, resulting in crystallization probability, which can be calculated by the following formula:

$$P_C(t) = P_c(t\text{-}1) + \left[PI_n(t) + PV_g(t)\right][1 - P_C(t\text{-}1)] \tag{4.3}$$

Each tile in the amorphous region has a desired heat energy to crystallize. Equation (4.3) can be used to determine the crystallization probability of the tile by considering pre-percolation behaviour. The probability of the crystalline percolation involves the heat energy-accumulation. In other words, the heat energy that results from joule-heating effect is accumulated and then crystal clusters grow under effective voltage applications. When enough energy has been accumulated to reach the percolation threshold, the cell resistance changes abruptly due to the formation of the percolated crystalline phases (conductive filaments) in the amorphous region.

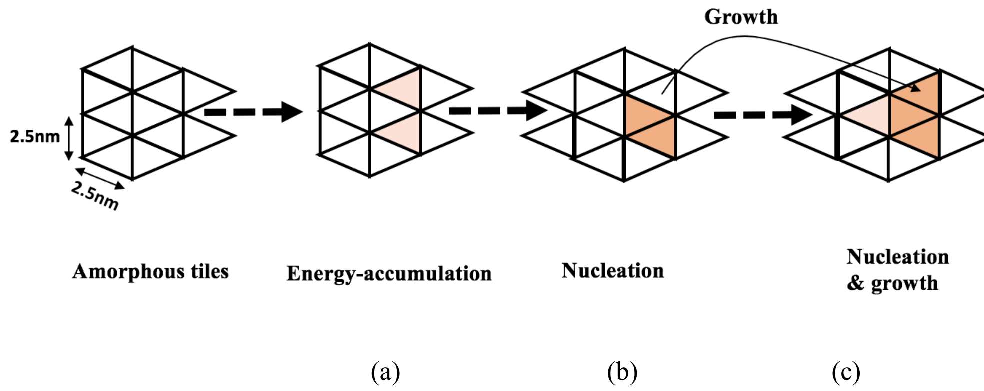


Figure 4.10 Switching events in the nucleation and growth approach: (a) Energy- accumulation, (b) Nucleation, (c) Growth.

The conductive crystalline filaments in a crystallisation simulation are created in an amorphous starting region between the active and ground terminals driven by the temperature distribution at each tile. Initially and to simulate a realistic phase-change material behaviour, random nucleation events with some tiles at the critical size and thrown at random locations inside the amorphous region. By taking in to account non-isothermal transformations, the crystallization dynamics is expected to display a random nature of nucleation and isotropic growth during crystallisation in the amorphous material [127][6]. This is important to simulate the physical material properties, due to variations in fabrication processes and the vacancies in GST material, exhibit some random crystalline formations in the metastable crystalline phase during the nucleation behaviours in a real system [85]. To introduce this randomness of the initial state of the amorphous material, $P_C(t)$ is calculated by comparing the calculations of both the nucleation and growth probabilities (PI_n + PV_g) in equation (4.3) with a random number. The random number is between 0 and 1, is assigned to each tile to determine the updating tile phase (crystallization event) at each time step. If the calculated value of (PI_n + PV_g) is higher than the corresponding random number given to the tile, the tile is in a crystalline phase. Otherwise, the tile is in an amorphous phase, as shown in Fig 4.10. Thus, the

crystallization probability is subsequently calculated for an untransformed tile, and then the distribution of crystalline-amorphous tiles in the PC layer can be determined by calculating the volume fraction of the crystalline phase in the GST layer. Where, the volume fraction of the crystalline material (χ), of the GST layer in the vertical three-terminal PCM device, is computed by:

$$\mathcal{X} = \frac{1}{N} \sum_{i=1}^{N} P_c(i) \quad (4.4)$$

where $0 \leq \chi \leq 1$ and N is the 2-dimensional grid size (i.e. the total number of tiles in the PC layer).

4.4 Validation of Crystallization Model

To validate the crystallization model developed in this research project , the evaluation of the volume fraction of the crystalline material (χ), discussed in previous section, is used here for comparison with typical published experimental measurements that was reported previously in refs. [2][3] for GST, where the volume fraction of the crystalline material describes the relationship between the conductive filaments and the nucleation events. The calculations of the crystalline volume fraction are carried out on the same dimensions, physical parameters and mesh size, as discussed in previous sections, of the GST layer of the vertical three-terminal PCM device during which the temperature increases with a constant rate. Figure 4.11 shows the calculated crystalline volume fraction for an initially amorphous material heated from room temperature using ramped annealing at a slow heating rate of 0.05 K/s. The onset of the rising part of the crystallization curve can be observed when the crystalline fraction exceeds a value of 15% [90] at temperature of 428 K, as reported in refs. [2][3]. A good agreement between simulation and experimental measurements in the literature is demonstrated in Figure 4.11, indicating the ability of this technical approach in predicting real

material behaviour in a vertical three-terminal PCM device. Thus, the calculations of the crystalline volume fraction are used to update the electrical and thermal conductivities of the GST layer, discussed in chapter 3, during the phase switching processes. The new value of the crystalline volume fraction is exported to Comsol to carry out a new temperature distribution at each simulation time step under various voltage applications for producing device resistance, as will be discussed in detail in the following chapters.

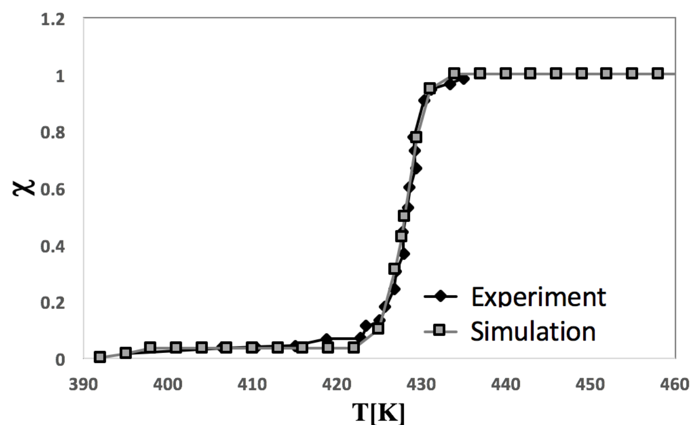


Figure 4.11 The evolution of crystalline fraction of GST as a function of temperature changes resulted in the simulation and compared with the experimental results that reported in [5][12][16][17]; the experimental data and the simulation results are black and grey marks respectively.

4.5 Chapter Summary

According to above discussions in this chapter, it is essential to develop physically realistic three-terminal (3T) PCM cell modelling taking into account cell structure, geometry layer objects included the physical parameters, electrical and thermal conductivities, of the cell materials. Some other effects are also considered, such as cell terminal positions, electrical pulse applications using SPICE Circuit Editor, mesh creation (element shapes and sizes) and strategy of importing/exporting data-based mesh elements through using COMSOL-MATLAB interface. All these factors are highlighted to understand the fundamental physics of the phase

change processes in a 3T device, and to design and optimize future phase change memory devices. For enabling the efficient formation of amorphous domes during the SET process in a crystalline material, it was found that it is necessary to insert a heater contact diameter of 10 nm or less for improving the thermal confinement of the cell and reducing heat loss via the ground. A detailed review of a standard and a widely proposed 3T PCM cell structure was presented to provide some confidence in producing a most practicable cell structure for the vertical 3T PCM device design. Using the electrical circuit implementation of SPICE model, which is numerically available within COMSOL^{TM} Multiphysics software, it was found that it could connect physical external circuit components such as voltage/current sources, resistors and capacitors to specified ports in the finite element. On the other hand, numerical Implementation Strategies of the classical nucleation and growth approach using COMSOL with MATLAB interface were presented, such as 3T cell creation in COMSOL draw mode tools, mesh elements (shapes and sizes) and a series of implementation steps between COMSOL and MATLAB for creating crystallization events. It could evaluate the calculations of the crystalline volume fraction by carrying out the calculations of both nucleation and growth probabilities in MATLAB. Finally, a validation of using the crystallization model for electrical applications, introduceing realistically numerical calculations during reversible transitions in the GST material of the 3T device, was observed by comparing between the results of numerical calculations of the crystalline volume fraction with the experimental results in refs. [2][3].

In particular, it is clearly evident that the proper design of the heater (position and thickness) within the proposed 3T PCM cell provides a key aspect to create the mushroom shaped amorphous region with full coverage of the ground electrode for producing high resistance levels, as will be discussed in the following chapter.

CHAPTER 5: Parametric Simulations of Voltage Conditions in the 3T Vertical Logic Device

In the preceding chapter, a full description of the numerical implementation steps of both the electro-thermal model, through (a finite-element method in Comsol) and the nucleation and growth model (in Matlab), was presented to produce a physically realistic three-terminal (3T) phase-change memory (PCM) for simulation purposes. The implementation included important factors such as cell structure, materials properties and dimensions of the cell layer and terminals positions. Furthermore, the external circuit components modelled using the SPICE Circuit Editor and mesh creation (element shapes and sizes) were also considered within the strategy for implementing the physically realistic nucleation-growth model using the Comsol-Matlab interface. In this chapter, the physically realistic finite-element model is used to carry out parametric studies to determine the optimum operating voltage conditions of 3T phase-change logic devices, and study the dynamics of device programming and resistive switching behaviour of practicable logic devices. The parametric study simulations focus on some reliability aspects of 3T PCM device operation such as (1) The programming cycle strategies of 3T PCM devices based on temperature-voltage characteristics and thermal confinement areas, (2) resistance states-based voltage conditions, (3) the amorphization (Set) and crystallization (Reset) kinetics for both the writing and erasing processes respectively, and (4) the resistance window for different logic operations.

5.1 Methodology

As discussed in previous chapters, the information in PCM cells is stored in the local atomic mesh structure of the phase-change material, which is confined in the device by three electrical contacts. It is worth recalling that the 'active' region of the cell, which is in contact directly

with the third (side) terminal (see Figure 4.4) plays a pivotal role as the active region during the programming and erase processes. Thus, the active region of the cell is used for the work in this thesis for switching between the high-resistance amorphous (or Set) state and the low-resistance crystalline (or Reset) state, by appropriate electrical excitations (voltage pulses). The voltages are applied across the cell terminals, using the SPICE Circuit Editor, and then the temperature-voltage characteristics are calculated by the finite-element solver under the Comsol model. In general, higher amplitude and short duration Set pulses are required to place the fully crystalline initial material state within the logic-memory cell into a partially amorphous region (within the active region), whereas a more moderate and longer duration Reset pulses are needed to switch the state of the active region back to the originally crystalline state. The state of the cell (1 or 0) is read out by sensing the resistance using a low voltage read pulse that does not disturb the stored state.

The amorphous state produced during the Set process in the active region works as a (mushroom shaped) cover across the side (heater) contact in order to control current flow between the ground and the other (top and bottom) contacts. As indicated in Chapter 4, the material of the heater was designed to be TiN, which has a higher electrical conductivity and lower thermal conductivity compared to usual metal electrode materials. This helps to reduce heat loss through the side (ground) metal contact, and at the same time, the heater works as an electrical contact to produce a confined amorphous region in contact with the heater-ground contact for programming the logic device. Hence the name 'mushroom cell' is used here (see the shaded regions shown previously in Figure 4.3) to discuss the phase switching states in the active region during the Set processes.

The use of the heater pillar-type contact in the mushroom cell is attractive since it helps to limit the programming volume of the phase change material that has to be amorphized and re-cystallized, thus also limiting the switching current/voltage to provide low power operation

needed for the programming. Since during the amorphization (Set) process the switching volume has to be heated up to and above the melting temperature (~620°C (or 900K) for GST) before being rapidly quenched to the amorphous state, it is the Set process that is the most voltage demanding process in the phase switching conditions within the GST material. The reduction of the Set voltages is thus a primary issue of concern in the development of a viable 3T phase-change device, which depends mainly on temperature-voltage characteristics induced in the GST material within the device.

5.2 Programming Strategies of 3T Logic Devices

Before going to investigate and provide a deep insight into the temperature-voltage characteristics induced in the phase-change material in 3T device, an analysis of the voltage/excitation requirement of 3T logic devices during the simulations of write, erase and read processes is necessary. To distinguish between the different logic states, the 3T logic device is required to produce a resistance contrast of typically 100 times between the minimum and maximum resistance states in such GST-based PCM devices [128]. Hence, the write (Set) cycles are performed on the 3T device when the GST material is initially in a fully crystalline phase, which is the minimum resistance, to predict the cell resistance variations and determine the higher resistance conditions for the logic levels ,0 and 1 states. While, the erase (Reset) cycles are performed when the GST material is partially amorphous phase, for predicting the sensible voltage levels that may use to erase the amorphous region. A short-read cycle is followed, each Set or Reset cycle, to obtain the change in the output resistance.

Figure 5.1 shows typical programming cycles that were applied in the numerical Comsol-Matlab model for simulations of the write, erase and read processes. A read operation is performed here after each writing and erasing cycles to monitor and sense the state of the phase-change material during writing/erasure, and then study and calibrate the programming voltages

accordingly. The write or SET operation (crystalline-to-amorphous state) is performed by melting the active PC region around the ground terminal, that is in contact directly with the side heater, through applying simultaneously two effective voltage differences across two different pairs of the 3T device (with respect to the ground terminal) before quenching this region into the amorphous phase. One of the voltage differences is applied between the top/side terminals and another is applied between the bottom/side terminals. In general, various applications of the voltage differences are used here to perform different logic functions, as will be discussed later in the next section. A readout operation is followed each write operation in the simulation to read and predict the stored information in the phase-change layer as a resistance by applying a low voltage, much lower than that in the programming operation, between the bottom and ground terminals. This read voltage should produce a negligible heating to not affect or induce any phase transition in the phase-change material. The erasing (RESET) operation is performed by applying an appropriate voltage difference between the bottom and ground terminals to recrystallize the amorphous hemispherical region and reverting back into the crystalline state. Here also, another readout operation is performed during the simulation to make sure the active phase-change material is erased, and the output resistance is dropped back into the initial crystalline resistance. There are stringent requirements for the terminal voltages amplitudes and pulse widths in 3T logic devices to produce the appropriate temperatures in the phase-change layer and correctly programme the device in the SET, RESET and readout cycles. This is more complicated condition by the fact that two voltages are applied simultaneously across different pairs of the 3T device, with respect to ground. By using different pairs of the three terminals for various voltage applications, an additional parameter is needed to control the shape and size of the amorphous (shield) region around the side ground conductor for producing appropriate device resistances. Furthermore, these voltage conditions strongly depend on the geometry, dimensions and various materials used in the logic device

and are thus specific to the particular device design that was discussed in the preceding chapter. The next section will consider the voltage condition requirements for programming device cycles.

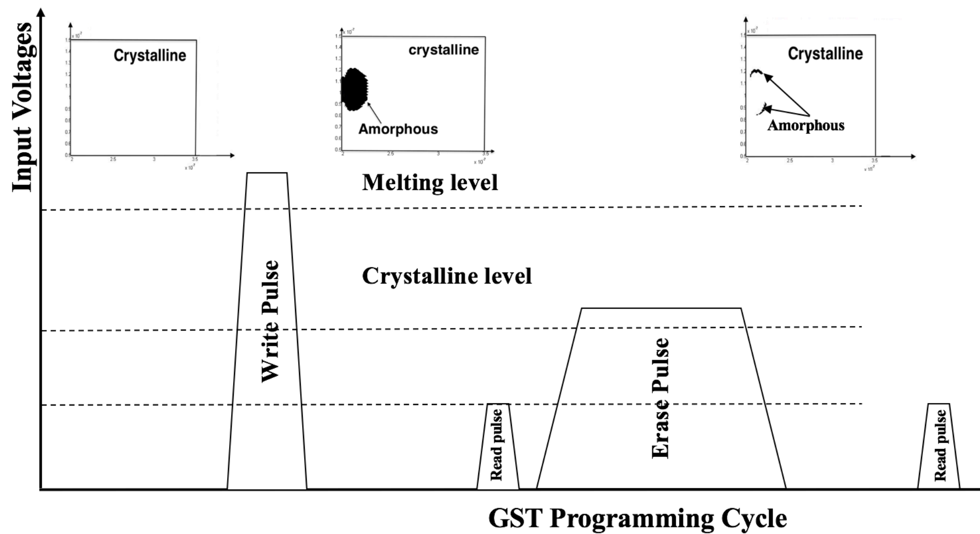


Figure 5.1 The steps of electrically programming cycles for storing and erasing different digital data based three-terminal PC cell.

5.3 Parametric Study of Voltage Applications

The vertical structure of the 3T PCM logic device was proposed in the preceding chapter. The device implementation was discussed through the finite-element model and the external electrical circuit connections to the 3T PCM cell using the SPICE circuit interface within Comsol Multiphysics to carry out the parametric, steady-state simulations of voltage applications. The parametric simulations were carried out through solution of Laplace's equation for the electric potential applications and therefore electric field within the device, which used to provide the heat source for the solution of the steady-state heat conduction equation (discussed in sections 3.2 and 3.3) to determine the temperature distribution throughout the device in general, and in the phase-change layer in particular. Thus, the SPICE editor within COMSOL Multiphysics is not only allowed to apply realistic voltage conditions

to the device ports and external loads, but it also enables direct evaluation of terminal voltages, currents and therefore device resistances without the need to carry out surface and volume integrations within the device to determine electrically these important circuital quantities.

Here, our main focus is on demonstrating extensively the effective voltage levels of the write, erase and read operations for different logic functions using the proposed 3T vertical device along with the designed cell structure and layer materials, as discussed in chapter 4. Two sets of voltage differences with fixed amplitudes are applied in the finite-element parametric simulations: one across the top-ground terminals, V_1, and the other is simultaneously applied across the bottom-side terminals V_2. In this parametric-steady of temperature-voltage simulations, the effective levels of interest are those that produce maximum temperature conditions (temperature events) at certain points of interest in the active phase-change layer, that exceed the melting point (for the SET operation), and the crystallisation temperature (for the RESET operation) during the write and erase processes respectively. These voltages and corresponding temperature events are used to control the size of the hemispherical amorphous region in contact with the side heater and therefore control the output resistance between the device terminals, needed to provide the necessary contrast for the different logic states, as demonstrated in Figure 5.2.

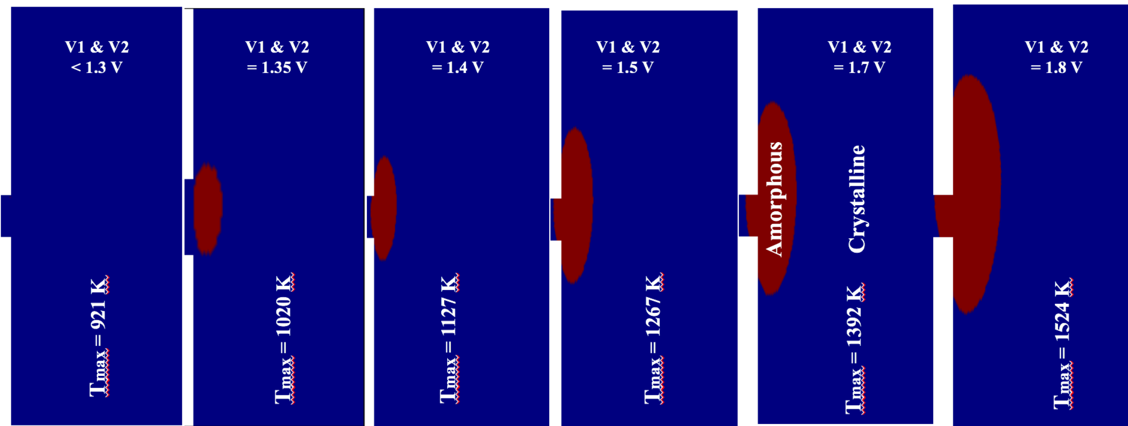


Figure 5.2 The hemispherical amorphous regions and maximum temperature-based steady-state voltage applications in a three-terminal PC device.

In this parametric study, two voltage differences with two different ranges are simultaneously applied to calculate the necessary voltages for the SET, RESET and readout processes corresponding to the temperature events. The top, bottom and ground contacts are labelled, in the proposed SPICE circuit model shown in Figure 5.3, by Pt, Ps and G respectively.

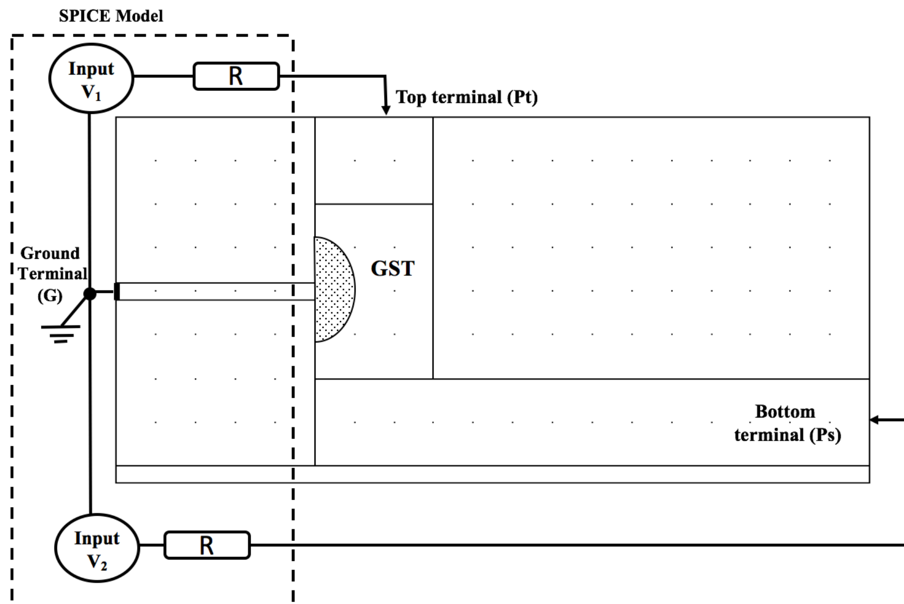


Figure 5.3 Schematic of the 3T-PCM device details, SPICE terminals with the PCM cell contacts.

The two voltage differences, denoted by V_1 and V_2, are applied simultaneously between the pairs of terminals (Pt-G) and (Ps-G) with a range of 1.4-1.8 V, to produce the minimum and maximum temperatures required for the temperature events during programming processes. The voltage levels are chosen to raise the temperature in the phase-change layer to the crystallization temperature or melting point of the temperature events. This step of our investigation was necessary to provide quantitative insight into the corresponding resistance range (maximum and minimum resistances) of the proposed vertical 3T PCM cell based on the temperature distribution within the active region of the phase-change GST layer. Using the steady-state simulations with a range of different voltage applications, the maximum temperatures at nine different locations (indicated in Figure 5.3) near the side heater in the phase-change layer were measured. Figure 5.4 also shows an example of the calculated temperature distribution within the vertical 3T device along with the high temperature concentration near the side heater, as expected, when voltage of 1.7 V was applied via the V1 and V2 terminals.

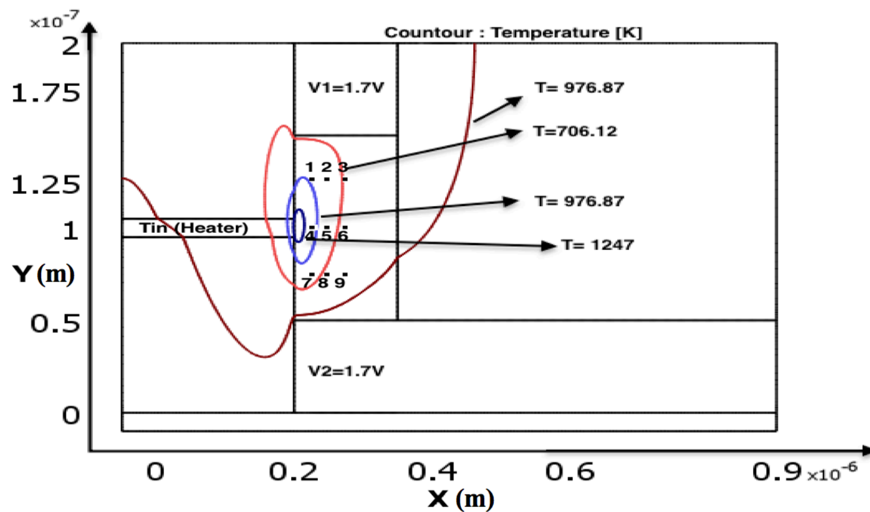


Figure 5.4 An example shows temperature-voltage differences in nine points distributed at different positions in the active PC region when the vertical 3T device under voltage applications of 1.7 V.

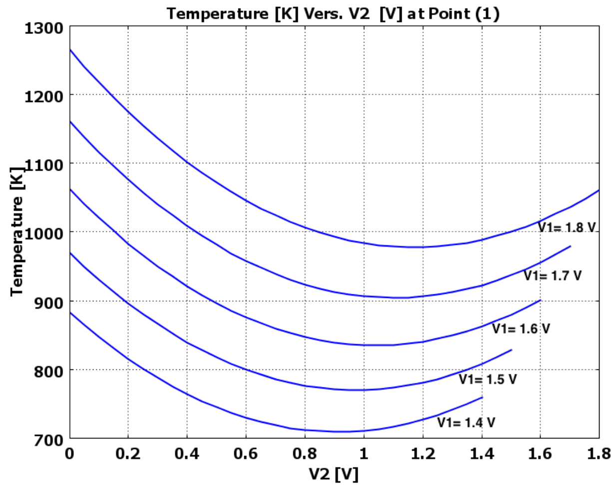
5.4 The SET Voltage Process Simulations

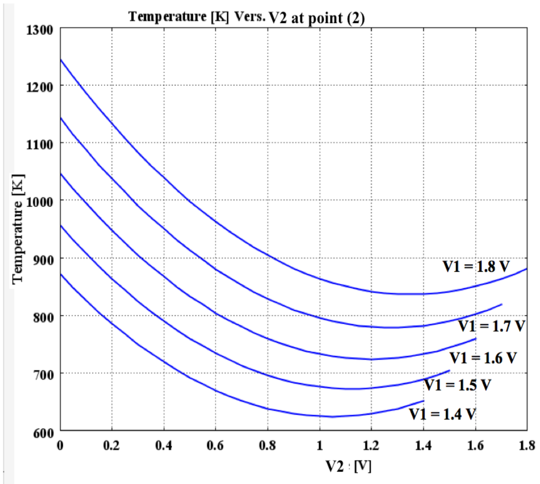
The SET or write operation involves heating the initially crystalline material within the active region of the phase-change layer to the melting point following by fast cooling and quenching to produce the amorphous hemispherical dome. The "mushroom" shaped amorphous dome starts to form in the active region where temperatures are above the melting point (900 K for GST), and then continues expanding to cover the contact area adjacent to the heater and then the final shape of highly resistive shielding is obtained (see figure 5.2). This amorphous (shield) region increases the resistance of the device to preclude current flow between the device terminals such that the output resistance between a shielded contact (the heater) and at least one other active contact (top or bottom) is higher than it would be if a continuous crystalline current pathway was available.

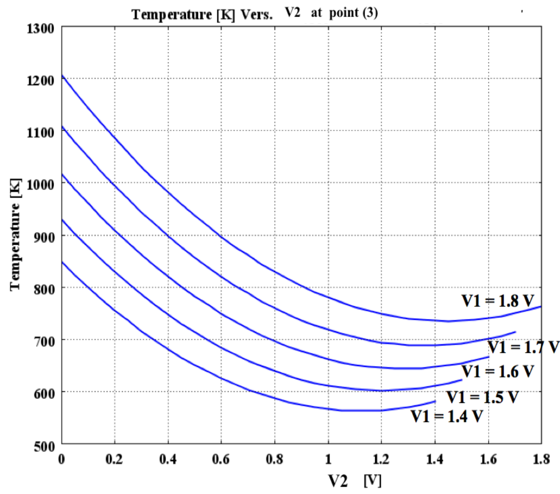
To outline the required characteristics (size and shape) of the amorphous region [69], some explicit assumptions during the SET operations are considered:

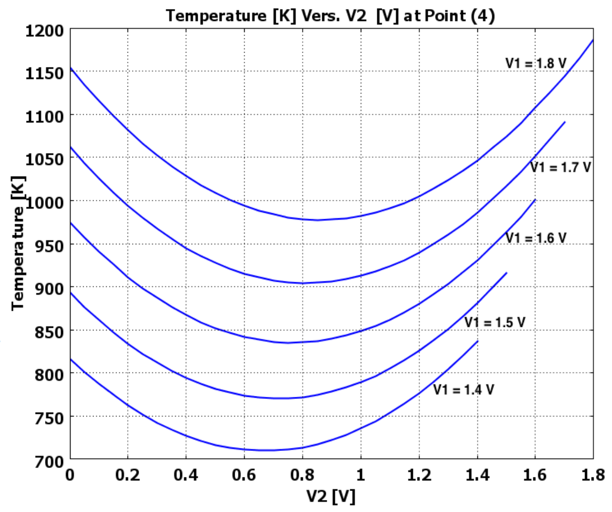
- The amorphous region needs to be in direct contact with the side electrode to provide sufficient coverage of resistive shielding.
- The programmed volume needs to be small enough to enable producing the reduction in cell size and increased integration with an easier erasure under lower voltages.
- The symmetry is preferable in the amorphous region around the side heater to enable the use of equal input terminal voltages for various logic.
- The amorphous region must provide high resistance contrast with stable resistance states between the totally crystalline and partially crystallized phase-change layer for distinction between the binary logic states.

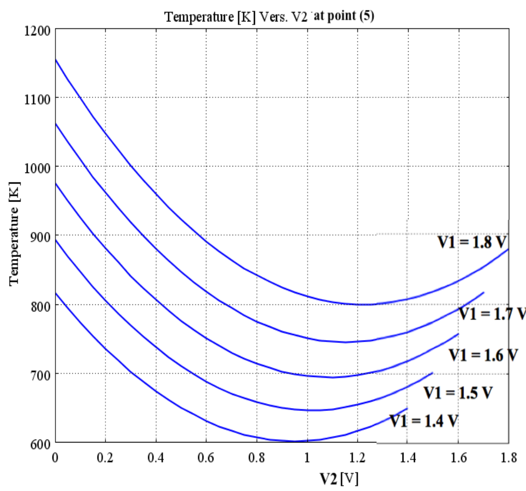
Figure 5.5 illustrates the calculated steady-state temperatures in the nine different positions distributing in the active region near the side heater. Under various voltage applications with an appropriate range of (1.4-1.8) V that can exceed the melting temperature (900 K), it can observe that the higher temperatures over the melting temperature are concentrated in the area nearest to the side heater, as shown in positions 1 and 4 of Figure 5.5. Regarding this assumption of the temperature condition for the SET operations, the voltage applications with a level of 1.7 V or over are probably suitable to use for different logic functions that can provide symmetric amorphous volume covering the heater. Thus, it can produce adequate melting volume, under these voltage levels, for creating an amorphous volume in the active region near the heater.

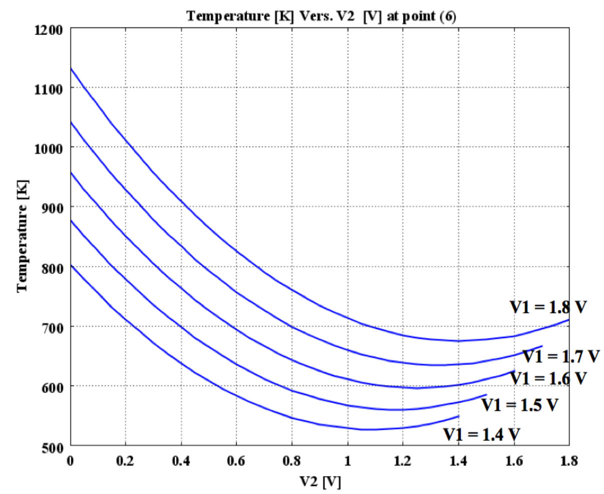

Temperature [K] Vers. V2 [V] at Point (1)
Temperature [K]
V2 [V]
V1= 1.8 V
V1= 1.7 V
V1= 1.6 V
V1= 1.5 V
V1= 1.4 V


Temperature [K] Vers. V2 at point (2)
Temperature [K]
V2 [V]
V1 = 1.8 V
V1 = 1.7 V
V1 = 1.6 V
V1 = 1.5 V
V1 = 1.4 V


Temperature [K] Vers. V2 at point (3)
Temperature [K]
V2 [V]
V1 = 1.8 V
V1 = 1.7 V
V1 = 1.6 V
V1 = 1.5 V
V1 = 1.4 V


Temperature [K] Vers. V2 [V] at Point (4)
Temperature [K]
V2 [V]
V1 = 1.8 V
V1 = 1.7 V
V1 = 1.6 V
V1 = 1.5 V
V1 = 1.4 V


Temperature [K] Vers. V2 at point (5)
Temperature [K]
V2 [V]
V1 = 1.8 V
V1 = 1.7 V
V1 = 1.6 V
V1 = 1.5 V
V1 = 1.4 V


Temperature [K] Vers. V2 [V] at point (6)
Temperature [K]
V2 [V]
V1 = 1.8 V
V1 = 1.7 V
V1 = 1.6 V
V1 = 1.5 V
V1 = 1.4 V

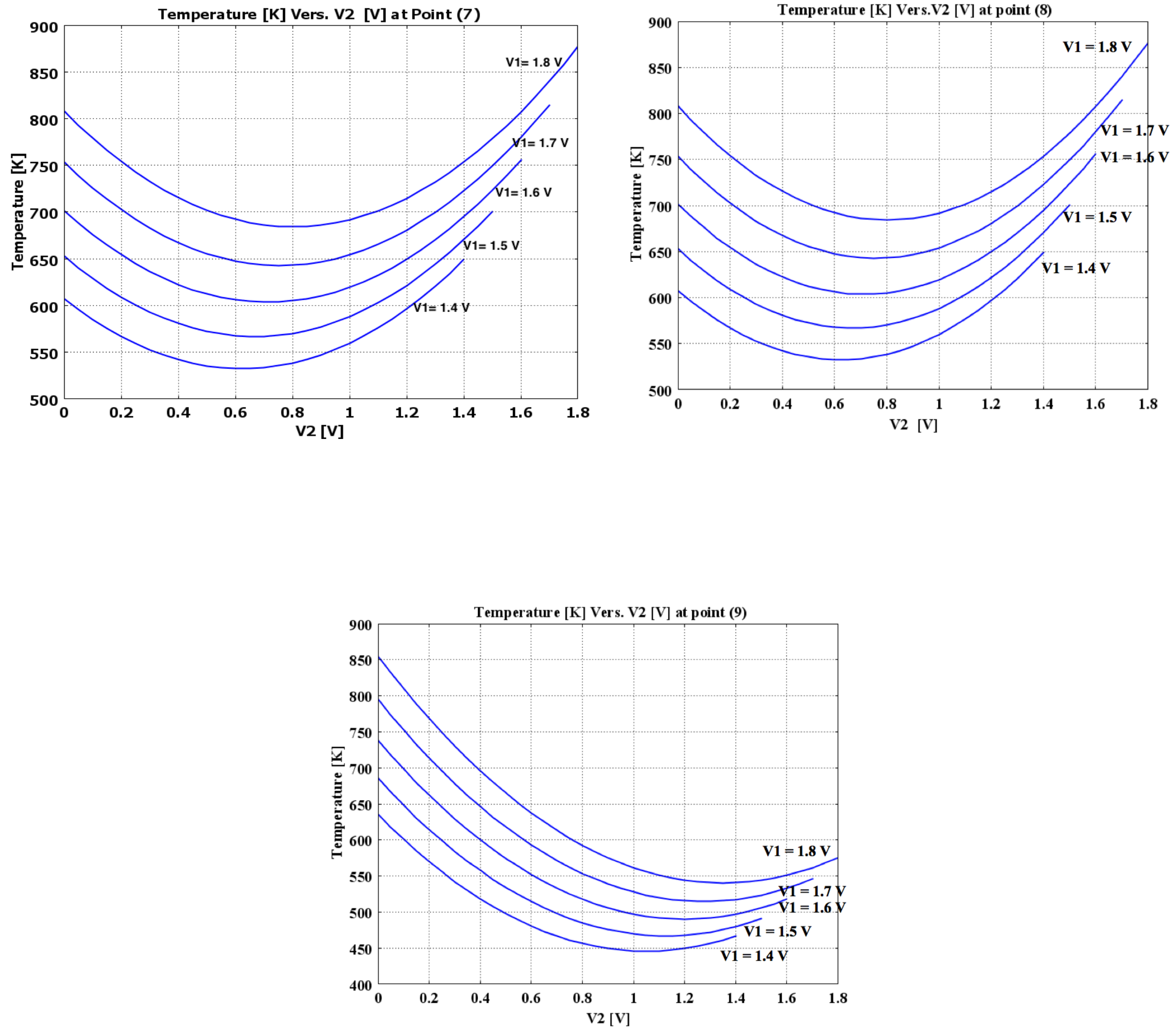


Figure 5.5 Steady state temperature distribution in the nine points (1-9) in PC layer with different positions, under range of voltage applications via the input V1 and V2.

5.5 Resistance Levels Requirements for Logic Programming

While the reasonable voltage differences for programming the vertical 3T PCM cell proposed in chapter 4 are determined by the parametric-steady solution of the temperature-voltage distribution, the output resistance is the direct sensing result of the read operation, as discussed in section 5.2 in this chapter. Thus, the steady-state programming resistances are critically subjected to the voltage conditions for the cell programming processes. The lower steady-resistance state of the vertical 3T PCM device, which is based on the proposed cell structure

design and the materials and dimensions of the cell layer, discussed in preceding chapter, is found when the phase-change GST material within the device was in fully crystalline phase. This lower resistance is obtained from the steady-state solutions with a value of around 4.5KΩ. Whereas, the higher resistance state of the vertical 3T PCM device should be calculated when the phase-change GST material within the device was in fully amorphous phase, which was found with a value of around 3.06 MΩ. Intermediate resistance states are also obtained when the phase-change GST material within the device was in partially crystalline phase.

The difference in cell resistance between the high and low levels during the write (Set) processes, has been considered for the proposed vertical 3T device, and how these levels affect on introducing two distinct logic levels. The resistance window should remain large enough to allow more reliable differentiation on readout between the two logic states in the presence of noise that can be observed from cell-to-cell variability etc. Moreover, the highest Set resistance should not be too significant since its value impacts on the evaluation of the readout current and ultimately determines the minimum time needed to sense the state of the cell within the readout operations, as discussed by Jeong et al in [129]. Therefore, to keep a reasonable electric high/low resistance ratio with a maximum resistance contrast typically approximate 100 times the minimum value of the readout cell resistance, as reported by H. Lo et. al.[128] and Park et. al.[130], the lower and higher steady-state levels of the resistance ratio were chosen with values of 4.5 KΩ and 1.7 MΩ respectively. These low and high resistances were calculated when the phase-change GST material within the device was in fully and partially steady-state crystalline phases respectively, where a stable resistance level with a value of 1.7 MΩ was obtained when the cell was under equally programming voltage applications of 1.8 V via the inputs V1 and V2. With the low and high resistance levels of 4.5 KΩ and 1.7 MΩ respectively, the cell can be programmed to present logic 1 and 0, respectively for distinct data storage of different logic functions, as will be discussed in next chapter. These two steady-state resistance levels with

their programming voltages, as distinct logic states for various patterns of the input voltage applications, are used then to produce applicable logic functions of many logic gates, as will be discussed in transient simulations in the following chapter.

5.6 The RESET Voltage Process Simulations

The RESET or erase process is carried out on a partially crystalline GST material of the vertical 3T phase-change device proposed in this study (see chapter 4) to re-crystallize the amorphized hemispherical region and then erase the stored information, reverting back to the low resistance state. The erasing process can be accomplished through application of the terminal erasing voltages via either V_1 or V_2. This is reasonable since there is a continuous crystalline pathway between the top and bottom metal contacts through the unchanged crystalline region of the original GST layer, which is substantially resulted a low resistance between these two contacts corresponding to the resistance of the crystalline phase [119]. Hence, the reset voltage differences are applied here across the bottom-ground contacts, as shown in figure 5.6, with various amplitudes for the RESET operation lower than the amplitudes of the programming (melting) SET voltages (lower than 1.7 v), as discussed in section 5.2 in this chapter. This is because the re-crystallization temperature with a value of around 428 K needs lower voltage conditions than the voltage conditions required for the melting temperature (900 K) [2][3]. Thus, the hemispherical amorphous region should be heated to temperatures close to those at which the maximum nucleation rate and/or crystal growth rate occurs at the transition temperature of the re-crystallization, as discussed in preceding chapter. The voltage conditions of the RESET operation are considered to carry out erasing transient simulations of reconfigurable logic in the 3T vertical device structure during re-crystallization process, as will be discussed in the following chapter.

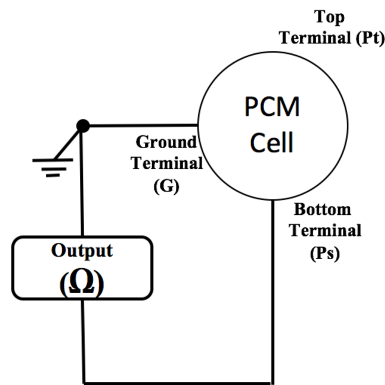


Figure 5.6 The electrical spice circuit for the reset processes.

5.7 Chapter Summary

According to the above discussions in this chapter, it is valuable to achieve a high resistance window for storing logic data in distinct resistance levels and under various voltage application patterns. As explained in programming cycle strategies in section 5.2, it was found that a high resistance ratio up to 100 times of magnitude of the lower resistance (which is the ratio between high and low resistance states) has been produced to provide more substantial programming margin and higher stability of binary data levels. The voltage levels obtained from the temperature-voltage simulations are then used to provide an easier erasure under a symmetric amorphous volume and remove the condition of identifying the inputs V_1 and V_2 when different input patterns of various logic functions are used. Indeed, it was found to be mainly using a parametric study state for studying the temperature-voltage characteristics to investigate the desired voltage differences for high temperature requirements that can achieve a melting volume within the active area of the GST layer (i.e. to evaluate the input voltages for sufficient heating in the GST layer to melt and then amorphize the material during the write processes). Then, the resistances-based temperature voltage characteristics, which were obtained from the steady state simulations as demonstrated in section 5.5, are then obtained to determine high

device resistances based on a particular volume of the resistive shielding (amorphous region). Thus, the steady-state lower and higher resistance levels were determined by the voltage levels of the terminal input SET applications that then govern the allowable erasing (RESET) voltages for reverting back the high resistance states of the amorphous regions to the low resistance state.

In particular, it was highlighted that the steps of steady-state simulations of the voltage levels across the inputs were necessary to determine and realize a reliable 3T PCM device with proper programming process for practical transient logic functionalities, as will be deeply explained in following chapter.

CHAPTER 6: Dynamic Simulations of Logic Functionality in 3T Reconfigurable Logic Devices

In the previous chapter, steady-state parametric simulations were carried out to determine the optimum terminal voltage conditions that yield the appropriate temperatures for writing, erasure and readout in the active phase-change layer in 3T logic devices. Next, these voltage conditions were used to provide the necessary resistance contrast of the 3T vertical device proposed in this work. In this chapter, the resistance-voltage characteristics determined from the parametric simulations are used to carry out transient (dynamic) resistance simulations of reconfigurable logic in the 3T vertical device structure designed in this work. The transient simulations involve optimum programming pulses of both the (SET) and erasing (RESET) processes to produce dynamic resistance simulations for reconfigurable logic functionality in the three-terminal.

There is an intensive body of work for investigating transient switching behaviour of nonvolatile phase-change materials in two-terminal devices for configurable digital systems, such as processors, memory, and field programmable gate arrays (FPGAs). While, the main concepts of involving the transient switching behaviour of the phase-change materials in the 3T devices for producing reconfigurable logic elements, remain a relatively fragmented body of work. Here, a set of possibilities for optimizing the dynamic switching characteristics of the vertical 3T device proposed in this work to suit a variety of logic applications can be discussed. The difference in reading levels of the resistance, which were obtained from one of the active terminal (top or bottom) and the ground (side) terminal, can be utilized as binary data 1 and 0 through the control of the phase switching in the active region from crystalline to amorphous states. Thus, this chapter demonstrates some critical aspects needed of performing a logic

function based reconfigurable 3T PCM device, such as the use of cell resistance (as a state variable) for introducing different logic operations. Consequently, distinct resistance levels are used as a function of the terminal voltages to program the nonvolatile reconfigurable 3T vertical devices and implement Boolean logic gates, such as NAND, NOR and NOT logic gates.

6.1 3T PCM Logic Device: Working Principle

In general, the logic switching process in phase-change memory devices is based on the repeatable switching behaviour of the phase-change chalcogenide active material between the amorphous and crystalline phases as discussed in Chapter 2. Thus, the phase switching is extremely exploited in this work for both logic and memory operations through heating (either partially or fully) the phase-change material to appropriate temperatures to switch between the amorphous and crystalline states. The two phase-change states are characterized to provide the resistance contrast required to distinguish between two logic states. Since the amorphous phase exhibits a high resistance, it is then used in this work to represent the digital logic 0, while the low resistance crystalline phase is used here to represent the digital logic 1.

As explained in the preceding chapter, and from the parametric-study simulations of the resistance-voltage conditions of the designed vertical 3T device, we observed that the high resistances are produced when the active area of the GST material is partially programmed into different amounts of the amorphous (or high resistivity) state. The low device resistances were then observed when this area is in fully crystalline state or a conducting pathway (crystalline continuity) is available through a partial amorphous region between the top or bottom and the ground electrodes. Transient simulations of reconfigurable logic functionality in the 3T vertical device structure designed in this work will be extensively discussed in following sections, regarding steady-state voltage conditions for programming the SET and RESET device

operations. This step is necessary to provide the optimum voltage pulse conditions needed for the determination of a wide reliable resistance contrast (high and low levels) in the 3T vertical device structure proposed in this work. Then, a resistance level threshold will be needed to identify and distinguish between the low resistance (LR) and high resistance (HR) resistance levels for the logic states 1 and 0 respectively.

6.1.1 Logic SET Pulse Simulations

In section 5.4 and from the parametric-study simulations of temperature-voltage solutions, we discussed voltage conditions that yield the appropriate temperatures exceeding the melting temperature (900 K). Under various voltage applications across both the terminals V_1 and V_2 of the proposed vertical 3T device structure (see Figure 5.2) we demonstrated that the voltage applications with a level of 1.7 V or over can produce an adequately amorphous volume covering the active region near the heater for the SET process. Then, distinct resistance levels can produce for different logic functions. So, we now turn our attention to consider appropriate electrical voltage pulses for the logic SET process.

For electrical evaluation of RESET/SET transient behaviour, the proposed 3T vertical cell structure in this study (see Figure 5.2), is embedded into an electrical test bench of SPICE model, as shown in Figure 6.1, along with two electrical pulse sources (for V_1 and V_2) and an external series resistance (R=1 KΩ), which is selected with appropriate level of no more than the lower cell resistance (4.5 KΩ) to produce no effect on the programming processes.

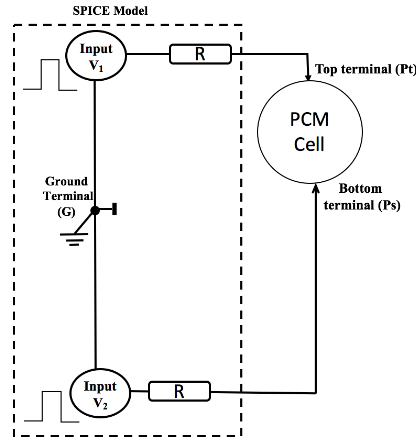


Figure 6.1 The electrical spice circuit for the transient simulations during SET or RESET processes.

In general, higher-amplitude of short-duration SET pulses place the GST material of the proposed 3T vertical cell structure in this study into the amorphous state, whereas more moderate and longer duration RESET pulses switch it back to the crystalline state. The state of the cell (1 or 0) is read out by sensing the resistance using a low voltage read pulse, 0.5 with 70 ns pulse width and 10 ns rise/fall times, that does not disturb the stored resistance state. Thus, we performed several transient simulations with lower pulse amplitudes than 1.7 V and durations (40 to 100 ns) applied across one or both the top bottom terminals, but the temperatures exhibited in the phase-change GST material of the 3T cell were below the melting temperature, especially when the pulses were applied across one terminal input, and thus obtain a final resistance state with lower level. This assures us that more heat energy needs with higher amplitude SET pulses to increase the effectiveness of producing high temperatures exceeding the melting temperature in the GST material. Trapezoidal SET voltage pulses of various amplitudes (1.7 to 2.0) V with 10 ns rise/fall times and 70 ns width, are used then to increase the temperatures in the GST material more than the melting temperature up to 1800 K at the maximum amplitude (2 V) of the input pulses, and produce a final resistance state with a stable level around 2.05 MΩ. Consequently, the SET voltage pulses, with a range of 1.7 V up to 2 V

and fast fall times (10 ns) for exhibiting a rapid cooling rate (see Figure 6.2), are adequate to program the proposed vertical 3T cell structure in this study for different logic functions, as will discuss later in this chapter.

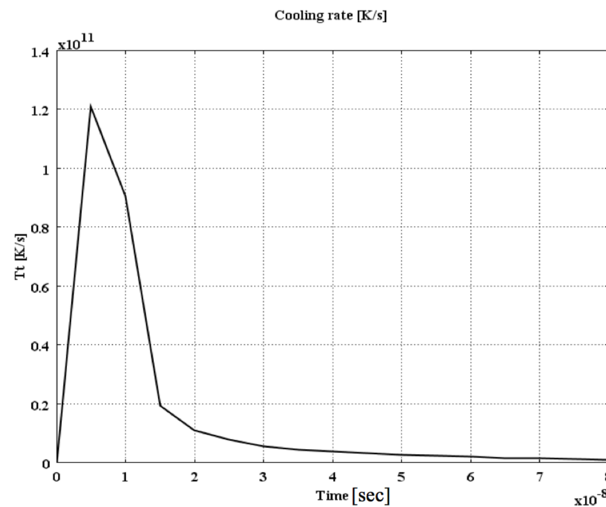


Figure 6.2 The cooling rate with an average value of around 60 K/ns under pulse amplitudes (1.7 to 2.0 V) with 10 ns rise/fall times and 70 ns width for during SET simulation processes.

6.1.2 Logic RESET Pulse Simulations

Logic RESET, or erase process, is most critical process in the development of the logic functionality of the 3T vertical device that proposed in this work. As a part of the programming device operation that discussed in section 5.2, The RESET or erase process is carried out on a partially programmed phase-change GST material within the 3T cell to erase the stored information and revert back to the low resistance state by re-crystallization of the amorphized hemispherical region that formed during the SET process. We have also discussed the RESET mechanism in section 5.6, which is carried out by applying the RESET voltages, with lower amplitudes than the amplitudes of the programming (melting) SET voltages, between the bottom-ground contacts of the designed 3T vertical structure (see Figure 5.5). So, we need now to determine appropriate electrical voltage pulses for the logic RESET process.

The lower programming (melting) amplitudes used for the SET operation is determined by a level of 1.7 V. Thus, trapezoidal RESET voltage pulses of amplitudes (1 to 1.5) V with 50 ns rise/fall times and (200-500) ns width, are used then to heat the partially amorphous region within the GST material and increase the temperatures up to the crystallization temperature, which is around 428 K [2][3]. With a RESET pulse subjected to an amplitude of 1.5 V and width of 500 ns, it was found that full re-crystallization of the amorphous regions was achieved, and the cell resistance decreased for all the SET pulses that subjected to amplitudes in the range (1.7-2) V of the programming cycles. Once the maximum nucleation rate and/or crystal growth rate occurs, which is at the transition temperature of the re-crystallization as discussed in chapter 4, the re-crystallization process happens at the amorphous-crystalline boundary, and then progresses in the amorphous region toward the heater, as shown in Figure 6.3. it can be observed that the re-crystallization of the amorphous phase is initiated by small crystal nuclei that appear in the boundary region, at the presence of a high electric field, then the new crystallites grow until the amorphous bit is fully re-crystallized when the optimum crystallization temperature is achieved. The corresponding temperature distribution during the RESET process has also been shown in Figure 6.4, where it can be seen that the temperature in the amorphous region near the heater has exceeded ~428 K (the temperature required to re-crystallize the amorphous dome and less than the GST melting temperature of ~900 K).

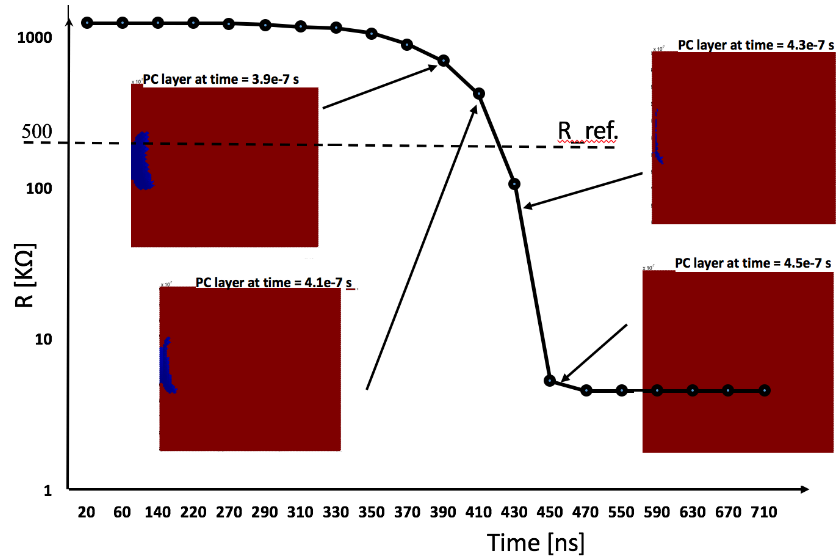


Figure 6.3 Electrical resistance changes and recrystallization progress in the GST layer of the proposed vertical 3T device during the erasing process. The (red) and (blue) regions are the crystalline background and amorphous dome respectively, and the voltage pulse application is set to 1.5 V with 50 ns rise/fall times and 500 ns width.

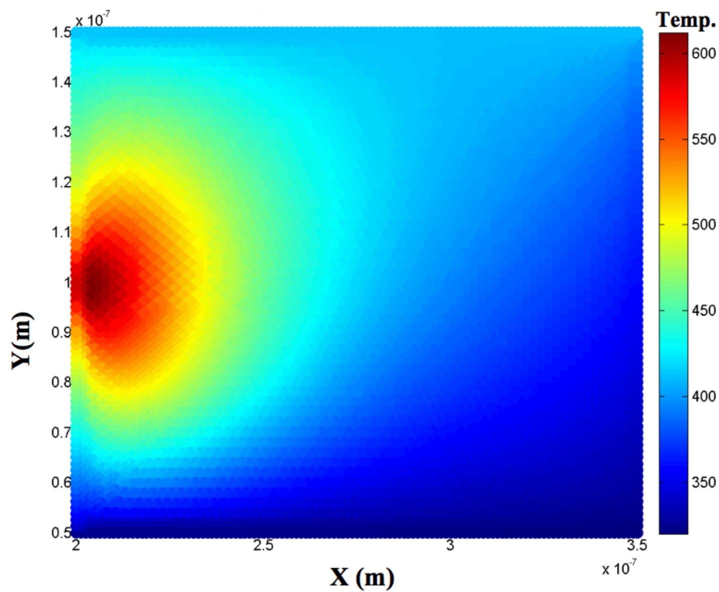


Figure 6.4 Corresponding RESET temperature distribution in the GST material of the proposed 3T device (at 4.5 e-7, i.e. the time of occurrence of maximum temperature) during the RESET process when the voltage pulse application is set to 1.5 V with 50 ns rise/fall times and 500 ns width.

Now we turn our attention to discuss the significant changes in the cell resistance of the proposed vertical 3T device during the erasing process. The erase voltage in this step is determined (1.5 V, with 500 ns pulse width and 50 ns rise/fall times), and then used to increase the electrical conductivity of the programming region. Then, the dynamic resistance of the GST material within the device decreases subsequently back to the crystalline resistance (4.5KΩ as discussed in chapter 5. Hence, the resistive shielding volume, around the ground side terminal, reduces slightly obtaining a reduction in resistance levels of the PC material, as described above in Figure 6.3. A comprehensive numerical simulation based on classical nucleation and growth theory is used, as discussed in the preceding chapter, to reflect a particular model of physical switching dynamics in the phase-change (PC) material, and then the results of electrical resistance switches are observed through the temperature distribution changes. Knowing that the resistance switching mechanism of the PC alloy was carried out every time step in the simulation process by using MATLAB during continuous variations in both electrical and thermal conductivities due to substantial changes in phase switching characteristic. In each time step here during the process, a read operation is performed with a voltage amplitude of 0.5 V to depict the temporal drift of the programmed resistance during the gradual onset of the phase-transitions from the amorphous-to-crystalline phase. A low read voltage (lower than both the SET and RESET pulses) does not disturb the current resistance state, as discussed in chapter 5. Thus, Figure 6.3 demonstrates an evidence of a considerable decrease in the output cell resistance by approximately three orders of magnitude over time during recrystallization process. That will be enough to use for various logic functions as will discuss later in this chapter.

6.2 3T PCM Device: Threshold Switching Resistance

For studying the various logic operations in a single element of the proposed vertical 3T device, the device is considered here as a binary logic system having the logic values ‘0’ and

‘1’ where the different logic values correspond to detectably different reading resistances during reading operations between the bottom and the heater electrical contacts. For practical convenience, it was preferable to have a wide difference in the output resistances (i.e. high resistance window) of the two logic states so that the logic states could be most readily identified. This objective is achieved here by associating one logic level to the situation where a continuous crystalline pathway was present between the bottom and the heater electrical contacts and the other logic level to the situation where a continuous crystalline pathway was not present between them. So, it was dependent on the current flow between these two electrical contacts, i.e. it was necessary for the electrical current to flow at least through a part of amorphous region rather than a crystalline region for producing high resistance levels. Thus, the output resistance decreased or increased relative to the former or latter situation, and it can sense by applying a read pulse having a low voltage of 0.5 V with 70 ns pulse width and 10 ns rise/fall times.

As discussed in section 6.2.1, The corresponding SET voltage pulses, have been determined, for programming the vertical 3T device in this study, with a range of (1.7 – 2) V and 10 ns rise/fall times. Then, the corresponding RESET voltage pulse, for erasing the same proposed device after the programming process, has also been determined with a pulse of 1.5 V and 50 ns rise/fall times (section 6.2.2). A reference resistance level is then considered for distinguishing purposes of binary logic states to demonstrate various logic functions-based different resistance forms. Hence, a reference resistance R_{ref} (500 KΩ) is used in this study as a reasonable value for determining the logic output states based the programming resistance window, as shown in Figure 6.3. The reference resistance defines the logic level (i.e. ‘0’ or ‘1’ state) of the readable resistance as following: the output resistance would be assigned logic ‘0’ if its value was above or equal the reference resistance. Otherwise, it would be assigned logic ‘1’ if its value was below the reference resistance. Thus, a reading resistance above the

reference value is referred to a high resistance level (HR) or low logic state with a logic value '0'. Similarly, a resistance below a reference value refers to a low resistance level LR or high logic state with a logic value '1'. Thus, the presence of differences in the reading resistances of the 3T PCM device depends on the relative amounts and spatial distribution of crystalline and amorphous regions within the GST material.

6.3 Logic Gate Operation Based Reconfigurable 3T PCM Device

After the logic working principle of the designed 3T vertical device is described and then the appropriate threshold resistance is identified, we turn our attention to use of this device as a reconfigurable logic element to realize majority logic gate functions, such as NAND and NOR gates. The NAND and NOR gates are universal gates which can be used to implement any other Boolean functions including the AND, NOR and NOT logic functions. Hence, the focus of this thesis is on the implementation of the NAND and NOR logic functions in the designed 3T logic devices, through governing the relationship between the input voltage differences and the desired output resistance corresponding to implement the truth tables for each logic gate. Consequently, the use of such this logic element (i.e. the designed 3T vertical device) for implementing primitive logic functions, such as the NAND and NOR gates, provides an interesting insight to use the GST phase-change material within a designed element of a 3T vertical device as a reconfigurable logic element.

For simplicity and to understand the key aspects of introducing resistance switches in the three-terminal cell for logic NAND or NOR gate, two distinct voltages (0V and 1.7V) are chosen here according to the parametric and transient simulation results of the resistance-voltage characteristics, which are discussed previous sections in this chapter and the preceding chapters. These voltages are used to conform the binary inputs '0' and '1' states, respectively, which applied simultaneously to input (top and bottom) terminals of the 3T vertical logic

device for representing the possible input patterns of the logic combinations: “00”, “01”, “10” and “11”. For programming simulations, the logic voltage patterns are applied on a single three-terminal PCM device embedded into a virtual circuit of electrical test bench SPICE model, which consists of two voltage sources and a load resistor connected in series with each source (see Figure 6.1). The series resistance should be with a level of no more than the lower cell resistance (i.e. 4.5 KΩ), i.e. to produce no effect on the programming processes as discussed early in this chapter.

6.3.1 NAND Logic Functionality Based 3T PCM Device

As discussed early in chapter 4, different logic operations could be performed using the proposed logic element of the 3T vertical device structure by application of different voltages to electrical contacts top, bottom and side terminals. For example, a logic functionality of such 2-bit NAND gate operation can be realized by applying simultaneously two input voltage differences in various unique patterns. One is between the top and side contacts and the other is between the bottom and side contacts (see Figure 6.5). So, the side contact is used here as a ground. Then, the 3T cell is programmed according to the input patterns into different configurations of partially amorphous regions that in turn produces various resistance forms corresponding to the output logic states of the NAND logic function.

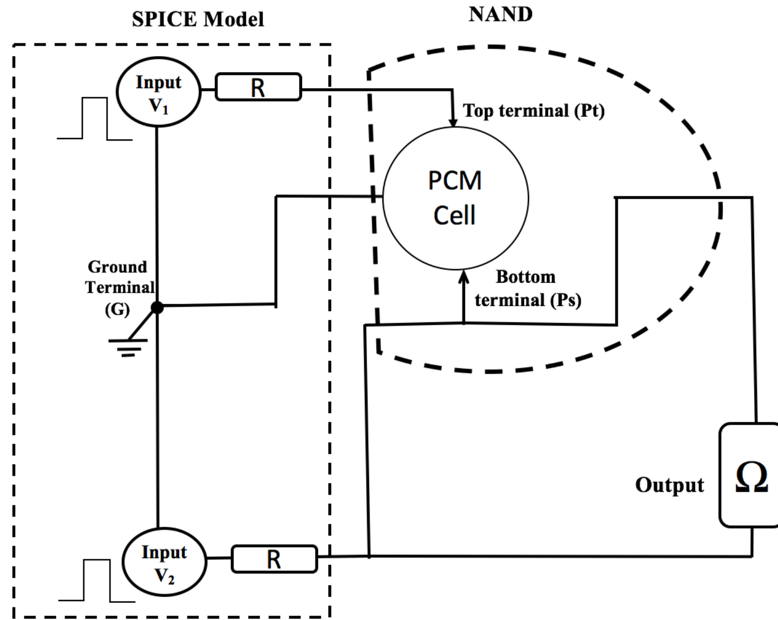


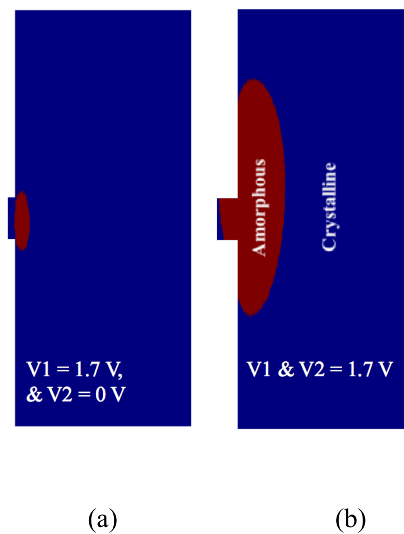
Figure 6.5 2-bit NAND gate function using a single element of the proposed vertical 3T device.

The resistance-voltage relationship within the 3T vertical cell is considered here to demonstrate the logic functionality of the 2-bit NAND gate. Two different pairs of the three-terminal (top-side and bottom-side) are used to provide the input binary pattern for the NAND gate, and then the corresponding resistance change of the device is used to determine the output logic state as part of the readout process. With the SET voltages of 0 V and 1.7 V (see Table 6.1) the sequence of logic patterns 00,01,10 and 11 is applied individually through the terminal inputs (V_1 and V_2) of the designed 3T cell along with a series resistance (R) with a value of 1.5 kΩ. Then, the stored data is obtained as distinct logic states by carefully sensing the readout resistance corresponding to the input patterns that limit the amorphous switching volume, as shown in Figure 6.6. The logic states are predefined according to specific threshold (reference) resistance, as discussed in section 6.3. The reference resistance (500 kΩ), is used as follows: if the readout resistance of the current writing attempt is equal to or greater than the threshold resistance, then the output state is set to logic 0; otherwise, this resistance is set to logic 1. So,

the logic NAND operation is realised by using the write-read programming processes and according to the SET voltage patterns summarized in table 6.1.

Table 6.1 The NAND gate logic operation based three-terminal vertical cell, V1 and V2 are the input voltages across the pairs (top-ground) and (bottom –ground) contacts respectively.

V_1		V_2		R out	NAND
(V)	Logic	(V)	Logic	(KΩ)	Logic
0	0	0	0	4.5	1
0	0	1.7	1	10	1
1.7	1	0	0	10	1
1.7	1	1.7	1	1591	0



(a) (b)

Figure 6.6 Amorphous switching volumes in 2-bit NAND gate function based a single element of the proposed vertical 3T device, when the device was under a SET logic voltage patterns (a) V_1 and V_2 = 1.7 V, (b) V_1 = 1.7 V and V_2 = 0 V.

6.3.2 NOR Logic Functionality Based 3T PCM Device

Another primitive operation of the logic NOR function can potentially be implemented by using the vertical 3T element proposed in this work. So, it can also use this function as a universal logic gate for implementing complex logic functions, such as binary addition [65]. Thus, we turn our attention to realize a full description of performing the NOR logic function using a single element of the proposed 3T logic device.

Generally, we carried out a logic programming strategy for performing the NOR function similar to those used in performing NAND gate function in the 3T vertical device, as discussed in the previous section. The two pairs, top-side and bottom-side of the three-terminal, are also used to provide the input binary pattern for the NOR gate. Then the corresponding resistance change in the device is obtained by comparing with a reference resistance (R_{Ref} = 500 kΩ) to determine the state of the output logic as part of the readout process. Under voltage applications of 0 V and 1.7 V summarized in Table 6.2, the sequence of logic patterns 00,01,10 and 11 is also applied individually through the terminal inputs (V_1 and V_2) of the designed 3T cell along with a series resistance (R) with a value of 1 kΩ. We found that the change in the series resistance to be 1 kΩ instead of 1.5 kΩ, as used in the NAND operation, produces output resistance states corresponding to the logic states of the NOR function. Table 6.2 summarized the relationship between the input patterns and the readout resistance for the logic NOR gate. When the logic input state is 10 or 01, the output resistance state is higher than the R_{Ref} (logic 0), which are different states than that found in the NAND gate function (logic 1). Figure 6.7 shows the change in the amorphous switching volume of the NOR gate function when both the input V_1 and V_2 are under logic patterns of 10 or 01, compared with those patterns for performing the NAND logic function. Thus, it could use the voltages (0 V and 1.7 V) with a similar fashion of logic patterns used in the NAND operations, to introduce reconfigurable logic function using the vertical 3T logic element proposed in this work.

Table 6.2 The NOR gate logic operation based three-terminal vertical cell, V1 and V2 are the input voltages across the pairs (top-ground) and (bottom –ground) contacts respectively.

V_1	Logic	V_2 (V)		R out (KΩ)	NOR
0	0	0	0	4.5	1
0	0	1.7	1	1187	0
1.7	1	0	0	1187	0
1.7	1	1.7	1	1730	0

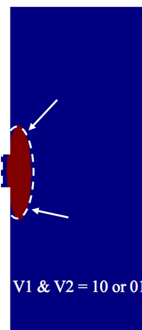


Figure 6.7 Amorphous switching volumes in performing the NOR gate function based a single element of the proposed vertical 3T device, when the device was under a SET logic voltage patterns 10 or 01.

6.4 Non-Volatile a 2-Bit Element Based 3T PCM Device

By describing the implementation of the NAND and NOR logic gates using three-terminal PCM devices, it is possible to construct more complex logic functions, such as NOT, XOR and XNOR. As mentioned above in this chapter, the NAND and NOR logic gates are standard gates that can be used to realize any possible truth tables of various logic functions (i.e. any Boolean logic function). Therefore, any logic operation of 2-bit input patterns can be described

by using a single reconfigurable three-terminal PCM element. For example, it can use the three-terminal PCM devices for building the logic and memory elements within the field programmable gate arrays (FPGAs) or crossbar configuration memory (CCM) through reducing the delay within the crossbar as well as the overall size of the configurable logic elements which in turn would reduce global routing overheads. The nature of the PCM material within the three-terminal cells eliminates the need to reconfigure the FPGA after power cycles through saving time as well as reducing the need to add external Flash memories or micro-controllers to re-program the FPGA configuration. Consequently, a single-reconfigurable three-terminal PCM device can indeed be used as a 2-bit memory element to provide various logic functions arranged within complex configurations for performing both logic and memory functions.

6.5 Chapter Summary

In summary, it has been shown in this chapter that it could be feasible to design and implement a reconfigurable 2-bit logic element based a single three-terminal PCM element. By using the PCM materials, the 2-bit logic element has been considered to be used for various non-volatile memory logic configurations by performing the resistive memory manner that is available in the chalcogenide GST material. By controlling the atomic structure of amorphous and crystalline states in the GST material implemented in a three-terminal logic element, different resistance levels were introduced through applied various logic patterns of the input electrical voltages. Thus, we have discussed firstly, in this chapter, the logic working principle of the three-terminal PCM devices to realize different logic memory operations for standard logic gates, such as NAND and NOR gates. Secondly, a binary logic system having the logic values ‘0’ and ‘1’ states, has been adapted to detect different reading resistances based on the Threshold (reference) Resistance (R_{ref}). Then, two distinct voltages, 0V and 1.7V, were chosen here based on the simulation results of the resistance-voltage characteristic to represent the

binary input ‘0’ and ‘1’ states, respectively, and describe a possible 2-bit binary function with different simultaneous patterns of voltage applications.

CHAPTER 7: Research Conclusions and Future Research Outlook

7.1 Research Conclusions

Temporary or permanent digital data storage is required in any function within information storage and processing systems. In the von Neumann computer architecture, solid-state memory plays a pivotal role in determining the hierarchical memory systems (memory taxonomy) and determines the corresponding characteristics and performance of the computer system in terms of speed, storage density and cost. The workhorses of established memory technologies such as SRAM, DRAM, Flash and the HDD have been developed and manufactured to provide competitive technologies, in terms of achieving high storage densities for modern digital system applications, with various levels of memory hierarchy during the past few decades. Going beyond the conventional architecture in digital and computer systems of processing of data followed by storage, research has been intensifying over the recent years to combine both processing and data storage collocally and at the same time to overcome the limitations of conventional architectures. However, recent research in this direction is facing some challenges on the feasibility of combining binary or non-binary computations with state memory storage in a single elementary process within a successful development of computer systems. Furthermore, it is unclear whether these technologies can be scaled any further below the 16 nm technology node, as discussed in chapter 1. Hence, phase change memory (PCM) devices is a promising technology that provides an alternative solution (resistive switching behaviour) for future digital data storage in modern nonvolatile electronic devices. In addition, the PCM devices can be easily compatible and integrated with the complementary metal–oxide–semiconductor (CMOS) platform.

The PCM technologies are based on two pivotal processes crystallization and amorphization, as a result of the fast and reversible switching between a high resistance amorphous phase and low resistance crystalline phase. The switching state behaviour of the

chalcogenide material, such as $Ge_2Sb_2Te_5$ (GST), under different voltage applications, is one of promising candidates to complement or even replace the CMOS logic technologies. By achieving appropriate control over the Joule-heating reaction in the chalcogenide material through using appropriate electrical voltage pulses, the resistive switching states can be used for storing and even computing binary or non-binary data. The duration and magnitude of the applied voltages in the PCM device can be used to produce distinct resistance levels for storing intermediate data states.

Two alternative programming strategies can be used with the PCM devices for processing and storing of digital data. In the first approach, data can be written as crystalline logic bits in an amorphous material through heating the amorphous GST material up to crystalline temperature (crystallization process). In the second approach, amorphous logic bits can be written in a crystalline material by heating the crystallized GST material to a temperature that exceeds the melting temperature, followed by quick quenching of the melted area at cooling rates of tens of Kelvins per nanosecond into the amorphous phase (amorphization process). The crystallisation and melting temperatures of the GST material are around 428 K and 900 K respectively as indicated in chapter 5.

Recent extensive research efforts, both theoretical and experimental investigations, have been carried out to explore and understand the device logic functionality-based phase change material, such as GST, during both the crystallization and amorphization programming processes. However, most previous studies and investigations are carried out on a two-terminal PCM cell or device structure. Alternatively, there is a great opportunity to explain the natures of both crystallization and amorphization mechanisms in a three-terminal (3T) phase-change device for the purposes of a feasible logic implementation.

The main contribution of this thesis is a feasibility study of designing and simulating the performance of a realistic 3T phase-change device having a reconfigurable logic functionality. The sensitivity of performing crystallization and amorphization processes in the 3T device is considered for performing various voltage applications across different pairs of the device terminals. The electrical and thermal effects on device performance are an important part of PCM device design and modelling. Great efforts are carried out in this study to determine the active programming region within the material for producing distinct resistance states of an applicable 3T designed device. Thus, the key questions that have been successfully answered in this thesis are summarized as follows:

- Can conventional (laboratory level or even commercially viable) PCM device structures, such as the widely used mushroom-type PCM cell, be used to produce a realistic 3T phase-change device? What are the physical, geometrical, and voltage conditions needed to perform the RESET and SET operations? What are the size and position of the three device terminals, and better thermal confinement? In addition, other electrical considerations are also important, such as voltage levels, high/low resistance windows for distinct resistance logic states (resistance-voltage characteristic) and most importantly, the temperature-voltage characteristic.
- What are appropriate materials and electrical (and thermal) boundary conditions that can be used with the phase-change material, including cell size and material configurations, to produce appropriate temperatures for logic programming purposes.
- Can logic data storage (or even multilevel storage states) for computing applications be achieved using 3T phase-change elements? what are the limitations that can preclude current flow in the phase-change material when simultaneous inputs of voltages are applied.

- what are other logic functions that can be performed using these 3T phase-change elements to be as a reconfigurable logic element?
- what is the suitable crystallization model that can use in the 3T phase-change model to be computationally compatible with the electrical voltage applications, regarding complexity of modelling the phase transition process.

Overall, the results reported in this study are very promising for the future development of phase change logic memory technology as clearly indicated (with the agreement in the selected phase-change model with previously reported experimental and theoretical phase-change studies). The proposed 3T logic cell structure with such the mushroom-type cell, is a potentially viable and widely used in CMOS-compatible technology, especially when the logic cell is in nanoscale size and the terminal voltage applications allow cell integrated compatible with standard CMOS logic circuits. This is a significant step forward in the quest for PCM to complement or even replace existing technologies, such as SRAM, DRAM, Flash and HDD, which have now reached their fundamental concepts for employing and combining both digital computing data and memory storage in the same element. This thesis was structured in chapters to provide possibilities of answering the important key findings along with highlighted discussions that can be summarized as follows:

In Chapter 1, a brief review and comparison of various traditional and emerging memory technologies, such as SRAM, DRAM, FeRAM, MRAM, RRAM, and PCM, was discussed. A detailed introduction to phase change materials and memory devices are also presented, followed by the aims and objectives of this study.

In chapter 2, a brief introduction to digital system basics, followed by details and reviews about valuable phase-change material studies of applicable logic functionalities to use the nature of resistive switching in the chalcogenide phase-change materials for digital PCM

applications, such as threshold logic and multiple resistance states. PCM cell concepts, such as the key switching characteristics and features of phase change materials, along with basic structural and material design considerations are also considered. Two main cell geometry categories, contact-minimized cell and volume-minimized cell, were discussed by reviewing a wide range of applicable studies to exploit and develop feasible nonvolatile PCM elements. Valuable studies about achieving the logic functionality in two and three terminals phase-change cell structures were discussed the performing logic switching states in the phase-change material and under various manners of voltage applications. However, most applicable studies have discussed the performance of logic functions based two-terminal phase-change cell structure through either sequential operation of voltage applications, where longer computing delay required under successive voltage applications across the two-terminal phase-change device, or by applying the voltage applications between multi-terminal device configurations of an array of two-terminal that leads to introduce a higher chip space density. Thus, a single device structure for a reconfigurable logic function is a unified solution for simultaneous voltage applications using different pairs of the device terminals.

Depending on the PCM cell geometry categories published in the literature, i.e. contact-minimized cell and volume-minimized cell, two distinct structures of the three-terminal cell design can be proposed for logic function investigations: lateral and vertical three-terminal cell structures. In this study, the vertical cell structure was adopted and developed for providing primitive logic functions of both the NAND and NOR logic operations. All the details of the vertical 3T cell were discussed in chapters 4, 5 and 6. Nevertheless the lateral 3T cell structure can be considerable interest for future structure challenges of the nonvolatile PCM logic devices to perform reliable multilevel storage density, binary or non-binary storage data.

In chapter 3, a brief description of Multiphysics phase-change concepts along with a review of electrothermal and Phase-Change Models were presented. An overview of the different approaches for modelling the phase change simulation processes was considered through highlighting their applicability, advantages and shortcomings. Since the crystallization dynamics of the phase-change material has a direct effect on product distinct resistance levels in a way that the pattern of these resistance levels could be used for nonvolatile logic-memory applications, this study was considered a realistic model for the crystallization simulations based on the classical nucleation theory.This approach was provided separate evaluations of both nucleation and growth rates which used to control the applicable crystallization process and predicted transient volume fraction of the crystalline material of the $Ge_2Sb_2Te_5$(GST) material under various electrical applications. From the solutions of both nucleation and growth rates, the crystalline volume fraction of the phase-change material in the three-terminal device was calculated. The thermodynamic parameters of the phase-switching behaviour within the phase-change material (of both crystalline and amorphous phases) were updated through using a strong correlation between the crystalline volume fraction and the thermoelectric effector temperature dependence of material parameters. The thermoelectric parameters, both electrical and thermal conductivities, of the phase-change material were used through intermediate calculations to evaluate temperature distribution within the material. By using a reliable analytical model, such as Ielmini's model as discussed in this chapter, for updating the electrical conductivity calculations of the phase-change material, the temperatures were evaluated and then the crystalline and amorphous phases in the material were determined. Consequently, this multi-physics analytical model was used to provide realistic match conditions between the predicted calculations of the device design simulations and the experimental results in the literature.

In chapter 4, the geometry of the vertical device was designed to match the electrically realistic findings of cell optimization study provided by Ielmini et. al., as discussed in chapter 2. This was one of the most important reasons to achieve a difference of three orders of magnitude between the high (partial amorphous) and low (crystalline) resistances under various voltage applications in the 3Tphase-change device performance. the proposed modelling of multi-physics nucleation and growth approach in a realistic vertical three-terminal phase-change device design was implemented as well though using 2-dimension (2D) numerical simulation provided by COMSOL-MATLAB interface. The simulation modelling is mainly based on solving the equations of the electrical, thermal and phase change sub-models. The direct interaction between the coupled electro-thermal model and the phase-change model were exploited through using the interface provided by COMSOL with MATLAB. Thus, a feasible vertical three-terminal device structure based the GST phase-change material was proposed by considering all the details, such as the positions of all the three terminals within the structure, surrounding materials and the electrical (and thermal) boundary conditions.

A 2D finite-grid elements of the proposed device structure were created in COMSOL Multi-physics, and then their temperatures were calculated by its solver to export later the temperature distribution of the GST layer to the MATLAB for obtaining the calculations of phase switching dynamics of the GST material. Validation of the crystallization model developed in this research project was presented through comparing the crystalline fraction calculations with their typically experimental measurements that published in the literature.

The implementation of the multi-physics approach in finite-elements based realistic device model was deeply discussed for performing the write/erase programming and read processes of various logic functions in the vertical three-terminal device design. However, one advanced

point was not considered through using multi-physics nucleation and growth approach in the three-terminal PCM model that may further enhance this modelling by extending the model to a full 3D capability. At the moment, such an extension would undoubtedly slow down the speed of numerical simulations, as for 3D simulations a large increase in the number of calculations will be required in the third dimension. Therefore, an approach to make the simulations time-efficient in 3D would also be required.

In chapter 5, the simulation details of performing both SET and RESET processes for various logic operations in a vertical three-terminal PCM model were presented. The discussion was considered the transient formation of stable crystalline nuclei and their subsequent growth following the thermal history in the GST material of the phase-change layer. Thus, a parametric study of temperature-voltage characteristics and then resistance-voltage characteristics were performed to determine pulse amplitudes of applicable voltage applications for both the transient SET and RESET simulations, as discussed in chapter 6. The desired voltages were obtained to produce the melting temperature (around 900K) in the active GST material for the programming SETprocesses, while other voltages were determined to produce the crystalline temperature (around 428 K) for the programming RESET processes. This was important also for writing and erasing processes of distinct resistance levels for performing various logic functions.

Also, in chapter 6 and from our great efforts resulted in both steady-state and transient simulations, some applicable logic function simulations, such as the logic functions of NAND and NOR gates, were performed on a single vertical three-terminal PCM device via providing a truth table of each logic operation. The truth table of each logic function reflects the actual logic relationship between the distinct output resistances and the input voltages based the proposed 3T device. Due to the difference between the resistivity of the GST phase-change

material according to the crystalline and partial amorphous phases, the GST layer in the three-terminal device allowed storing logic information by associating the logical level '0' and '1' to these two phases respectively. In this study, the levels '0' and '1' have been referred to the low and high resistance levels, respectively. A reasonable reference resistance, R_{ref} = 500 KΩ, was used in this study to determine the logic levels '1' and '0' of the readable resistance levels. Thus, a good agreement was observed from the simulation results within the truth table of each logic function that considered the actual logic functionality of the proposed element of a vertical three-terminal device. At the end of this chapter, some advanced logic functionalities, such as a 2-bit multiplexer or any logic operation of 2-bit input patterns, were discussed by using a single vertical phase-change element to reflect a reconfigurable logic functionality of a three-terminal phase-change device.

7.2 Future Work

The use of a realistic developed phase-change model, such as classical nucleation and growth approach, is a valuable tool for studying the details of phase transitions in phase-change materials. Under this approach, it was possible to carry out the SET and RESET transient simulations in 3T phase-change devices of various logic functions at practical computational times. A vertical three-terminal device based on GST phase-change material was proposed and used in this work to perform primitive logic functions of some essential logic gates, such as NAND and NOR gates. Consequently, the study in this thesis opens a possible way toward a series of future research directions that can be summarized as follows:

- The modelling and simulation work carried out in this thesis focused on using a vertical three-terminal phase-change device to perform essential logic functions of some primitive logic gates, such as NAND and NOR gates. The vertical cell was designed based on concepts of contact-minimized phase-change cell that considered

the effect of using a heater metal contact to achieve efficient heating within a specific region of the phase-change layer. Cell design can be extend to a lateral three-terminal phase-change cell structure based on concepts of volume-minimized PCM cell [6]. The lateral three-terminal phase-change elements may provide a way toward producing multilevel storage data-based computing system by offering high density area for programming into multiple resistance states without increasing cell size [131]. Although the use of a three-terminal multilevel cell (MLC) approach may increase memory density, the concept of volume-minimized phase-change (lateral) cell will intrinsically produce larger cross-sectional cell area than in a vertical three-terminal cell to achieve reliable intermediate resistance levels [6][63][80][83]. Thus, the size of the three-terminal lateral cell needs to be considered for producing various logic applications.

- Another useful extension to the current research is extending the previous 2D finite-element model to a full 3D capability. This provides a more realistic modelling of the temperatures and current/voltage conditions in the devices. This also enables more realistic studies of scaling to take place since the device cell confinement is not in three-dimensions and hence closer comparison to experimental studies. However, several challenges should be tackled when the model simulations are in 3D, such as cell structure, materials of the layers and creating appropriate mesh elements with an appropriate size and shape, reflecting the critical size of crystalline nuclei.
- The current study applied one of the main programming strategies of the phase change material in a three-terminal device by switching a crystalline phase to an amorphous phase during the writing processes, and then the amorphous to crystalline phases during the erasing processes. The other programming strategy may also be interesting to investigate (i.e. starting from amorphous to crystalline phases, and then followed

by an erasing process from crystalline to amorphous phase). This programming strategy requires more attention related to erase the crystalline region in an amorphous material [78], as discussed in chapter 2 of this thesis.

- The energy accumulation and direct overwrite processes in $Ge_2Sb_2Te_5$ (GST) material to reach the threshold point of abruptly resistance changes, as discussed by Y. Li et al. [64], can be exploited to emulate a synaptic-like response based three-terminal phase-change devices for arithmetic computing and multistate memories. By performing arithmetic computing functions with the GST phase-change materials, a "brain-like" functionality can be designed through using simple elements of a phase-change neurons, such as the device cells designed in this work and the multi-physics computational model. Using this technique, neuromorphic processing systems for non-binary arithmetic processing for a biological neuromorphic type processing can also be designed.

Bibliography

[1] T. P. Leervad Pedersen, J. Kalb, W. K. Njoroge, D. Wamwangi, M. Wuttig, and F. Spaepen, “Mechanical stresses upon crystallization in phase change materials,” *Appl. Phys. Lett.*, vol. 79, no. 22, pp. 3597–3599, 2001.

[2] S. Senkader and C. D. Wright, “Models for phase-change of Ge2Sb2Te5 in optical and electrical memory devices,” *J. Appl. Phys.*, vol. 95, no. 2004, pp. 504–511, 2004.

[3] K. B. Blyuss, P. Ashwin, A. P. Bassom, and C. D. Wright, “Master-equation approach to the study of phase-change processes in data storage media,” *Phys. Rev. E - Stat. Nonlinear, Soft Matter Phys.*, vol. 72, no. 1, pp. 1–8, 2005.

[4] V. Weidenhof, I. Friedrich, S. Ziegler, and M. Wuttig, “Laser induced crystallization of amorphous Ge2Sb2Te5 films,” *J. Appl. Phys.*, vol. 89, no. 6, pp. 3168–3176, 2001.

[5] P. Hosseini, “Carbon Based Materials for Advanced Memory and Computing Devices,” *PhD Thesis, Exeter University*. 2013.

[6] M. W. Simone Raoux, “Phase Change Materials Science and Applications,” in *Springer Science & Business Media*, 2010.

[7] L. Wang, C. H. Yang, and J. Wen, “Physical principles and current status of emerging non-volatile solid state memories,” *Electron. Mater. Lett.*, vol. 11, no. 4, pp. 505–543, 2015.

[8] C. Chen and J. An, “DRAM write-only-cache for improving lifetime of phase change memory,” *IEEE 59th Int. Midwest Symp. Circuits Syst.*, no. October, pp. 16–19, 2016.

[9] A. Chen, “Solid-State Electronics A review of emerging non-volatile memory (NVM) technologies and applications,” *Solid State Electron.*, vol. 125, pp. 25–38, 2016.

[10] P.C. Lacaze and L.C. Lacroix, “Non-volatile memories,” *John Wiley Sons.*, pp. 15–19, 2014.

[11] Q. Stainer et al., “Self-referenced multi-bit thermally assisted magnetic random access

memories," *Appl. Phys. Lett.*, vol. 105, no. 3, pp. 32405–1–32405–3, 2014.

[12] M.J. Xing et al., "Single ferromagnetic layer magnetic random access memory," *J. Appl. Phys.*, vol. 114, no. 8, pp. 84306–1–84306–4, 2013.

[13] Z. Diao et al., "Spin-transfer torque switching in magnetic tunnel junctions and spin-transfer torque random access memory," *J. Phys., Condens. Matter*, vol. 19, no. 16, pp. 165209–1–165209–13, 2007.

[14] K. Ando et. al., "Spin-transfer torque magnetoresistive random-access memory technologies for normally off computing," *J. Appl. Phys.*, vol. 115, no. 17, pp. 172607–1–172607–6, 2014.

[15] H. Ishiwara, "Ferroelectric random access memories," *J. Nanosci. Nanotechnol.*, vol. 12, no. 10, pp. 7619–7627, 2012.

[16] Y. Hou et. al., "Fast switching protocol for ferroelectric random access memory based on poly(vinylidene fluoride-trifluoroethylene) copolymer ultrathin films," *Appl. Phys. Lett.*, vol. 102, no. 6, pp. 63507–1–63507–3, 2013.

[17] I. Friedrich et al., "Structural transformations of Ge2Sb2Te5 films studied by electrical resistance measurements," *J. Appl. Phys.*, vol. 87, no. 9, pp. 4130–4134, 2000.

[18] S. Raoux et. al., "Phase-change random access memory: A scalable technology," *IBM J. Res. Dev.*, vol. 52, no. 4–5, pp. 465–479, 2008.

[19] Y. Yin et al., "Dependences of electrical properties of thin GeSbTe and AgInSbTe films on annealing," *Jpn. J. Appl. Phys*, vol. 44, no. 8, pp. 6208–6212, 2005.

[20] P. Zhou et al., "Role of TaON interface for CuxO resistive switching memory based on a combined model," *Appl. Phys. Lett.*, vol. 94, no. 5, pp. 53510–1–53510–3, 2009.

[21] Q.Q. Sun et al., "Controllable filament with electric field engineering for resistive switching uniformity," *IEEE Electron Device Lett.*, vol. 32, no. 9, pp. 1167–1169, 2011.

[22] N. Lu et al., "A novel method of identifying the carrier transport path in metal oxide

resistive random access memory," *J. Phys. D, Appl. Phys.*, vol. 48, no. 6, pp. 65101–1–65101–5, 2015.

[23] Y. Fujisaki, "Overview of emerging semiconductor non- volatile memories," *IEICE Electron. Exp.*, vol. 9, pp. 908–925, 2012.

[24] H. Shiga et.al., "A 1.6GB/s DDR2 128Mb chain FeRAM with scalable octal bitline and sensing schemes," *IEEE ISSCC*, pp. 464–465, 2009.

[25] Y. K. Hong et al., "130 nm technology 0.25 µm2, 1T1C FRAM cell for SoC (System-on-a-Chip)- friendly applications," *IEEE VLSI*, pp. 230–231, 2007.

[26] S. K. Kurinec and K.E. Iniewski, *"Nanoscale Semiconductor Memories: Technology and Applications," CRC Press*. 2013.

[27] C. Lam, "Cell design considerations for phase change memory as a universal memory. In VLSI Technology, Systems and Applications," *VLSI-TSA, IEEE*, pp. 132–133, 2008.

[28] H.-S. Philip Wong and Sayeef Salahuddin, "Memory leads the way to better computing. Nature Nanotechnology," vol. 10, no. 3, pp. 191–194, 2015.

[29] J.S. Meena et al., "Overview of emerging nonvolatile memory technologies," *Nanoscale Res. Lett.*, vol. 9, no. 526, p. 1, 2014.

[30] B. Prince, "Trends in scaled and nanotechnology memories," *IEEE NVMSTS*, pp. 55–61, 2005.

[31] C. S. Hwang, "Prospective of semiconductor memory devices: from memory system to materials," *Adv Electron Mater*, vol. 1, p. 1400056, 2015.

[32] M. Marinella, "The Future of Memory," *Albuquerque, NM 87185*, p. 319, 2013.

[33] M.J. Marinella et al., "Storage Class Memory," *ITRS Emerging Research Device, workshop*. 2012.

[34] W. Kim et al., "Extended scalability of perpendicular STT-MRAM towards sub-20nm MTJ node," *IEEE IEDM*, p. 24.1.1–24.1.4, 2011.

[35] T. Sakamoto et al., “Nanometer-scale switches using copper sulfide,” *Appl. Phys. Lett*, vol. 82, pp. 3032–3034, 2003.

[36] M. N. Kozicki et al., “Nanoscale memory elements based on solid-state electrolytes,” *IEEE T. Nanotechnol*, vol. 4, pp. 331–338, 2005.

[37] M. Kund et al., “Conductive bridging RAM (CBRAM): an emerging non-volatile memory technology scalable to sub 20nm,” *IEEE IEDM*, pp. 754–757, 2005.

[38] Y. Li, H. Zhao, H. Tian, X. Wang, W. Mi, Y. Yang, and T. Ren, “Novel Graphene-Based Resistive Random Access Memory,” *IEEE Int. Conf.*, pp. 3–6, 2016.

[39] Sita Dugu et al., “A graphene integrated highly transparent resistive switching memory device A graphene integrated highly transparent resistive switching memory device,” *APL Mater.*, vol. 6, no. 5, p. 58503, 2018.

[40] L. Wang, “A Study of Terabit Per Square Inch Scanning Probe Phase Change Memory,” *PhD Thesis, Exeter University*. 2009.

[41] C. Wei, A. Dhar, and D. Chen, “A Scalable and High-Density FPGA Architecture with Multi-Level Phase Change Memory,” pp. 1365–1370, 2015.

[42] Y. Hongxin, “High Performance Lateral Phase Change Random Access Memory,” *PhD Thesis, Singapore University*. 2013.

[43] S. Lai and T. Lowrey, “OUM-A 180 nm nonvolatile memory cell element technology for stand-alone and embedded applications,” *IEDM Tech. Dig.*, p. 36.5.1-36.5.4, 2001.

[44] G. Navarro et al., “Effects of SiO2 inclusions in GeTe based alloys for PCM applications,” *European Phase Change and Ovonics Symposium (EPCOS)*. 2013.

[45] Q. Wang, “Improving the Performance and Energy Efficiency of Phase Change,” vol. 30, no. 2009, pp. 110–120, 2015.

[46] H. Hayat, “A Study of The Scaling and Advanced Functionality,” *PhD Thesis, Exeter University*. 2016.

[47] C. V Thompson, “Evaluation of Phase Change Materials for Reconfigurable Interconnects,” *Master Dissertation, Nanyang Technological University*. 2010.

[48] M. Hase and J. Tominaga, “Thermal conductivity of GeTe/Sb2Te3 superlattices measured by coherent phonon spectroscopy,” *Appl. Phys. Lett.*, vol. 99, pp. 2–4, 2011.

[49] C. Ahn, S. W. Fong, Y. Kim, S. Lee, A. Sood, C. M. Neumann, M. Asheghi, K. E. Goodson, E. Pop, and H. S. P. Wong, “Energy-Efficient Phase-Change Memory with Graphene as a Thermal Barrier,” *2015*, vol. 15, no. 10, pp. 6809–6814.

[50] A.Behnam el at., “Nanoscale phase change memory with graphene ribbon electrodes,” *Appl. Phys. Lett.*, vol. 107, no. 12, p. 123508, 2015.

[51] R. A. Cobley, C. D. Wright, and J. A. Vazquez Diosdado, “A Model for Multilevel Phase-Change Memories Incorporating Resistance Drift Effects,” *IEEE J. Electron Devices Soc.*, vol. 3, no. 1, pp. 15–23, 2015.

[52] Y. Yin, N. Higano, H. Sone, and S. Hosaka, “Ultramultiple-level storage in TiNSbTeN double-layer cell for high-density nonvolatile memory,” *Appl. Phys. Lett.*, vol. 92, pp. 2–4, 2008.

[53] M. Joshi, “A Fast and Energy-Efficient Multi Level Cell Based Phase Change Memory System,” *PhD Thesis, Florida University*. 2010.

[54] Ovshinsky, “Logical Operation Circuit Employing Two-Terminal Chalcogenide Switches,” *Patent, Ulllted States, Us Pat. 543,737*, 1996.

[55] S. R. Ovshinsky, “Optical cognitive information processing - A new field,” *Jpn. J.Appl. Phys.*, vol. 43, p. 4695, 2004.

[56] P. Hosseini, J. A. V. Diosdado and C. D.Wright, “Beyond von-Neumann computing with nanoscale phase-change memory devices,” *Adv. Funct. Mater.*, vol. 23, no. 18, pp. 2248–2254, 2013.

[57] M. M. Aziz and R. J. H. C.D. Wright, Y. Liu, K.I. Kohary, “Arithmetic and biologically-

inspired computing using phase-change materials," *Adv. Mater.*, vol. 23, pp. 3408–3413, 2011.

[58] A. L. Lacaita, A. Redaelli, D. Ielmini, F. Pellizzer, A. Pirovano, A. Benvenuti, and R. Bez, "Electrothermal and phase-change dynamics in chalcogenide-based memories," *IEDM Tech. Dig. IEEE Int. Electron Devices Meet. 2004.*, pp. 911–914, 2004.

[59] A. Redaelli, D. Ielmini, A. L. Lacaita, F. Pellizzer, A. Pirovano, R. Bez, P. Milano, and L. Vinci, "Impact of crystallization statistics on data retention for phase change memories," *IEEE Electron Devices Meet.*, vol. 0, no. c, pp. 5–8, 2005.

[60] Y. Kwon and D. H. Kang, "Statistics of crystallization kinetics in nanoscale systems," *Scr. Mater.*, vol. 78–79, pp. 29–32, 2014.

[61] J.A. Kalb el at., "Crystal morphology and nucleation in thin films of amorphous Te alloys used for phase change recording," *J. Appl. Phys.*, vol. 98, p. 54902, 2005.

[62] H. B. Bakoglu, "Circuits, Interconnections, and Packaging for VLSI," *Addison Wesley, Reading, MA*, p. 527, 1990.

[63] S. R. Ovshinsky, "Reversible electrical switching phenomena in disordered structures," *Phys. Rev. Lett.*, vol. 21, no. 20, p. 1450, 1968.

[64] Y. Li, Y. P. Zhong, Y. F. Deng, Y. X. Zhou, L. Xu, and X. S. Miao, "Nonvolatile 'AND,' 'OR,' and 'NOT' Boolean logic gates based on phase-change memory," *J. Appl. Phys.*, vol. 114, pp. 5–8, 2013.

[65] M. Cassinerio, N. Ciocchini, and D. Ielmini, "Logic computation in phase change materials by threshold and memory switching," *Adv. Mater.*, vol. 25, pp. 5975–5980, 2013.

[66] W. Zhang and T. Li, "Helmet: A resistance drift resilient architecture for multi-level cell phase change memory system," *2011 IEEE/IFIP 41st Int. Conf. Dependable Syst. Networks*, pp. 197–208, 2011.

[67] K. L. Grosse, F. Xiong, S. Hong, W. P. King, and E. Pop, "phenomenon of nanometer-scale Joule and Peltier effects in phase change memory devices," *Appl. Phys. Lett.*, vol. 102,p. 193503, 2013.

[68] S. R. Ovshinsky, "Symmetrical current controlling device," in *US Patent 3271591, U. P. 3271591*, 1966.

[69] H. P. Wong, S. Raoux, S. Kim, J. Liang, J. P. Reifenberg, B. Rajendran, M. Asheghi, and K. E. Goodson, "Phase Change Memory," *Proc. IEEE*, vol. 98, no. 12, pp. 2201–2227, 2010.

[70] S. Hudgens and B. Johnson, "Overview of Phase-Change Chalcogenide Nonvolatile Memory Technology," *MRS Bull.*, vol. 29, pp. 829–832, 2004.

[71] R. A. Cobley and C. D. Wright, "Parameterized SPICE model for a phase-change RAM device," *IEEE Trans. Electron Devices*, vol. 53, no. 1, pp. 112–118, 2006.

[72] S.R. Ovshinsky el at., "A Threshold switching in chalcogenide-glass thin films. J. Appl. Phys.," *J. Appl. Phys.*, vol. 51, pp. 3289–3309, 1980.

[73] S. Prakash et al., "A guideline for designing chalcogenide-based glasses for threshold switching characteristics," *EEE Electron Device Lett.*, vol. 18, pp. 45–47, 1997.

[74] S.R. Ovshinsky, "Localized states in the gap of amorphous semiconductors," *Phys. Rev. Lett.*, vol. 36, pp. 1469–1472, 1976.

[75] D.Emin, "Current-driven threshold switching of a small polaron semiconductor to a metastable conductor," *Phys. Rev.*, vol. 74, p. 35206, 2006.

[76] D. Ielmini and Y. Zhang, "Analytical model for subthreshold conduction and threshold switching in chalcogenide-based memory devices," *J. Appl. Phys.*, vol. 102, no. 5, pp. 0–13, 2007.

[77] N. Papandreou, H. Pozidis, a. Pantazi, a. Sebastian, M. Breitwisch, C. Lam, and E. Eleftheriou, "Programming algorithms for multilevel phase-change memory," *Proc. -*

IEEE Int. Symp. Circuits Syst., pp. 329–332, 2011.

[78] C. D. Wright, L. Wang, P. Shah, M. M. Aziz, E. Varesi, R. Bez, and M. Moroni, "The Design of Re-writeable Ultra-High Density Scanning-Probe Phase-Change Memories," *IEEE Trans. Nanotechnol.*, vol. 10, no. 4, pp. 900–912, 2010.

[79] D. Krebs, "Electrical transport and switching in phase change materials," *PhD Thesis, RWTH Aachen Univ.*, 2010.

[80] Geoffrey W. Burr et al., "Phase change memory technology," *J. Vac. Sci. Technol. B Microelectron. Nanom. Struct.*, vol. 28, no. 2, p. 223, 2010.

[81] A. Pirovano, a. L. Lacaita, a. Benvenuti, F. Pellizzer, S. Hudgens, and R. Bez, "Scaling analysis of phase-change memory technology," *IEEE Int. Electron Devices Meet. 2003*, pp. 699–702, 2003.

[82] S. Raoux, G. W. Burr, M. J. Breitwisch, C. T. Rettner, Y.-C. Chen, R. M. Shelby, M. Salinga, D. Krebs, S.-H. Chen, H.-L. Lung, and C. H. Lam, "Phase-change random access memory: A scalable technology," *IBM J. Res. Dev.*, vol. 52, no. 4, pp. 465–479, 2008.

[83] A. Pirovano, A. L. Lacaita, A. Benvenuti, F. Pellizzer, and R. Bez, "Electronic Switching in Phase-Change Memories," *IEEE Trans. Electron Devices*, vol. 51, no. 3, pp. 452–459, 2004.

[84] D. Loke, J. M. Skelton, W.-J. Wang, T.-H. Lee, R. Zhao, T.-C. Chong, and S. R. Elliott, "Ultrafast phase-change logic device driven by melting processes.," *Proc. Natl. Acad. Sci. U. S. A.*, vol. 111, no. 37, pp. 13272–13277, 2014.

[85] Stanford R. Ovshinsky et al., "Multi-Terminal Device Having Logic Functional," *US Pat. 7,186,998 B2*, 2007.

[86] T. Lowrey, "Multi-terminal Chalcogenide Logic Circuits," *US Pat. 7,969,769 B2*, 2011.

[87] C. David Wright, M. Armand, and M. M. Aziz, "Terabit-per-square-inch data storage

using phase-change media and scanning electrical nanoprobes," *IEEE Trans. Nanotechnol.*, vol. 5, no. 1, pp. 50–61, 2006.

[88] J. M. Li, H. X. Yang, and K. G. Lim, "Field-dependent activation energy of nucleation and switching in phase change memory," *Appl. Phys. Lett.*, vol. 100, no. 26, pp. 1–5, 2012.

[89] D.-H. Kim, F. Merget, M. Laurenzis, P. H. Bolivar, and H. Kurz, "Electrical percolation characteristics of Ge2Sb2Te5 and Sn doped Ge2Sb2Te5 thin films during the amorphous to crystalline phase transition," *J. Appl. Phys.*, vol. 97, no. 8, p. 83538, 2005.

[90] M. M. Aziz and C. D. Wright, "A slope-theory approach to electrical probe recording on phase-change media," *J. Appl. Phys.*, vol. 97, no. 10, p. 103537, 2005.

[91] G. Yue-Feng, S. Zhi-Tang, L. Yun, L. Yan, L. Yi-Jin, and F. Song-Lin, "Three-Dimensional Finite Element Simulations for the Thermal Characteristics of PCRAMs with Different Buffer Layer Materials," *Chinese Phys. Lett.*, vol. 27, no. 8, p. 88501, 2010.

[92] Y. Yin and S. Hosaka, "Controllable crystallization in phase-change memory for low-power multilevel storage," *Jpn. J. Appl. Phys.*, vol. 51, no. 6 PART 1, pp. 1–4, 2012.

[93] S. Sainon, S. Harnsoongnoen, and C. Sa-ngiamsak, "Comparison on the performance of the confined- chacogenide phase change memory with thin metal interlayer and lateral phase change memory," vol. 1, pp. 176–179, 2011.

[94] M. M. Aziz and C. D. Wright, "An analytical model for nanoscale electrothermal probe recording on phase-change media," *J. Appl. Phys.*, vol. 99, no. 3, p. 34301, 2006.

[95] L. Yan, S. Zhi-Tang, L. Yun, and F. Song-Lin, "Three-Dimensional Finite Element Analysis of Phase Change Memory Cell with Thin TiO2 Film," *Chinese Phys. Lett.*, vol. 27, no. 3, p. 38502, 2010.

[96] F. Xiong, "Ultra-Low Power Phase Change Memory With Carbon Nanotube

Interconnects," *Master Dissertation, Illinois University*. 2010.

[97] T. Zhang et al., "Phase change memory based on capped between polygermanium layers Phase change memory based on Ge2Sb2Te5 capped between polygermanium layers," vol. 113503, no. 2008, pp. 1–4, 2014.

[98] H. Hayat, K. Kohary, and C. D. Wright, "Can conventional phase-change memory devices be scaled down to single-nanometre dimensions ?," *Nanotechnology*, vol. 28, no. 3, p. 35202, 2016.

[99] I. Cinar, O. B. Aslan, a. Gokce, O. Dincer, V. Karakas, B. Stipe, J. a. Katine, G. Aktas, and O. Ozatay, "Three dimensional finite element modeling and characterization of intermediate states in single active layer phase change memory devices," *J. Appl. Phys.*, vol. 117, no. 21, p. 214302, 2015.

[100] M. Avrami, "Kinetics of phase-change II. Transformation-time relations for random distribution of nuclei," *J. Chem. Phys.*, vol. 8, p. 212, 1940.

[101] M.J. Starink, "Kinetic equations for diffusion-controlled precipitation reactions," *J. Mater. Sci.*, vol. 32, pp. 4061–4070, 1997.

[102] M.C. Weinberg el at., "Crystallization kinetics and the JMAK equation," *J. Non-Cryst. Solids*, vol. 219, pp. 89–99, 1997.

[103] W. Yu, X. Yi, and C. D. Wright, "Analysis of crystallization behaviour of $Ge_2Sb_2Te_5$ used in optical and electrical memory devices_Wright 2014," vol. 6, no. 7, pp. 415–424, 2014.

[104] K. F. Kelton, "Analysis of crystallization kinetics," *Materials Science and Engineering, A Structural Materials Properties Microstructure And Processing*, vol. 226. pp. 142–150, 1997.

[105] J. A. V´azquez, "A Cellular Automata Approach for the Simulation and Development of Advanced," *PhD Thesis, Exeter University*. 2013.

[106] N. Ohshima, "Crystallization of germanium-antimony-tellurium amorphous thin film sandwiched between various dielectric protective films," *J. Appl. Phys.*, vol. 79, no. 5, p. 8357, 1996.

[107] J. Kohout, "An alternative to the JMAK equation for a better description of phase transformation kinetics," *J Mater Sci*, vol. 43, pp. 1334–1339, 2008.

[108] A. Aladool, M. M. Aziz, and C. D. Wright, "crystallization dynamics in the $Ge_2Sb_2Te_5$ phase-change material Understanding the importance of the temperature dependence of viscosity on the crystallization dynamics in the $Ge_2Sb_2Te_5$ phase-change material," *J. Appl. Phys.*, vol. 121, no. 22, p. 224504, 2017.

[109] D. Turnbull and J. C. Fisher, "Rate of nucleation in condensed systems," *J. Chem. Phys.*, vol. 17, no. 4, p. 429, 1949.

[110] M. Volmer and A. Weber, "Keimbildung in ubersattigten Gebilden," *Z. Phys. Chem.*, vol. 119, pp. 277–301, 1926.

[111] B. Becker and W. Doring, "Kinetische Behandlung der Keimbildung in ubersattigten Dampfen," *Ann.phys.*, vol. 24, pp. 719–752, 1935.

[112] G. Eleonora, "Material studies for advanced phase change memories : doping , size reduction and interface effect," *PhD Thesis, Sylvain*, 2013.

[113] David T. Wu., "Nucleation theory," *Solid State Phys.*, vol. 50, pp. 37–187, 1997.

[114] H. B. Singh and A. Holz, "Stability limit of supercooled liquids," *Solid State Commun.*, vol. 45, no. 11, pp. 985–988, 1983.

[115] M. S. Salinga, "Phase Change Materials for Non-volatile Electronic Memories," *PhD Thesis*, RWTH Aachen University, p. 204, 2008.

[116] E. R. Meinders, H. J. Borg, M. H. R. Lankhorst, J. Hellmig, and A. V. Mijiritskii, "Numerical simulation of mark formation in dual-stack phase-change recording," *J. Appl. Phys.*, vol. 91, no. 12, pp. 9794–9802, 2002.

[117] Y. Kwon, B. Park, H. Yang, J. H. Hwang, D. H. Kang, H. Jeong, and Y. Song, "Modeling of data retention statistics of phase-change memory with confined- and mushroom-type cells," *Microelectron. Reliab.*, vol. 63, pp. 284–290, 2016.

[118] K. F. Kelton, a. L. Greer, and C. V. Thompson, "Transient nucleation in condensed systems," *J. Chem. Phys.*, vol. 79, no. 12, pp. 6261–6276, Dec. 1983.

[119] Ovshinsky et al., "Multi-Terminal Device Having Logic Functional," *US Pat. 0178402 A1*, 2004.

[120] U. Russo, D. Ielmini, A. Redaelli, and A. L. Lacaita, "Modeling of programming and read performance in phase-change memories - Part I: Cell optimization and scaling," *IEEE Trans. Electron Devices*, vol. 55, no. 2, pp. 506–514, 2008.

[121] Y. Li, S. M. Yu, C. H. Hwang, and Y. T. Kuo, "Temperature dependence on the contact size of GeSbTe films for phase change memories," *J. Comput. Electron.*, vol. 7, no. 3, pp. 138–141, 2008.

[122] J. A. Vázquez Diosdado, P. Ashwin, K. I. Kohary, and C. D. Wright, "Threshold switching via electric field induced crystallization in phase-change memory devices," *Appl. Phys. Lett.*, vol. 100, p. 253105, 2012.

[123] Comsol, "Comsol Multiphysics User's Guide," *Comsol AB*, 2008.

[124] L. Wang, C. D. Wright, P. Shah, M. M. Aziz, A. Sebastian, H. Pozidis, and A. Pauza, "Ultra high density scanning electrical probe phase-change memory for archival storage," *Jpn. J. Appl. Phys.*, vol. 50, no. 9 PART 2, 2011.

[125] D.-H. Kim, F. Merget, M. Först, and H. Kurz, "Three-dimensional simulation model of switching dynamics in phase change random access memory cells," *J. Appl. Phys.*, vol. 101, no. 2007, p. 64512, 2007.

[126] C. Peng, L. Cheng, and M. Mansuripur, "Experimental and theoretical investigations of laser-induced crystallization and amorphization in phase-change optical recording

media," *J. Appl. Phys.*, vol. 82, no. 9, p. 4183, 1997.

[127] S. Senkader, M. Aziz, and C. Wright, "A model for the phase-change process in GeSbTe thin films used for optical and electrical data storage," *Proc. SPIE Vol. 5069*, vol. 5069, pp. 98–104, 2003.

[128] H. Lo et al., "Three-terminal probe reconfigurable phase-change material switches," *IEEE Trans. Electron Devices*, vol. 57, no. 1, pp. 312–320, 2010.

[129] G. T. Jeong et al., "Process technologies for the integration of high density phase change RAM," *Proc. Integr. Circuit Des. Technol. Int. Conf.*, pp. 19–22, 2005.

[130] W. I. Park et al., "Self-assembled incorporation of modulated block copolymer nanostructures in phase-change memory for switching power reduction," *ACS Nano*, vol. 7, no. 3, pp. 2651–2658, 2013.

[131] Y. Yin, K. Ota, N. Higano, H. Sone, and S. Hosaka, "Multilevel storage in lateral top-heater phase-change memory," *IEEE Electron Device Lett.*, vol. 29, no. 8, pp. 876–878, 2008.

[132] F. M. Lee et al., "A novel cross point one-resistor (0T1R) Conductive Bridge Random Access Memory (CBRAM) with ultra low set/reset operation current," *Dig. Tech. Pap. - Symp. VLSI Technol.*, pp. 67–68, 2012.

[133] S. Raoux, F. Xiong, M. Wuttig, and E. Pop, "Phase change materials and phase change memory," *MRS Bull.*, vol. 39, no. 8, pp. 703–710, 2014.

[134] W. Wełnic and M. Wuttig, "Reversible switching in phase-change materials," *Mater. Today*, vol. 11, no. 6, pp. 20–27, 2008.