Electro-thermal process for probe storage on phase-change media

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ABSTRACT

We have investigated the feasibility of a probe storage technique, based on the interaction of a conductive tip with a phase-change (PC) media. The electro-thermal writing process was modeled using a finite element method. Both the crystalline and the amorphous phases were taken into account as a possible initial state of the phase-change material. The analysis of the corresponding current flows and temperature distributions showed that the choice of the initial state of the PC material greatly influences the shape of the written dots, due to the important difference in the electrical properties of these two states. When introducing a phase-change process in the model, the simulation results indicated indeed, that the crystalline dots spread through the thickness of the PC layer, whereas the amorphous dots are more localized at the top of the layer. One can then expect important effects on the readout process (and contrast) and the erasing mechanism, depending on the initial state of the storage media.

Keywords: Probe storage, chalcogenide thin-film, $Ge_2Sb_2Te_5$, electro-thermal modeling

1. INTRODUCTION

Constant technological improvements and innovations are required for data storage technology, to meet the need for ever higher storage capacity. Conventional technologies may soon reach their limits, and new techniques have been proposed. One of them is based on scanning probe microscopy. In this technique, a sharp tip is used to interact with the media, and to store and retrieve the data. The use of such a tip allows the confinement of the interaction volume to the nanometer scale. This concept has been previously demonstrated by IBM[1] with a thermo-mechanical probe on a polymer layer. As part of a European project, we are currently investigating the feasibility of probe-based storage on phase-change materials, well known for being extensively used in rewritable optical data storage. This technique is based on a conductive tip in contact with the storage media while scanning, to write, read and erase data. The writing and the readout principles are schematised in Fig. 1. The electro-thermal writing process is performed by passing a current from the tip to the sample. Then, the active layer is heated by the Joule effect. The phase-change process can occur and the information is stored in the material as crystalline or amorphous dots. For the readout process, a lower current is used, in order to limit the temperature increase in the system. The readout contrast relies on the great difference of electrical resistivity of the amorphous and crystalline phases, which, in the case of the $Ge_2Sb_2Te_5$ (GST) alloy is about four orders of magnitude[2] at room temperature. This characteristic can be seen as a positive point with respect to the readout contrast. Nevertheless, as the current flows preferentially towards regions of high conductivity, important differences in the temperature distribution are expected to appear, depending on the initial state of the phase-change material and on the electrical conductivity of the other materials used in the system. In this paper, we present the simulation results of the electro-thermal mechanism that takes place during the writing process. The study has been realised considering both the crystalline and the amorphous phases as a possible initial state of the PC media to analyse the effect on the shape and the size of the written dots and to determine the best configuration concerning the feasibility of the writing as well as the readout and the erasing processes.

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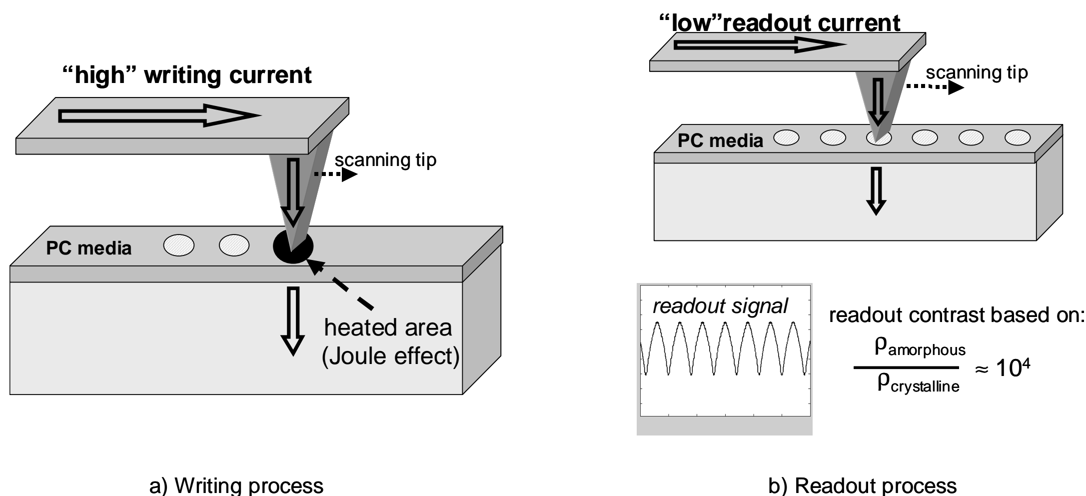


Fig. 1: Writing and readout principles of the probe storage system

2. MODELING THE ELECTRO-THERMAL WRITING PROCESS

2.1 Structure description

The storage system consists of a multilayer structure in which the active media is a 30nm thick $Ge_2Sb_2Te_5$ layer. This layer is sandwiched between a capping layer, on top of the structure, necessary to protect the GST layer from oxidation, and an under layer. The top layer must be carefully chosen with respect to its electrical properties to allow enough current to flow in the GST layer but also from a tribological point of view, since the scanning tip is in contact with this layer. These three layers are deposited on top of a silicon substrate. The modeling was performed in a three dimensional geometry with cylindrical symmetry. A 2D section of the structure is illustrated in Fig. 2. The inner part of the tip is made of Si, coated with a thin layer to improve the electrical contact. The contact radius between the base of the tip and the thin-film is 10 nm.

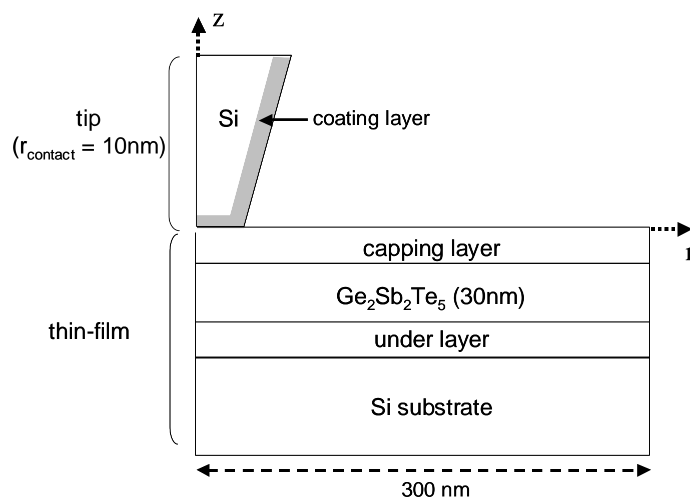


Fig. 2: 2D section of the geometry used in the simulation program

2.2 The theoretical model

The electro-thermal process was described by the Laplace equation and the heat equation, expressed respectively by equations 1 and 2, where σ is the electrical conductivity, V the electrical potential and E the electric field. ρ, k, and Cp correspond respectively to the density, the thermal conductivity and the specific heat.

$$\nabla.\left(\sigma.\nabla V\right)=0 \tag{1}$$

$$\rho C_p \frac{\partial T}{\partial t} - K.\nabla^2 T = \sigma \left|E\right|^2 \tag{2}$$

The system was solved by a finite element method to determine the electric field, the current flow and the temperature distribution in the whole structure. To model the writing process, a voltage was applied at the top of the tip. The bottom of the substrate was maintained at ground potential. These two boundaries were kept at room temperature, while the others were considered electrically and thermally insulated.

3. SIMULATION RESULTS

The model presented above was first of all used to optimise the structure for the electro-thermal process. We had in particular to determine the thickness and the electrical conductivity of the capping and the under layers that allow the current to flow in the GST layer, rather than laterally in the capping layer, in order to obtain a sufficient temperature increase for the phase-change process. The results of the optimisation could be applied to the experimental system since it was possible to adjust the electrical conductivity of the layers with the deposition conditions. Then, we complemented the simulation program and introduced a phase-change model. As mentioned before, we considered both the case of amorphous dots written in an initial crystalline material and the case of crystalline dots in an amorphous material, to analyse and to compare the corresponding dots' shapes and sizes.

3.1 Optimisation of the structure

The objective was to determine the properties of the capping and the under layers that enable a sufficient temperature increase in the GST layer to amorphise or to crystallise the material. We realised a parametric study of the electro-thermal process as a function of the thickness and the electrical conductivity of these two layers. We based our analysis on the maximum temperature in the GST layer when the system reached the steady state. The voltage applied at the boundaries of the structure was 10V. As explained in the next paragraph, the electrical conductivity of GST is temperature and electric field dependent. But in this quantitative analysis of the influence of the capping and the under layers, the GST electrical conductivity was considered constant and equal to $1000\Omega^{-1}m^{-1}$. The results are plotted in Fig. 3. The graphics represent the maximum temperature in the GST layer as a function of the characteristics of the capping layer (cf. Fig.3a) and the under layer (cf. Fig. 3b).

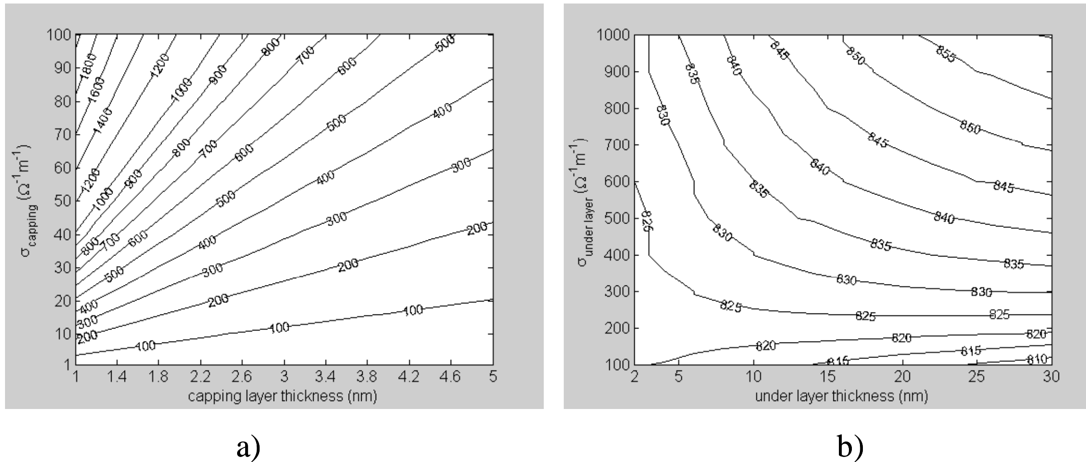


Fig. 3: Maximum temperature (ºC) in the GST layer as a function of the thickness and the electrical conductivity of a) the capping layer and b) the underlayer

The capping layer greatly influences the electro-thermal process since the temperature ranges from 100ºC to 2200ºC as its thickness and electrical conductivity are varied between 1 and 5nm and between 1 and $100\Omega^{-1}m^{-1}$ respectively. On the contrary, the characteristics of the under layer have minor effects on the electro-thermal process since a temperature variation of only 55ºC is induced in the range of the calculations. By modifying the thickness and the electrical conductivity of the capping layer it is then possible to control the temperature increase in the GST layer. The optimized structure must fulfill the temperature requirements for both the amorphisation and the crystallisation processes, since we consider here a re-writable system. More precisely, 650ºC, which is the melting temperature of $Ge_2Sb_2Te_5$, are needed to amorphise the material, and a temperature of about 300ºC must be reached to complete the crystallisation process in about 100ns. Another parametric study was then performed, still analysing the maximum temperature in the GST layer but as a function of the electrical conductivity of the capping layer and the GST layer. The thickness of the capping layer, selected from the previous results, was in that case 1.5nm. The figures 4a and 4b represent the results respectively for small and high values of the GST layer conductivity (corresponding to the amorphous and the crystalline states). The amorphous state is highly resistive at ambient temperature. For a GST electrical conductivity below $5\Omega^{-1}m^{-1}$, the temperature doesn't exceed 100ºC, whatever the electrical conductivity of the capping layer is. But taking into account the temperature and electric field dependences, and assuming that the electrical conductivity of the GST layer can be increased up to $20\Omega^{-1}m^{-1}$, a temperature of 300ºC is reached when the conductivity of the capping layer is at least $50\Omega^{-1}m^{-1}$ (Cf. Fig. 4a). Starting with the crystalline state (Cf. Fig. 4b), i.e. with a material of high conductivity, the melting temperature of 650ºC is also reached when the electrical conductivity of the capping layer is $50\Omega^{-1}m^{-1}$. Higher electrical conductivities are possible for the writing process since, as shown in Fig. 4, higher temperatures are obtained. But regarding the readout and the erasing processes, a too conductive capping layer may lead to short-circuit through crystalline areas. A capping layer with an electrical conductivity of $50\Omega^{-1}m^{-1}$ seemed to be a good compromise for the three processes.

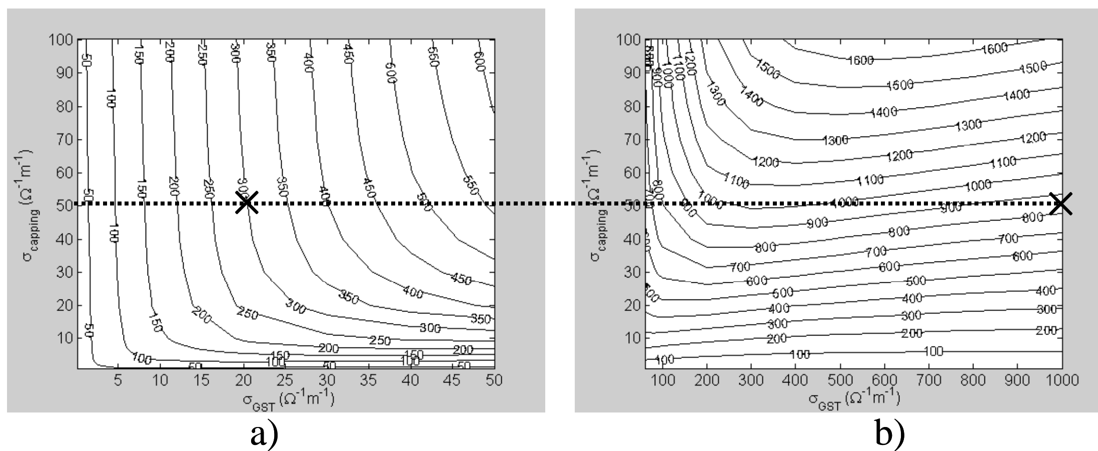


Fig. 4: Maximum temperature reached in the GST layer as a function of the electrical conductivity of the 1.5 thick capping layer a) for small electrical conductivity of the GST layer and b) for high electrical conductivity of the GST layer

3.2 The writing process

The results presented so far were obtained assuming the electrical conductivity of the GST layer as constant. The aim was to analyse qualitatively and quantitatively the influence of the characteristics of the capping and the under layers. The resulting optimized structure consists of a 1.5nm thick capping layer and a 10nm thick under layer, whose electrical conductivity are respectively $50\Omega^{-1}m^{-1}$ and $100\Omega^{-1}m^{-1}$. To model the whole writing process, the temperature and electric field dependence of the conductivity of the GST layer has to be taken into account. The GST layer is in this case no longer uniform regarding its electrical properties and the results may be different. The amorphous and the crystalline states are also characterized by different thermal conductivities[3,4], respectively 0.2 and $0.5Wm^{-1}K^{-1}$. We then complemented the simulation program, introducing appropriate expressions and values of the electrical and thermal conductivities for the amorphous and the crystalline states, and models for the phase-change processes.

3.2.1 From the amorphous to the crystalline state

Amorphous chalcogenide thin films have been extensively studied in the 1970's in threshold and memory switching devices[5,6]. At ambient temperature they are characterised by a very low electrical conductivity of about $0.1\Omega^{-1}m^{-1}$ for the GST alloy. But under higher temperatures and in the presence of a sufficient electric field, a reversible transition between this highly resistive state and a conductive state can be observed. This behavior has been explained by introducing a temperature (T) and electric field (E) dependence in the conductivity[7,8] such as

$$\sigma_{am}(T,E)=\sigma_0\times\exp\left(-\frac{\Delta\xi_{am}}{kT}\right)\times\exp\left(\frac{E}{E_0}\right)\ \Omega^{-1}m^{-1} \qquad (3)$$

where σ_0 is a constant, $\Delta\xi_{am}$ is the activation energy and E_0 is a critical electric field which can be temperature dependent. In the calculations, E_0 was considered constant.

The parameters σ_0 and $\Delta\xi$ were determined from experimental data of the electrical conductivity as a function of the temperature, obtained by a four-probe technique. Assuming first of all no electric field dependence, σ_0 and $\Delta\xi$ were respectively found to be $1.9\times10^4\Omega^{-1}m^{-1}$ and 0.3eV and were consistent with values given in the literature[2]. E_0 is very difficult to determine experimentally since one has to distinguish the effect of the electric field dependence from the temperature one. Few data are mentioned in the literature[5,6,9], ranging from 10^6 to $10^8 Vm^{-1}$. The value of E_0 introduced in the program was $5\times10^7 Vm^{-1}$. The time-dependent problem was solved for a pulse of voltage of 100ns with a 20ns rise time (cf. Eq. 4).

$$V(t)=10\times\left[1-\exp\left(-t/\tau\right)\right];\ \tau=20ns \qquad (4)$$

The calculations were first of all performed without crystallisation process to analyse the time dependence of some parameters, like the temperature and the electric field in the active layer, and the temperature distribution in the structure. Fig. 5 represents, respectively from the top to the bottom, the maximum electric field, temperature and electrical conductivity in the GST layer as a function of time. The curves point out the switching effect, from a highly resistive to a conductive state as the electric field exceeds a certain threshold value of about $3\times10^8 Vm^{-1}$, due to the electric field and temperature dependence of the GST conductivity. Thanks to this sudden increase of the GST electrical conductivity, the current easily flows in the active layer and a very high temperature of about 1000ºC is reached. Fast crystallisation processes can then be expected. Before introducing a phase-change process in the model, the analysis of

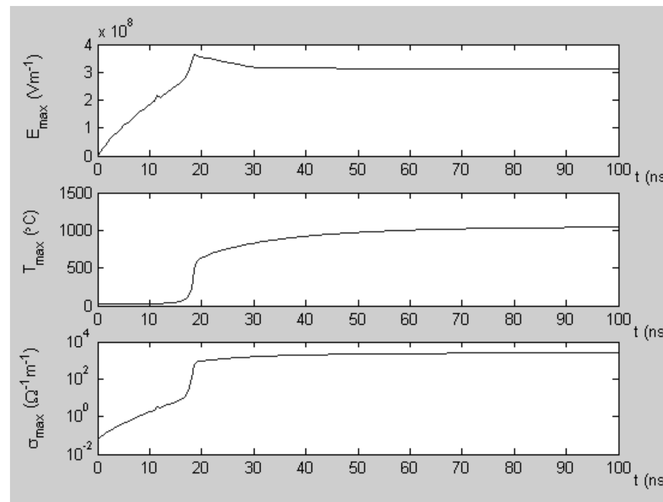
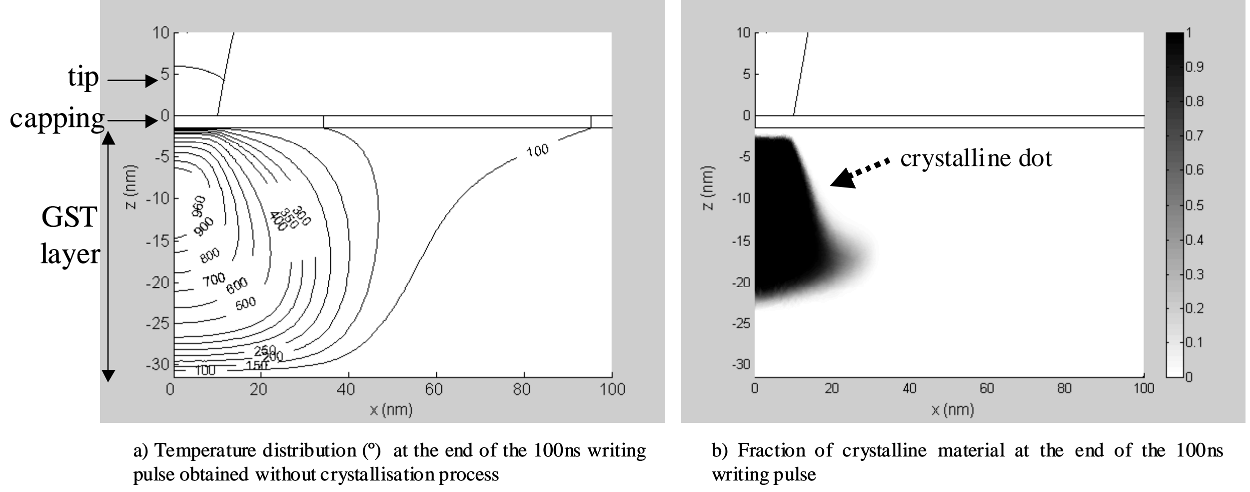


Fig. 5: Maximum value of the electric field, the temperature and the electrical conductivity in the GST layer versus time without crystallisation process.

the temperature distribution can give some information on the shape and the size of the written dots. The contour plot of Fig. 6a represents the isothermal lines at the end of the pulse in the bottom part of the tip, the capping and the GST layers. We can see that in this first case, the temperature distribution is well localised under the tip. The contours spread

through the thickness of the GST layer and the hottest are is located about 10nm below the interface with the capping layer.



a) Temperature distribution (°) at the end of the 100ns writing pulse obtained without crystallisation process

b) Fraction of crystalline material at the end of the 100ns writing pulse

Fig. 6: Temperature distribution (°C) and fraction of crystalline material at the end of the 100ns writing pulse of a crystalline dot in an amorphous material

The model used to describe the crystallisation kinetics was based on the widely used Johnson-Mehl-Avrami-Kolmogorov (JMAK) theory[10]. Although this model is only valid under specific conditions, like the fact that nucleation is assumed to be a random and uniform mechanism, it can be used as a first approach to the crystallisation process and easily introduced in the simulation program. The JMAK equation expresses the volume fraction of crystalline material χ under isothermal annealing conditions such that

$$\chi(t) = 1 - \exp\left(-\left(K_{cryst} t\right)^{n}\right), \tag{5}$$

where t is time, K_{cryst} the crystallisation rate and n the Avrami factor.
The crystallization rate K_{cryst} is usually given by the Arrhenius equation (Cf. Eq. 6),

$$K_{cryst} = \nu \exp\left(-\frac{E_a}{k_B T}\right), \tag{6}$$

where ν is a frequency factor, E_a the activation energy, T the absolute temperature and k_B the Boltzmann constant.
The parameters n, ν and E_a characterising the crystallization kinetics of the GST material were obtained from values[3,11-13] and fitting of experimental data[2] reported in the literature. The values introduced in the model are summarized in Table 1.

n	ν	E_a
2.6	1.5×10^{22} s^{-1}	2 eV

Table 1: Constants used in the crystallisation kinetics model of $Ge_2Sb_2Te_5$

It was mentioned before that as the material becomes crystalline, its electrical and thermal properties are modified. To describe the variation of electrical conductivity in the material, the percolation theory[14], which stipulates that there is a sharp transition from insulation to conduction when the volume fraction of a conductive medium in an insulating matrix reaches about 15%, was added to the model. During the calculations, the values of the electrical and thermal conductivities were changed respectively from the amorphous ones (i.e. Eq. 3 with $K_{am} = 0.2WK^{-1}m^{-1}$) to the crystalline ones (i.e. Eq. 7 with $K_{am} = 0.5WK^{-1}m^{-1}$) as χ exceeded 15%. The electrical conductivity of the crystalline material is

temperature dependent and can also be expressed by an Arrhenius relation, but with a much smaller activation energy of 0.04eV (Cf. Eq. 7). Equation 7 was obtained from fitting of experimental data[2].

$$\sigma_{cryst}(T) = 1.5 \times 10^{4} \times \exp\left(-\frac{0.04\,eV}{kT}\right) \Omega^{-1}\mathrm{m}^{-1} \tag{7}$$

The simulation results of the crystallization process modeled by the JMAK equation and the percolation theory of conduction are illustrated in Fig. 6b, which represents the fraction of crystalline material χ at the end of the 100ns writing pulse. The shape of the crystalline dot follows the isothermal lines. The written dot spread through most part of GST layer thickness, but is still surrounded by the amorphous material.

3.2.2 From the crystalline to the amorphous state

Amorphisation of the crystalline state occurs when the material is heated above its melting temperature and subsequently cooled down at very high rates in order to quench the material in its amorphous phase. Concerning the $Ge_2Sb_2Te_5$, the melting temperature is 650ºC and cooling rates of at least 10ºC/ns have to be achieved[15]. The pulse of voltage introduced previously in the model had to be modified in order to analyse the cooling behavior of the system, as plotted in Fig. 7. The rise and fall times were 20ns.

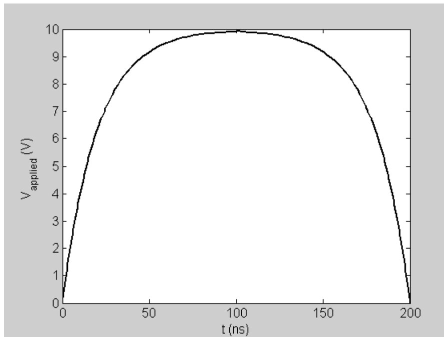
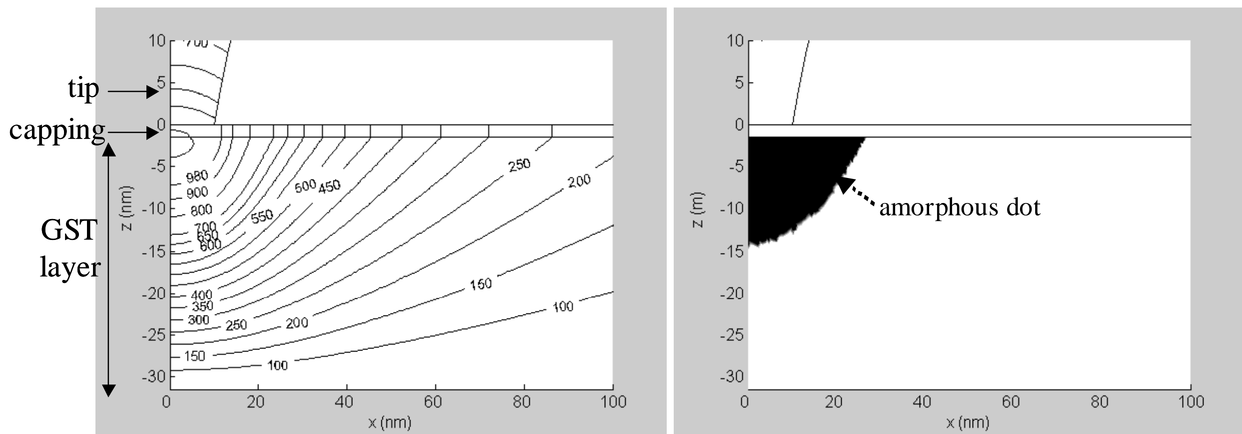


Fig. 7: Pulse of voltage applied for the writing process modeling of an amorphous dot in a crystalline material

The GST layer in its crystalline state was defined by a thermal conductivity of $0.5\mathrm{WK}^{-1}\mathrm{m}^{-1}$ and an electrical conductivity expressed by Eq. 7. The system defined by Laplace and heat equations was then solved for the whole duration of the pulse, i.e. for 200ns, and the amorphous dot was determined at the end of the calculations by the area that fulfill both amorphisation conditions, as mentioned above. The simulation results are presented in Fig. 8. We analysed first of all the temperature distribution prior to cooling, i.e. when the applied voltage reaches its maximum value after 100ns. Fig. 8a shows that the shape of the isothermal lines is very different from the one obtained from an amorphous material. The temperature distribution is no longer well localized under the tip but spreads laterally in the GST layer. A maximum temperature of 900ºC is reached and the hottest area is located at the top of the GST layer. When the applied voltage was switched off, the temperature in the GST layer decreased with a maximum cooling rate of 22ºC/ns. Quenching effect occured, resulting in an amorphous mark at the top of the GST layer, as represented in Fig. 8b.



a) Temperature distribution (º) at t=100ns, just before cooling.

b) Amorphous dot at the end of the pulse ($T_{max} \geq$ 650ºC and cooling rate ≥ 10ºCns)

Fig. 8: a) Temperature distribution (ºC) just before cooling and b) resulting amorphous dot at the end of the writing pulse.

4. CONCLUSION

We have modeled the electro-thermal writing process of a probe storage technique, based on a conducting tip interacting with a phase-change (PC) media, to investigate the feasibility of such system. The PC material considered here was the $Ge_2Sb_2Te_5$, well-known in optical recording technology. The amorphous and the crystalline states of GST are characterized by very different electrical conductivities, which are electric field and/or temperature dependent. The aim of the modeling was then to analyse the effect of the initial state of the active media on the current flow and the temperature distribution during the writing process. Models for the crystallisation and the amorphisation processes were introduced and a comparison of the corresponding recorded marks was realised. The simulation results showed that the crystalline dot spread through most part of the GST layer thickness, just below the tip, and was surrounding on all sides by the amorphous material. On the contrary, when starting from a crystalline material, the amorphous dot presented a hemi-spherical shape, localised at the top of the GST layer. Important effects on the readout contrast and also on the feasibility of the erasing process are then expected, whether the GST material is initially in its amorphous or crystalline phase. The model proposed here is being developed to answer these questions and to determine the best configuration concerning the initial state of the PC material, the detailed form of the memory stack and the format of the writing, reading and erasing processes.

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