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A Model for Multilevel Phase-Change Memories Incorporating Resistance Drift Effects

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ABSTRACT Phase change memories are emerging as a most promising technology for future nonvolatile, solid-state, electrical storage. However, to compete effectively in mainstream storage applications, a multilevel cell capability is most desirable. Unfortunately, phase-change memories exhibit a temporal drift in programmed resistance (and in threshold switching voltage) which appears to be a fundamental and universal property of the amorphous or partially amorphous phase. Phase-change device models should therefore include these drift effects in a realistic way so that circuit and systems designers can assess the likely performance of multilevel phase-change memories in a variety of potential applications. In this paper, therefore, we present a comprehensive SPICE-based model for phase-change devices that includes the capability for programming into multiple resistance levels, the prediction of the drift of cell resistance (and threshold voltage) with time, and the capability for modeling the randomness inherent to the resistance drift phenomenon. Simulations of multilevel programming and drift phenomena using the model are presented and compared to experimental results, with which there is very good agreement.

INDEX TERMS Nonvolatile memory, phase-change memory, memristors.

I. INTRODUCTION

Phase Change Memories (PCMs) are emerging as a most promising technology for future non-volatile, solid-state, electrical storage. PCMs offer excellent scalability, good endurance (cyclability) and fast write/read speeds. Furthermore, phase change memories can operate as true random-access devices, meaning that individual cells can be written, erased and re-written, unlike in conventional CMOS flash memory architectures. Such capabilities have been exploited in the commercial applications of PCMs in mobile phones, such as the 45-nm node 1 Gbit PCM chips produced by Micron with an erase time approximately ten times faster than (NOR-type) flash memory [1]. However, to compete effectively in mainstream mass-storage applications, where CMOS (NAND-type) flash memory and magnetic hard disk technologies currently dominate, it will be necessary to increase significantly the storage density currently achieved with phase-change technology. The main routes to achieve this are: (i) by direct downscaling (i.e., moving to smaller technology nodes) of single bit cells; (ii) by vertical stacking (i.e., 3D device architectures) of single bit cells; and (iii) by the implementation of multilevel (multi-bit) cells. While progress via route (i) is expected as a matter of course, such progress is relatively slow and costly, and to date phase-change technology lags somewhat behind conventional CMOS-flash memory technologies (already around the 20nm node). Progress via route (ii) potentially requires complex 3D device fabrication techniques, although significant advances have been made by the integration of phase-change cells and selector devices in a relatively simple stackable crossbar architecture [2]. Increasing PCM storage capacity by route (iii), the use of a multilevel cell (MLC) approach, is, on the face of it, a simple and attractive proposition, and could mean that phase-change devices would find applications not only in mass storage (flash replacement) but also, in the suggested "new" format of "storage-class memory" [3]–[5].

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Data are stored in phase-change memory cells by a programmed cell resistance, and with today's materials and cell architectures this programmed resistance can differ by 2-3 orders of magnitude between a fully crystallized (the so-called "set" state) and a fully amorphized (the so-called "reset" state) cell. This would seem to leave an ample "window" for the provision of multi-bit storage via the use of partially amorphized (i.e., partially "reset") or partially crystallized (i.e., partially "set") cells. However, it is found that resistance of PCM cells in all but the fully-crystalline state drifts (increases) with the "off" time t_{off} (i.e., the time between the end of the programming pulse and a subsequent read event), empirically described by a power law dependence given by [6]–[10].

$$R = R_0 . \left({}^{t_{off}}/_{t_0} \right)^{\nu_R} \tag{1}$$

where R_0 and t_0 are constants and the exponent ν_R characterizes the rate of drift and gives the slope of the straight line obtained when log(R) is plotted versus log(t). Thus, a cell written into a particular resistance state will exhibit a different resistance at a later time, leading to the possibility of readout errors and potentially limiting the viability and usability of multilevel storage with phase-change technology. Furthermore, the nature of the drift itself exhibits "randomness" in so much as the resistance varies in a "noisy" fashion on short (∼ second) time scales while on longer time scales the drift can be described by a monotonic increase in resistance characterized by the exponent ν_R as in (1) (see [11] for further details).

While significant progress has been made, experimentally and theoretically, in understanding and characterizing the physical processes that lie behind multilevel storage in phase-change memories and the associated resistance drift phenomenon, the development of circuit design models with a multilevel capability that also includes realistic modeling of the critical resistance drift effect has received relatively little attention. In this paper therefore we propose a comprehensive SPICE model for multilevel PCM cells that includes: (i) the capability for programming into multiple resistance levels; (ii) the prediction of the drift of cell resistance (and threshold voltage) with time; (iii) the capability for modeling the randomness inherent to the resistance drift phenomenon. This model can be used by circuit and systems designers to provide realistic simulations of the likely performance of MLC PCMs in a variety of potential applications.

II. PROPERTIES OF MULTILEVEL PHASE CHANGE MEMORIES

The structure of an archetypal phase-change memory cell, the so-called "mushroom-cell" design, is shown in Fig. 1. Here, the active volume of phase-change material (typically $Ge_2Sb_2Te_5$ or GST for short) sits on top of a TiN "heater" electrode whose lithographically-defined dimensions determine (along with the applied voltage and current) the size of the switching volume, i.e., the region of the GST layer that undergoes amorphous to crystal transformations. For binary switching, the active volume is switched, reversibly, between completely amorphous and completely crystalline states; for multilevel storage, partial amorphization or partial crystallization of the active volume is required.

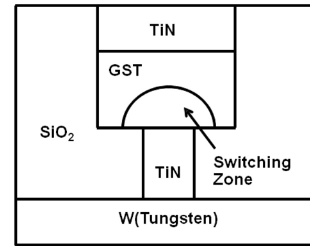

FIGURE 1. Schematic of a typical PCM "mushroom" cell design showing the dome-shaped switching zone (active volume) in the GST layer.

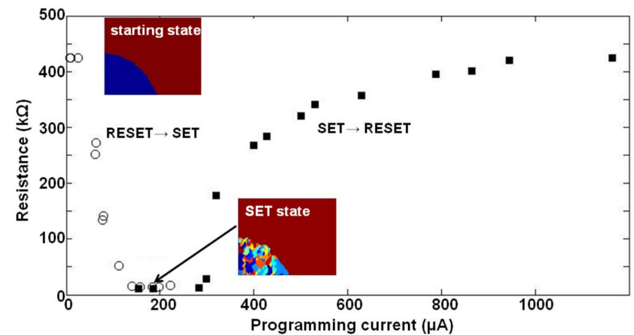

FIGURE 2. Computational simulation of the characteristic resistance-current "U" curve, in this case for a PCM cell of the type shown in Fig. 1 (with a bottom heater electrode of 200 nm diameter and a GST region of 400 × 150 nm). Also shown (inset) is the amorphous starting (reset) state (blue region amorphous, brown region crystallized) corresponding to the far left of the U curve, and the fully recrystallized (set) state (each different color corresponds to a different crystallite grain).

The capability for multilevel storage can perhaps be understood most easily using the so-called "U" curve relating cell resistance to programming current, an example of which is shown in Fig. 2. Starting on the left hand side of the "U," the cell is in the amorphous high resistance ("reset") state and increasing the amplitude of the (pulsed) programming current reduces the cell resistance, due to the onset of crystallization (of course the programming voltage also needs to be above the threshold voltage for conduction in the amorphous state - see [12]). When the cell is fully crystallized the resistance reaches its minimum value ("set" state) at the bottom of the "U." Upon further increasing the programming current the cell begins to re-amorphize until, at the far right of the "U," the cell is fully re-amorphized. Multilevel storage can thus be programmed into the phase-change cell by varying the programming current to give intermediate resistance states lying between the top and bottom of the "U" curve. It is possible to use either the left-hand or right-hand side of the "U" curve to provide a multilevel capability, but the right-hand side is more commonly used since it produces more reliable (i.e., repeatable) results [13], and it is this approach that is used in this paper.

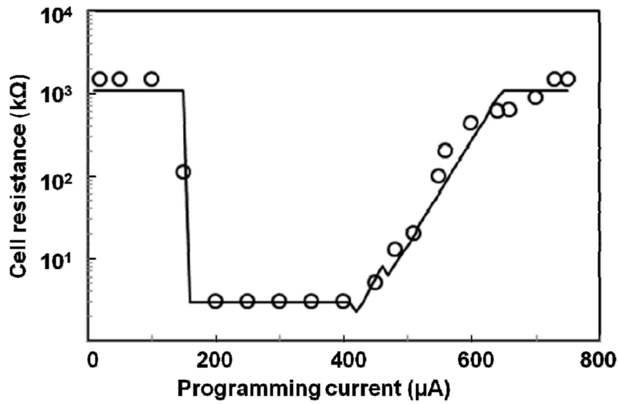

FIGURE 3. Experimental R-I curve (circles–from [17]) and (solid line) as simulated by SPICE model.

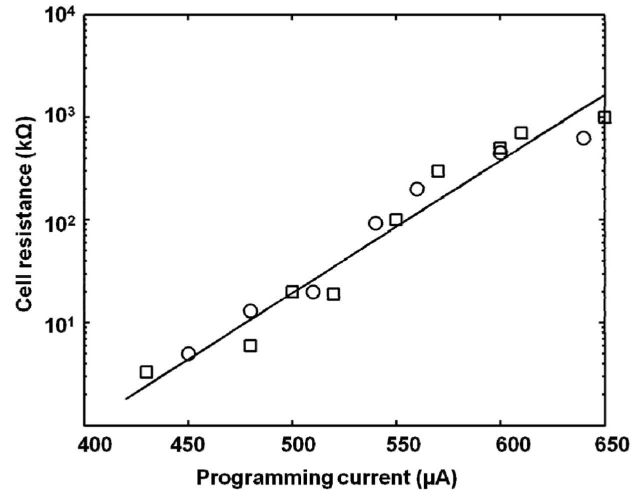

FIGURE 4. Cell resistance as a function of programming current on the right-hand side of the "U" curve taken from experiment (circles from [17] and squares from [29]) and (solid line) according to the relationship in (2).

The "U" curve of Fig. 2 was generated by computer simulation of the response of a "mushroom" type phase-change cell of the form shown in Fig. 1 for the case of a 200 nm diameter bottom (heater) electrode and a 400 nm x 150 nm thick GST layer. The phase-distribution of the GST layer is shown inset for both the high-resistance starting amorphous state (to write the starting amorphous dome a voltage pulse of 2.5 V amplitude, 20 ns duration and fast fall-time was used) and for the low-resistance, fully-recrystallized state (written with 1.5 V amplitude, 100 ns duration pulse); these two states (i.e., fully amorphous and fully crystalline) correspond to those used in binary storage. For such simulations of Fig. 1 a comprehensive physical model for the electrical, thermal and phase-transformation processes at work in the PCM cell was used (this physical model and its associated material parameters has been described extensively in previous publications (see [12], [14], and [15]), to which the reader is referred for further details). However, for this paper, as already discussed in §I, we are concerned with the development of a realistic PCM *device model* (in SPICE) that incorporates multilevel capabilities and the effects of resistance (and threshold voltage) drift. Such a device model should of course provide results in good agreement with both physical models and experimental data, which, as we show below, is indeed the case for the SPICE-based device model described herein.

The capability for multilevel storage in phase change memories has been known for some time, and was demonstrated using as many as 16-states per cell in both electrical and optical phase- change memories by Ovshinsky [16] some 10 years ago. A typical experimental R-I "U" curve, taken from the work of Ventrice *et al.* [17] is shown in Fig. 3; here, the device geometry was also of the "mushroom" cell type and the critical dimensions of the cell (electrode diameter, GST thickness etc.) were similar to those used in the computational simulations of Fig. 2, with which there is good general agreement. Over the right-hand-side of the "U" curve, the region of interest for multilevel applications, the relationship between the programming current amplitude I_p (in μA) and the resistance R_{cell} (in kΩ) of the phase change cell can be approximated by the simple equation

$$R_{cell} = R_{min}^{\beta\,(I_p - I_0)} \qquad (2)$$

where I_0 is the programming current for minimum resistance R_{min} (in kΩ) and β is a constant. A plot of (2) is shown in Fig. 4 (for the case R_{min} = 3kΩ, I_0 = 400 μA and β = 0.027) where it is compared to experimental results from [17] and [18] where good agreement is seen. The relationship of the form of (2) is therefore used in this work to program a particular cell into one of a number of multilevel resistance states.

While programming phase change cells into multiple resistance levels is relatively straightforward, as already mentioned above the programmed resistance is observed to drift with time, as described by (1). The origin of this drift has been primarily explained in the literature by two different mechanisms: (ii) stress release in the amorphous phase due to the build up of hydrostatic pressure during the reset process [6], [9] and (ii) a structural relaxation process involving atomic rearrangement of the amorphous network and associated changes in the band structure [8], [10], [18]–[20]. While there is still ongoing discussion as to which of these mechanisms is actually responsible for the observed drift, the adverse effects of resistance drift on multilevel storage are clear and potentially quite severe. A programmed resistance state will exhibit a different resistance at a later time, leading to the potential of readout errors and limiting the number of states that can be used and/or length of time a cell can be left without re-programming. Furthermore, as already pointed out in §I (and shown for example in Fig. 5), superimposed on the resistance drift described by (1) there is also a stochastic variation on short (second) time scales. As a result the read-resistance of a programmed multilevel state may go up or down when read events are closely spaced (∼ seconds apart).

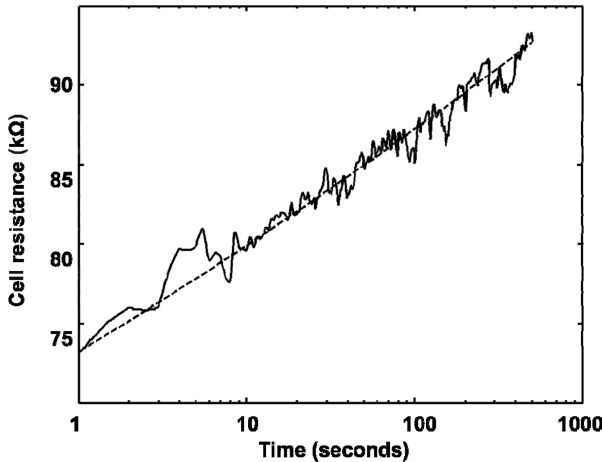

FIGURE 5. Example of the drift of cell resistance with time for a cell programmed into the (here partially) amorphous state. The solid line shows experimental results taken from [11] in which the stochastic nature of the drift on short-time scales is evident. The dashed line shows the drift according to (1), with a drift factor ν_R in this case of 0.038.

This stochastic short-term nature of the resistance drift is also included in the SPICE model presented here.

In addition to the drift of resistance, the threshold switching voltage for phase change cells is also observed to drift [6]–[8]. The threshold switching voltage is the voltage that needs to be applied to an amorphous cell to switch it into the so-called "on" state. Above the threshold voltage the conductivity of the amorphous phase suddenly increases and sufficient current can then be driven through the cell to instigate Joule heating and crystallization. Below the threshold voltage the amorphous phase has a very small conductivity and without the threshold effect extremely large (and impractical) voltages would be needed to force enough current through the cell to induce crystallization. Thus, the threshold voltage is also a critical parameter for operation of a phase-change cell, and its variation with time should also be included in any realistic simulation. Experimental measurements by Ielmini *et al.* [6] of the drift of threshold voltage, V_T, found that it was closely correlated to the observed resistance drift. Indeed, the variation of V_T with time t_{off} after the end of the programming pulse could be expressed as

$$V_T = V_{T0} + \Delta V_T \left({}^{t_{off}}\!/_{t_0}\right)^{\nu_0} \quad (3)$$

where V_{T0} and ΔV_T and t_0 are constants and ν_0 characterizes the rate of drift and gives the slope of the straight line obtained when $\log(V_T - V_{T0})$ is plotted versus $\log(t)$. Ielmini *et al.* [6] found that, for any individual cell, the drift exponents for both R and V_T were almost identical. The facility for threshold voltage drift according to (3) is therefore included in the SPICE model presented here - see §III - but it should be noted that (3) only applies after a short transient "recovery time" (of around 30 ns) from the end of the programming pulse. It should also be pointed out that, in drift measurements carried out over nine decades of time, Karpov *et al.* [7] found a slightly different behavior for threshold voltage drift that suggested a logarithmic time dependence. The reasons for this difference are not clear, and in any case it would be a simple matter to modify the SPICE models presented here to include a logarithmic rather than power law dependence of V_T with time.

III. MODELING OF MULTILEVEL PHASE-CHANGE MEMORIES USING SPICE

It is clear from the experimental results presented in the literature (see [6]–[11], [18]–[20]) and the discussions above that the drift of both resistance and threshold voltage appear to be fundamental and universal properties of the amorphous or partially amorphous phase in PCMs (at least those fabricated with the commonly used chalcogenide alloys), and that such drifts have a most important role to play in the achievement of reliable multilevel operation. Models for phase-change memory performance should therefore include these drift effects in a realistic way so that circuit and systems designers can assess the likely performance of multilevel PCMs in a variety of potential applications - and this is the aim of the SPICE model developed in this section.

Several authors have published SPICE type models for multilevel PCM simulations, but none have to our knowledge included the all important drift effects. Wei *et al.* [21], for example, developed an HSPICE macromodel for binary and multilevel storage in PCM cells. In Wei's model the multilevel capability was achieved using the left-hand side of the "U" curve and by increasing the width of the set pulse at constant current amplitude. A good correspondence between experimental and simulated "U" curves was obtained, but no simulated or experimental data on drift was given. Lee *et al.* [22] published a compact HSPICE macromodel for resistive memories, primarily for single bit cells but also extendable to multilevel operation. An aim of their model was to use the minimum number of circuit elements to improve simulation speeds. Again, the multilevel capability was achieved by using variable width current pulses and drift effects were not included. Ventrice *et al.* [17] proposed a compact model for multilevel applications based on a voltage controlled voltage source (VCVS) to model the basic I-V characteristic of the cell, an equivalent thermal circuit to compute the cell temperature and a time-integrating circuit to estimate the volume fraction of crystallized material. The model was used to simulate the cell resistance for programming from the reset state with increasing current pulse amplitudes, and good agreement with measurements on real devices was obtained. Although Ventrice's model is extendable to multilevel simulation, no (simulated or experimental) multilevel results were presented and drift was again not included. Liao *et al.* [23] allowed for partial crystallization in a PCM model implemented in HSPICE using Verilog-A. Crystal fraction was determined using RC circuits with a voltage controlled resistor and capacitor, and a linear relationship between crystallized fraction and cell resistance was used. With appropriate calibration their model successfully

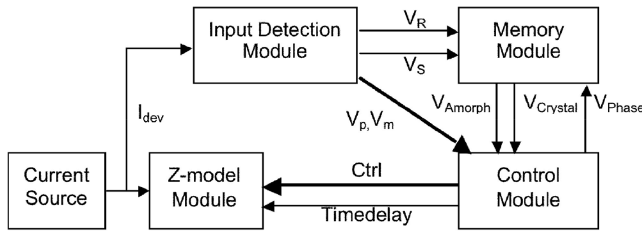

FIGURE 6. Block diagram of the multilevel PCM SPICE model incorporating drift effects.

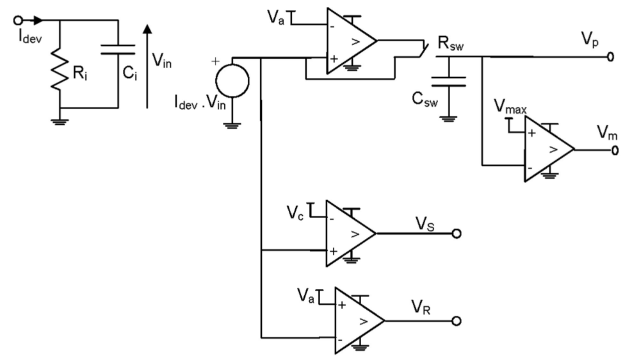

FIGURE 7. Circuit details for the input detection module.

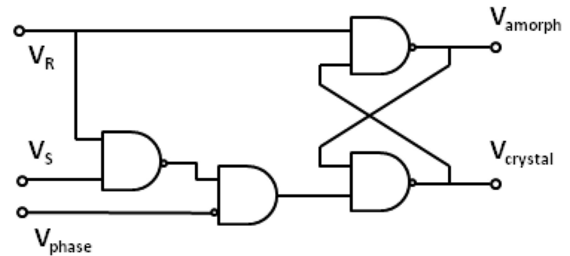

FIGURE 8. Circuit details for the memory module.

simulated the "U" curves for test cells. Their model is also capable of multilevel simulations, although no great detail of such simulations was given and of course the drift effect was not included. Interestingly Kwong *et al.* [24] introduced intermediate resistance levels also in a voltage controlled resistor circuit model for PCM operation, but in their case this was to model the *decrease* in stored resistance value for a PCM cell over very long durations (years) that result from the long-term crystallization of amorphous (reset) cells and affects data retention lifetimes, rather than the capability and reliability of multilevel storage. Finally, a paper by Jo *et al.* [25] reported on a compact Verilog-A model for multilevel cells. Programming into either partial set (i.e., the left hand side of the "U" curve) or partial reset (i.e., the right hand side of the "U") by variable amplitude current pulses was simulated, but drift effects were not included.

To enable a proper simulation of multilevel storage in phase change cells, including the all important drift effects, we have developed a realistic SPICE model shown in block diagram form in Fig. 6. The model shares some features with a single-bit PCM SPICE model previously published by us and based on a simple switchable two-phase resistance, where the selected phase was determined by the detected amplitude and duration of the programming current pulse [26], [27]. The new model of Fig. 6 is far more comprehensive and includes the capability for simulating I-V curves, R-I curves, multilevel resistance states, resistance drift and threshold voltage drift effects, together with the stochastic nature of drift observed for short time scales. Referring to Fig. 6, the model comprises four major sub-blocks, namely an *input detection module*, *Z-model module*, *memory module* and *control module*. The function of each of these is described briefly below. Note that the current source circuit in Fig. 6 provides the input signals for the PCM cell and comprises simply of a set of program and read current generators.

The input detection module, shown in Fig. 7, detects the input programming or read current pulse, as I_{dev}, applied to the PCM device (cell) and generates as its output an appropriate input voltage for the memory module, in relation to the voltages, V_a or V_c (defined in Table 1). For conventional binary operation, the input detection module outputs two voltage states, V_S and V_R, corresponding to fully crystallized and partially /fully amorphized states respectively, along with a voltage output (V_m) that sets the amorphous resistance value. For multilevel operation the input detection module additionally detects the intermediate programming current amplitudes and outputs a voltage (V_p) for the appropriate partially amorphous ("un-drifted") resistance value.

The memory module, shown in Fig. 8, uses the voltages V_S and V_R from the input detection module to select, via the Z-model module, the programmed state of the cell as crystalline or amorphous / partially amorphous. During static I-V simulations, a feedback signal from the control module, V_{phase}, also switches the internal memory to the crystalline state.

The Z-model module, shown in Fig. 9, provides the final PCM cell resistance appropriate to the programming conditions and to any time delay between programming and reading. The values of V_{vR}, V_t and V_{Ram0} in the Z-model module (as supplied by the control module shown in Fig. 10) provide for the variation of the programmed amorphous (or partially amorphous) resistance according to (1) and the variation of the threshold voltage as described by (3).

A. MULTILEVEL RESISTANCE STATES

For the simulation of multilevel operation, four different amplitude (but fixed-duration) programming current pulses are fed into the input detection module which converts them using an RC integrator (see Fig. 7) to a voltage source having a value equivalent to the input "energy." The output of the RC integrator feeds a number of parallel-connected comparators that generate output voltages corresponding to a fully crystalline state (V_S), and amorphous/partially amorphous states (V_R and V_m, or V_p). V_S and V_R are used by the memory circuit of Fig. 8 to generate the requisite outputs $V_{crystal}$ or

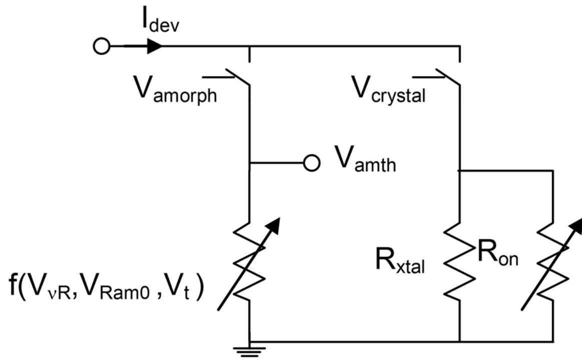

FIGURE 9. Circuit details for the Z-model module.

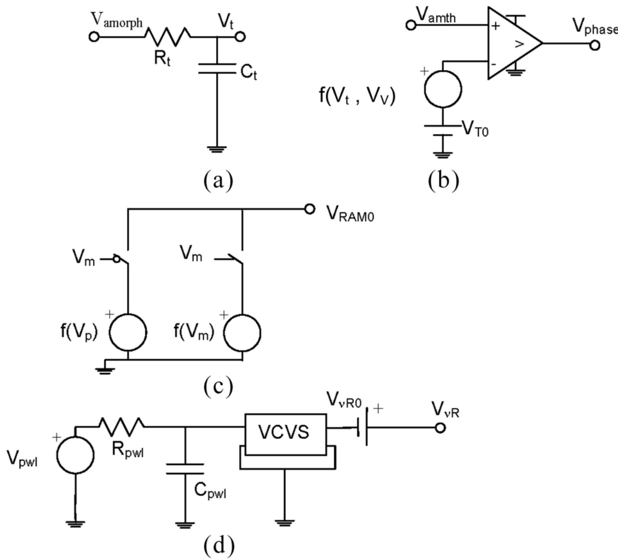

FIGURE 10. Control module showing the circuits for (a) simulation of the time delay (between programming and reading), (b) simulation of the drift of the threshold voltage, (c) the selection of multilevel "un-drifted" resistance states, and (d) simulation of the stochastic nature of the resistance drift.

V_{amorph}, whereas V_m, and V_p are used to select the "un-drifted" resistance (V_{Ram0}) of the amorphous states via the amorphous control circuit of Fig. 10(c). Finally the appropriate PCM resistance, including drift effects, is selected by the Z-model (of Fig. 9) using switches driven by the output from the memory module.

B. MODELING RESISTANCE DRIFT

The resistance drift is modeled over time within the Z-model circuit of Fig. 9. The "un-drifted" resistance signal [V_{Ram0} from Fig 10(c)] is varied through an Algorithmic Behavioural Module (ABM) by the time delay V_t [defined in the control circuit of Fig. 10(a)] and by the drift factor ν_R defined in the ABM as the voltage $V_{\nu R}$ - see Fig. 9. The "drifted" device uses the relationship of (1).

C. MODELING THRESHOLD VOLTAGE DRIFT

The threshold voltage drift circuit is shown in Fig. 10(b), where the threshold voltage signal *(*V_{amth}*)* from the Z-model

TABLE 1. Circuit parameters used in the spice model.

Parameter	Parameter name	Parameter value
$R_i.C_i$	Input time constant (see Fig. 7)	10 ns
$R_{sw}.C_{sw}$	Clamping time constant (see Fig. 7)	100 ns
V_a	Full amorphous energy equivalent (see Fig. 7)	0.41 V
V_c	Crystalline energy equivalent (see Fig. 7)	0.15 V
$R_{crystal}$	Nominal crystalline resistance (see Fig. 9)	3k Ω
R_{on}	Secondary crystalline resistance (see Fig. 9)	3k Ω
$R_t.C_t$	Time control time constant (see Fig. 10(a))	to 2M s
V_{T0}	Undrifted threshold voltage (see Fig. 10(b))	0.46 V
$R_{pwl}.C_{pwl}$	Stochastic filter time constant (see Fig. 10(d))	625 s
G	VCVS attenuation (see Fig. 10(d))	0.0035 to 0.007
$V_{\nu R0}$	Stochastic resistance drift factor (see Fig. 10(d))	0.02 to 0.11

is compared to the "un-drifted" threshold voltage (V_{T0}) added to voltage *(*V_t*)* dependent on the time delay and a voltage (V_V) representing the threshold voltage drift factor (ν_0). If, during a programming pulse, the programming voltage exceeds the drifted threshold (and the current is sufficiently high – see Fig. 3), the state of the PCM is changed to crystalline.

D. MODELING THE STOCHASTIC NATURE OF RESISTANCE DRIFT

To model the stochastic nature of the resistance drift the control circuit of Fig. 10(d) is used, adapted from a circuit design by Hageman [28]. Here a piecewise linear signal source *(*V_{pwl}*)* references a text file of a series of randomly generated voltages defined over a specific time range and interval. The circuit elements R_{pwl} and C_{pwl} together with a VCVS (voltage-controlled-voltage-source) condition the output of the piecewise source. The VCVS output is then added to a DC voltage *(*$V_{\nu R0}$*)*, representing the resistance drift factor ν_R, to form the required stochastic resistance drift *(*$V_{\nu R}$*)*, which then feeds into the ABM in Fig. 9.

IV. RESULTS

The above model has been used to simulate the performance of a typical PCM cell for use in multilevel storage applications and the results compared to published data from practical devices [6], [11], [17], [29]–[31]. Details of the various parameters used in the simulations are given in Table 1.

The simulated (static) current-voltage characteristic for the device is shown in Fig. 11. This is obtained in the simulation by applying a ramped current input and plotting this current against the voltage across the input to the Z-model module of Fig. 9. It can be seen that the cell remains in the "off" state until the threshold voltage is reached (1.2V in this case), whereafter it switches to the conducting "on" state and then further increases in the input signal put the cell into the crystalline (set) state where it remains when the current is removed. Also shown in Fig. 11 are experimental

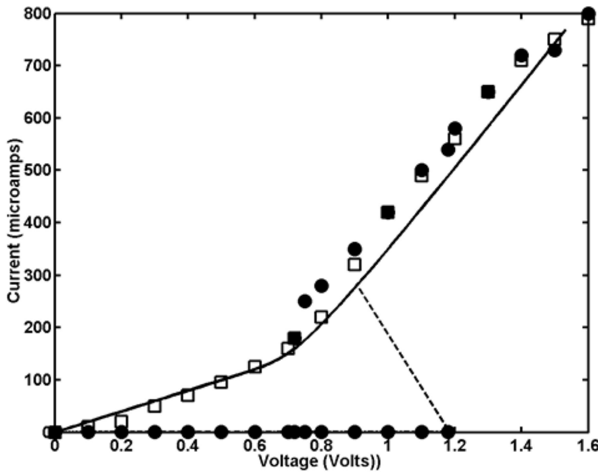

FIGURE 11. Static current-voltage characteristics simulated by the model (solid line for the crystalline phase, dashed line for the amorphous phase) and compared to experimental results (taken from [6]—circle symbols for the amorphous phase, square symbols for the crystalline phase).

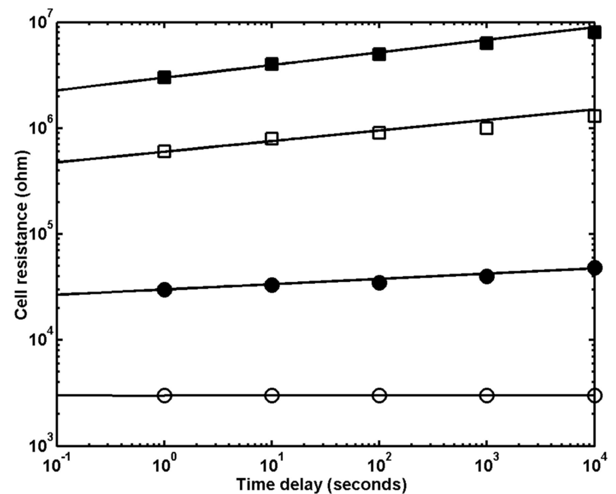

FIGURE 13. Simulated drift of resistance for a cell programmed into four different resistance levels (solid lines). Also shown (symbols) are experimental results taken from [30]. Note that the lowest resistance level is for a fully crystalline cell, which does not exhibit drift.

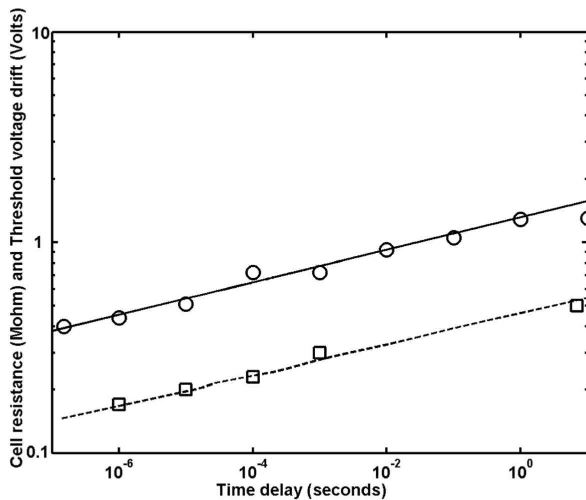

FIGURE 12. Simulated drift of resistance (solid line) and threshold voltage in the form V_T–V_{T0} (dashed line) compared to experimental measurements (taken from [6]—circles show resistance drift, squares show threshold voltage drift).

results from [6], with which the simulated results are in good agreement.

Next we simulate the all important drift phenomenon that is experimentally observed for both the programmed resistance and the threshold voltage. The resistance drift is simulated by programming the cell into the reset or partially-reset state and then reading the cell resistance after a variable time delay t_{off} [set by the circuit of Fig. 10(a)] while varying, as explained in the previous section, the resistance using the ABM in the circuit of Fig. 9. Results are shown in Fig. 12, for a ν_R factor of 0.077 and R_0 = 380 kΩ, over eight decades of time delay, where they are also compared to experimental results from [6] and again good agreement is obtained. Also shown in Fig. 12 are simulated and experimental (again from [6]) results for the drift of threshold voltage (in the form V_T - V_{T0}) with the time t_{off} after programming the device into the reset state; these simulated and experimental results also agree well over eight decades of time. As explained in §III above, the circuit of Fig. 10(b) simulates the drift by incorporating a voltage source implementing the relationship of (3), in this case with the parameters ν_T, V_{T0} and ΔV_T of 0.074, 0.55V, 0.46V.

Combining the drift models of §III.B and §III.C with the multilevel capability explained §III.A enables a realistic simulation of the performance of PCMs in multibit applications. The existence of drift will impact on the selection of the intermediate resistance values and/or the time after programming that a multilevel cell can be left before it needs to be reprogrammed to avoid read errors. Although the model is extendable to an arbitrary number of resistance levels, as an example we here use four (one "set" resistance and three partially "reset") programmed resistances, so representing a 2-bit (4-level) memory cell. The intermediate resistance levels are programmed according to the current-resistance relationship in (2), and then each level is read at a time t_{off} (from 0.1s to 10,000s) after programming has been completed. The selection of the intermediate resistance values was chosen to allow good separation of the final (drifted) resistances, and to allow comparison to measurements on real devices (taken from [30]). The results are shown in Fig. 13 where it can be seen that very good agreement is obtained between simulated and real devices.

As shown in Fig. 13, the drift factor ν_R is known to increase with increasing resistance, in this case going from zero for the 3kΩ "set" state to 0.12 for the reset state with an initial (in this case at 1 second after programming) value of 3 MΩ. Indeed, experimental studies have shown that the resistance drift factor ν_R increases both with increasing programmed resistance and with decreasing read current

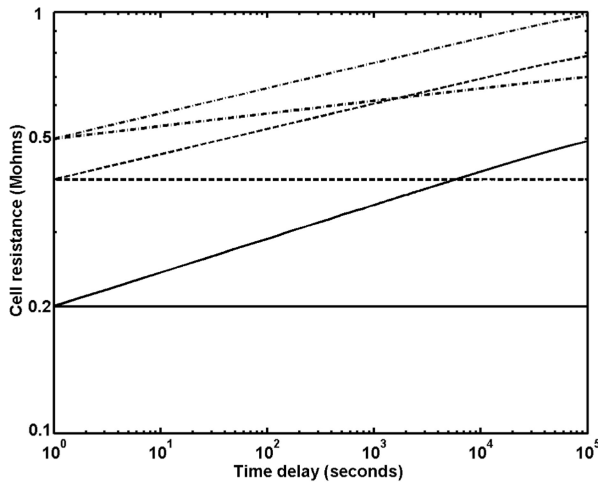

FIGURE 14. Simulated drift of resistance for three partially amorphous cell states with starting resistances of 200 kΩ (solid line), 400 kΩ (dashed line), and 500 kΩ (dash-dot line). Two curves for each resistance state are shown to illustrate the effects of the statistical spread of the drift factor ν_R experimentally observed in real cells (see [8]). Note that the potential for overlap of resistance states, in this case after only a few thousand seconds, is clear.

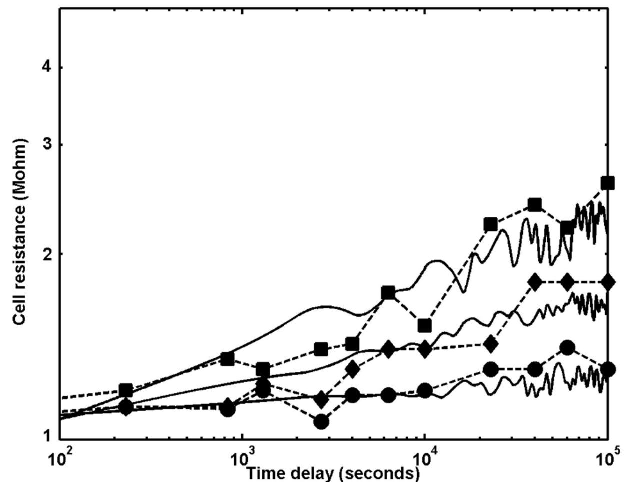

FIGURE 15. Simulated (solid lines) resistance drift, including the short-term stochastic variation of drift, for three different cells each with an initial programmed resistance around 1 MΩ. Also shown (symbols) are experimental measurements taken from [31].

amplitude [8], [19]. In addition there is a statistical spread of observed drift factors between program-read measurement cycles for any individual cell, and a statistical spread between cells (explained in [8], [19] as a result of the statistical fluctuations of defect annihilations). Thus, within any real PCM device there is expected to be a potentially large variation of drift behavior from programming cycle to programming cycle and from cell to cell. This can be captured in our model by using a suitable range of resistance drift factors in the ABM of Fig. 9 (and these drift factors could be linked to the initial resistance state of the cell to generate appropriate values for intermediate states, such as those shown in Fig. 13). An example is shown in Fig. 14 using the minimum and maximum values of ν_R observed for a real device programmed into multilevel states [8]. The results show clearly the potential problem of level intermixing due to drift.

Next, we simulate the stochastic nature (with time) of resistance drift. As outlined in §III.D this stochastic behavior can be incorporated into the SPICE model of the PCM by the piecewise linear voltage source in Fig. 10(d). As an example we show in Fig. 15 the time evolution of resistance for three different PCM cells each with an initial programmed resistance of around 1 MΩ, but each with a different ν_R factor (reflecting the statistical variations of drift from cell to cell) and each showing a stochastic time variation of resistance - put simply the drift is “noisy”. Also shown in the figure are experimental resistance measurements for the three different cells (taken from [31]) which show clearly the noisy nature of the drift and which agree well with the simulations.

Finally, we note that the value of the “un-drifted” threshold voltage (V_{T0} in (3)) also depends on the programmed resistance of the PCM cell [29] (i.e., it is not a constant). Thus we note that this dependence can also be included in our model by simple modification of the threshold voltage module of Fig. 10(b).

V. CONCLUSIONS

A comprehensive SPICE model for simulation of the performance of multilevel phase change memories has been developed, incorporating the phenomena of resistance and threshold voltage drift that are experimentally observed in the amorphous and partially amorphous phase. In addition the model includes the stochastic nature of resistance drift that is observed over relatively short time scales, and the capability for including statistical fluctuations in drift factors that are experimentally observed from programming cycle to programming cycle and from cell to cell. A detailed comparison has been made between simulated results and published experimental results for multilevel programming, resistance and threshold voltage drift and stochastic effects, and the agreement is very good. The model presented in this paper therefore provides circuit and systems designers with a realistic way to assess the likely performance of multilevel PCMs in a variety of potential applications, such as for conventional Flash and DRAM replacements or for the “new” format of storage-class memory.

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