

Integratable all-photonic nonvolatile multi-level memory

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Implementing on-chip nonvolatile photonic memories has been a long-term, yet elusive goal. Photonic data storage would dramatically improve performance in existing computing architectures¹ by reducing latencies associated with electrical memories² and potentially eliminating optoelectronic conversions³. Furthermore, multi-level photonic memories with random access would allow for leveraging even greater computational capability^{4–6}. However, photonic memories^{3,7–10} have thus far been volatile. Herein, we demonstrate a robust, nonvolatile, all-photonic memory based on phase-change materials. By utilizing optical near-field effects, we realize bit storage of up to eight levels in a single device that readily switches between intermediate states. Our on-chip memory cells feature single shot read-out and switching energies as low as 13.4pJ at speeds approaching 1GHz. We show that individual memory elements can be addressed using a wavelength multiplexing scheme. Our multi-level, multi-bit devices provide a pathway towards eliminating the von-Neumann bottleneck and portend a new paradigm in all-photonic memory and non-conventional computing.

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The advent of photonic technologies, in particular in the area of optical signaling, coupled with advances made in nanofabrication capabilities has created a growing need for practical all-photonic memories^{3,7-10}. Such memories are essential to supercharge computational performance in serial computers by speeding up the von-Neumann bottleneck, i.e. the information traffic jam between the processor and the memory. This bottleneck limits the speed of almost all processors today; it has already led to the introduction of multicore processor architectures and drives the search for viable on-chip optical interconnects. However, shuttling information optically from the processor to electronic memories is presently not efficient because electrical signals have to be converted to optical ones and vice-versa. Instead, information transfer and storage exclusively by optical means is highly desirable because of the inherently large bandwidth^{1,3}, low residual cross-talk and high speed of optical information transfer. On a chip this has been challenging to achieve because practical photonic memories would need to retain information for long periods of time and require full-integration with the ancillary electronic circuitry, thus requiring compatibility with semiconductor processing¹¹.

Ideal candidates for all-optical memories are phase-change materials (PCMs), already the subject of intense research and development over the last decade, but in the context of electronic memories¹²⁻¹⁴. A striking and functional feature of these materials is the high contrast between the crystalline and amorphous phase of both their electrical and optical properties^{15,16}. In particular, chalcogenide-based PCMs have the ability to switch between these two states in response to appropriate heat stimuli (crystallization) or melt-quenching processes (amorphization)¹⁷. These PCMs, mainly tellurides and antimonides, can be switched on a sub-nanosecond timescale^{15,18} with high reproducibility which enables ultra-fast operation over switching cycles up to 10^{12} times^{14,16} using current-generation materials (with new and improved materials, such as the so-called phase-change super-lattice materials¹⁹, expected to deliver even better performance in the future). In addition, at normal operating temperatures the states are highly stable for years^{15,20}, a key requirement for a truly nonvolatile memory. These beneficial properties of PCMs have already led to prominent commercial applications in optical data storage such as rewritable optical discs (in DVD and Blu-ray formats)²¹ and more recently for use in optoelectronic modulation and display applications in the visible spectrum²².

Many PCMs show significant change in refractive index in the visible and even larger changes in the near-infrared wavelength regime, which is the spectral region of choice for telecommunication applications^{23–26}. Here, by using such nanoscale PCMs embedded in nanophotonic circuits, we demonstrate that fast and repeatable all-optical, multi-level, multi-bit, nonvolatile memory operations, with wavelength division multiplexed (WDM) access, can be achieved on a chip at telecommunications wavelengths compatible with on-chip optical interconnects. In contrast to free-space optical implementations where PCM cells are switched with a focused laser in the far-field, our devices are operated in the optical near-field in analogy to plasmonic devices. Therefore our waveguide integrated memory cells are not restricted in size by the diffraction limit of the input light and can hence be miniaturized to nanoscale dimensions. We employ the well-studied alloy $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (GST) because of its data retention capabilities^{15,17} and high state discrimination²³ down to nanoscale cell sizes, which enables dense packaging and low-power memory switching. In our devices, data is stored in a nanoscale GST cell placed directly on top of a nanophotonic waveguide. Both writing into the memory cell and read-out of the stored information is carried out via evanescent coupling to the phase-change material and is thus not subject to the diffraction limit; because this is done directly within the waveguide using nanosecond optical pulses, our approach provides a promising route towards fast all-optical data storage in photonic circuits.

The geometry of our memory cell and the operating principle is shown schematically in Fig. 1a. We store information in the GST (yellow region) by employing evanescent coupling between light travelling along the waveguide and the GST element. This interaction results in the absorption of optical power due to the non-vanishing complex refractive index of GST. As illustrated in Fig. 1b, the crystalline state (which we label Level 0) exhibits higher attenuation and thus less optical transmission than the amorphous state (which we assign to Level 1). Therefore, stored data is encoded in the amount of light transmitted through (along) the waveguide (i.e. exiting the end of the waveguide) and can be read-out with low-power optical pulses (red trace in Fig. 1a). The phase state of the memory element influences the optical properties of the propagating light field and therefore the waveguide mode profile, as illustrated for the simulated transverse-electric (TE) mode in Fig. 1d. In the crystalline state, the phase-change material is more absorptive, thus pulling the light towards the GST cell, and leading to

strong attenuation of the passing optical signal. In the amorphous phase, on the other hand, the absorption is reduced and therefore the GST film does not attenuate the waveguide transmission to the same degree. Writing into the memory or erasing the stored information is achieved by inducing a phase-transition with a more intense light pulse (blue trace, *Write/Erase*). If the energy absorbed by the GST is high enough to heat it up to its transition temperature, these pulses can initiate either amorphization (*Write*) or crystallization (*Erase*). For amorphization, the GST is melted and then cooled down rapidly to preserve this disordered state. On the other hand, heating the GST above the crystallization temperature (but below the melting temperature) for a few nanoseconds¹⁵ enables recovery of the atomic ordering and thus crystallization. Thus, our scheme is the photonic equivalent of resistive memories, whereby by transmission (equivalent to conduction) is modulated by varying the absorptive state (conductivity) of the material – and different from the phenomenon employed in conventional optical storage (where reflectivity is modulated). In this letter we describe three distinct and key aspects of our devices, viz. i) an all photonic nonvolatile memory element, ii) addressing several disjoint elements using wavelength multiplexing to deliver multi-bit access and finally, iii) show how multi-levels of memory can be stored in a single memory cell including single shot read and write.

The fabricated on-chip memory elements are operated by using an optical pump/probe setup as described in the methods section and the supplementary information. Both writing and erasing of the memory is performed with nanosecond light pulses that are generated off-chip (for experimental expediency only) with an electro-optical modulator (EOM) and subsequently coupled into the on-chip waveguides. The read-out is performed both with sub-nanosecond readout pulses (500 ps, generated with the EOM) and with continuous wave (CW) light, in both cases with at least one order of magnitude less power compared to the *Write* pulse. To separate the read-out ($\lambda_{\text{probe}}=1570$ nm) from the *Write/Erase* pulses ($\lambda_{\text{pump}}=1560$ nm), a color-selective filter (Pritel TFA-1550) with a spectral extinction ratio in excess of 40 dB is used. Further suppression of the pump light is achieved by letting the pump and probe light-waves counter-propagate through the photonic circuitry.

In Fig. 2a the change in read-out transmission upon repeated switching between the crystalline (low transmission) and amorphous (high transmission) state of the GST is shown.

Each event that results in a change in transmission (we will call this “switching” henceforth) represents the single-shot read out of the state (Levels “0” or “1”). The results demonstrate unequivocal binary data storage in our photonic memory chips with good reversibility and high transmission contrast. As illustrated in Fig. 2b, the switching process is highly reproducible over fifty cycles with a measured confidence interval (shaded area) of $\pm 7.1\%$. The low-transmission state (Level 0) is initially prepared from the fully crystallized phase in such a way that reversibility of the operation is ensured (see methods section). On the other hand, the absolute transmission at Level 1 is determined by the employed switching energy, which defines the final level of amorphization, and the GST dimension along the waveguide, which defines the modulation depth. To ensure high transmission contrast between the amorphous and crystalline states we use in Fig. 2 a cell of 5 μm length; with this device we achieve a change in read-out transmission of 21 % using a single 100 ns write pulse of 533 pJ energy. Since the GST cell absorbs nearly 80.7 % of the pulse in the crystalline state (derived from a measured optical attenuation of -7.14 dB past the device), this corresponds to a switching energy of 430 pJ. Further demonstrations of binary operation were realized by employing devices with smaller GST lengths and lower *Write* pulse energy, as described in the supplementary material. In particular, a modulation depth up to 58.2 % and binary operation with pulses as short as 10 ns with switching energies of 13.4 pJ (See supplement S4) was achieved. While the data in Fig. 2 demonstrates the nonvolatility of our memory for several minutes (indicated by the time bar), in the supplementary material S8 we confirm that the phase-state is preserved over a much longer times, up to a period of at least three months. Indeed, extrapolating from the well-studied data retention properties of GST^{15,20} our all-optical memory can be expected to remain nonvolatile on a timescale of years.

In our devices, amorphous GST exhibits nearly five times lower optical attenuation compared to crystalline GST. This conveniently allows us to use pulses within the same energy range when switching back and forth between states: one pulse can initially induce amorphization while a second identical pulse will either keep the same state or partially crystallize the PCM device because the resulting Joule heating leads to lower temperatures for the second pulse compared to the first one (since the GST is in the amorphous phase after the

first pulse) and melting may not take place. For the *Erase* process to go back to Level 0, we use a train of consecutive pulses with gradually decreasing power as described in the methods section.

The optical switching of our memory element is further confirmed by high resolution transmission electron microscopy (HRTEM). We prepared devices in both the amorphous and crystalline phases using the optical switching processes outlined above. A thin lamella along direction of propagation in the waveguide was cut through the GST section for TEM imaging, as described in the methods section and the supplementary material. From the images, the deposited GST layer and the ITO layer can be seen, as indicated in Fig. 2c; the measured thickness for each layer is about 10 nm as expected from the deposition rates. The HRTEM image in Fig. 2c also clearly shows the crystalline phase written into (the GST element of) this device. To further illustrate the crystal order we show the Fourier transform of Fig. 2c in Fig. 2d, where the diffractogram reveals the features of cubic GST. The diffractogram of a device written into the amorphous state is shown in Fig. 2d, where the presence of only diffuse halos confirms amorphization (for an HRTEM image of a device in the amorphous state see the supplementary information).

Besides repeatability, speed is an integral part of all memory devices. In this context, the speed at which *Read*, *Write* and *Erase* operations can be achieved in a single memory element is important. In our photonics memory cell, the read-out relies on photon absorption because information is encoded in the amount of power transmitted through the waveguide. Hence, the read-out can be performed on picosecond time scales and is therefore not a crucial bottleneck in achieving high speed operation. On the other hand, *Write* and *Erase* are linked both to amorphization and crystallization times which are intrinsic properties of the GST-cell and have been reported to take place at picosecond¹⁸ (amorphization) and nanosecond to sub-nanosecond²⁷ (crystallization) timescales, respectively. In our case, the writing speed (amorphization) is the more stringent requirement since it determines how quickly information can be stored. As outlined above, here we were able to switch with pulses as short as 10 ns. To determine how fast our memory might be operated, we monitor the phase-transition by performing time-resolved measurements during optical switching. The observed transient behavior is presented in the supplementary material in Fig. S7 where we analyze the switching dynamics and the speed of the

PCM photonic memory. Besides the length of the *Write* pulse, the speed of the device is also limited by the post-excitation relaxation time (which we call dead time). For 700 ps write pulses we obtain an operation speed of 800 MHz (taking pulse length and dead time into account). Further details of this analysis are presented in Supplement S3 from which we expect that writing speeds of a few GHz can be achieved by using picosecond instead of nanosecond pulses²⁸.

We now take our memory concept a step further by illustrating how single-cell access in a multi-bit, multi-wavelength device can be realized. The simplicity of our all-optical memory approach, with a PCM storage element coupled evanescently to a waveguide, makes it fully compatible to on-chip nanophotonic circuitry, so allowing for easy integration and exploitation of a wide range of commonly used optical signal processing techniques such as WDM approaches. Here, we show a wavelength-multiplexed integrated multi-bit architecture with ultra-fast read-out and up to 10 dB modulation depth. Our approach relies on the wavelength-filtering property of on-chip optical cavities which enables wavelength selective addressing of individual, nonvolatile memory elements (wavelength selectivity via the use of optical cavities was demonstrated recently by Kuramochi et al.³ for volatile memories having a storage 'lifetime' in the nanosecond range; our device in contrast demonstrates this in a nonvolatile memory with a nominal lifetime counted in years.).

We demonstrate that three memory cells can be wavelength selectively operated (i.e. written, erased and read) through one single waveguide by embedding GST elements (of $1 \times 1 \mu\text{m}^2$ footprint) into three ring resonators coupled to the waveguide, as shown in Fig. 3a. Since cavity internal interference prevents off-resonance wavelengths from entering a ring, only light close to resonance can be used to switch or read-out the respective memory cell. Wavelength selective operation is thus made possible by slightly detuning the ring resonances which can, for example, be achieved by designing the ring radii differently. By doing so, we observe, as presented in Fig. 3b, groups of three clearly separated resonance peaks in the device transmission. To switch the individual memory cells we thus use laser pulses at 1560.1 nm, 1561.5 nm and 1563.35 nm, respectively. While *Write* is carried out with a single 10 ns pulse, repeatability is again ensured by performing *Erase* with a train of consecutive 50 ns pulses of

decreasing energy. In Fig. 3c the individual changes of the three resonances upon switching, a result of the modified refractive index of the GST element, are shown. The left panel demonstrates that the initial state is recovered after one *Write/Erase* cycle. The right panel clearly shows that each memory element can be addressed individually; the pulse on resonance leads to amorphization of the respective GST element, while the other memory cell is clearly unaffected. In Fig. 3d we further show that each memory entry can be read-out individually with 500 ps pulses, with a pulse energy of 0.48 ± 0.003 pJ. Here, pulses at three distinct wavelengths (1560.0 nm, 1561.45 nm and 1563.3 nm, respectively) are used to probe the cell transmission (and thus the memory entry) of the cavity at the respective wavelength. The readout pulses are red-detuned from the wavelength of the pump pulse onto the slope of the cavity resonance in order to maximize the read-out contrast upon switching. While we achieve a modulation depth of 3 dB upon switching each individual memory cell, the read-out level of the non-addressed memory elements does not change. In the supplementary material we further show that, with this approach, modulation depths exceeding 10 dB are possible.

Next, we discuss the potential of our optical cell for future high-density data storage by reducing the overall dimensions of the memory element and using multi-level access (i.e. storing multiple bits per memory element) in a single cell. The smallest realized memory element has a footprint of $0.25 \mu\text{m}^2$ (See the inset of Fig. S7a in the supplementary materials). We expect that even smaller cells could be operated in accordance with recent reports on electrical PCM-based devices^{14,29}. Here we show that our memory element does not only have a small footprint but is also capable of multi-level storage in a single cell, using simple but extremely effective write/erase and read techniques. Using optical *Write/Erase* pulses with varying pulse energy we are able to freely and reliably move between these intermediate levels with high repeatability. This multi-level operation relies on the freely accessible intermediate crystallographic states of the GST, i.e. states with a mixture of crystalline and amorphous regions. These mixed states exhibit optical transmission properties lying between those of the level 1 and level 0 shown in Fig. 1a. The number of additional memory levels can be defined by tailoring the degree of crystallization within a single cell. Such multi-level operation is demonstrated in Fig. 4a-c for four clearly distinct levels. The presented data is recorded in a $5 \mu\text{m}$ long PCM element, with each transition between levels being initiated by a single 100 ns light pulse. Four clearly

distinguishable levels are reached with pulses P_i of level-specific energies in the range 465 to 585 pJ (see figure caption for details). In Fig. 4a these levels were reached in a serial manner and subsequently the *Erase* operation was carried out from level 3. Furthermore, the same bit levels were also shown to be accessible in random order as shown in Fig. 4b; here the *Erase* operation (i.e. a return to level 0) was not only possible from the highest transmission state, but from any intermediate level as shown in Fig. 4c. These results demonstrate that both *Write* and *Erase* operations, to and from any level, are possible with high accuracy allowing a reliable multi-bit memory operation. This exciting aspect of our photonic memories is particularly attractive because such arbitrary transitions are very difficult to achieve in electronic memories employing phase change materials, where iterative write-and-erase algorithms involving multiple (typically 3 to 5) write/read/(re-write) cycles are needed to achieve a pre-defined level, adversely affecting the overall write speed and power consumption³⁰.

The number of possible levels in a memory cell is limited by the separation (difference in transmission) between the highest and lowest state and the required confidence interval of an intermediate level. The former can be increased by using either a larger memory cell or higher pulse energies. The confidence interval, on the other hand, is mainly limited by the minor variations in the switching and by the signal-to-noise ratio (SNR) of the read-out measurement. Therefore, the number of memory levels can be increased by just using a higher read-out power ensuring a better SNR (within limits). This is demonstrated in Fig. 4d, where we demonstrate 8 levels of state discrimination (i.e. 3 bits per cell) within a single photonic memory cell. Each level corresponds to a partial crystalline state, presenting a specific change in transmission by applying pulses with varying energies as presented in Fig. 4e. The individual levels are reached with pulses P_i of level-specific energies in the range 372 to 601 pJ (see figure caption for details). In this figure, it can also be observed that the difference between the transmissions of any two consecutive levels is much higher than the uncertainty marked by the color coded background. In Fig. 4d is also demonstrated that each level can be reached from both directions, i.e. with an amorphization as well as a crystallization step. This implies that any level is accessible from all others, with very accurate control of the transmission levels and remarkable repeatability (as seen by the accurate re-writing of levels 1 to 4 in Fig. 4d), just by applying the

appropriate *Write* or *Erase* pulse; such capabilities provide a huge leap forward in terms of functionality and will be crucial for the realization of practicable photonic memories..

Finally, we address another crucial aspect of data storage, i.e. energy consumption per bit. Since in our memory cell both writing and erasing rely on phase-transitions of the PCM, the switching energy is given by the amount of energy that is required to heat the GST above the melting (amorphization) or glass-transition (crystallization) temperature, respectively. Therefore, the energy consumption is directly related to the volume of the memory element and read-out contrast. This relationship between switching energy and read-out contrast is shown in Fig. 4e. In binary operation, we achieved a read-out contrast of 21% with 430 pJ switching energy (cf. Fig. 2). On the other hand, we measured switching energies as low as 13.4 pJ for a reduced contrast of 0.7% which still enabled clear distinction of the two levels (See supplement S4). In addition, we estimate that energy consumption can be improved up to one order of magnitude by operating the memory with sub-nanosecond instead of tens of nanosecond pulses. In our thermo-optical analysis in the supplementary information we observe that the portion of absorbed energy that gets lost due to thermal diffusion increases significantly with increasing pulse length. Therefore, shorter and more intense pulses are also beneficial in terms of energy requirement by quickly heating up the PCM to the required transition temperature while reducing thermal diffusion losses.

In this very first prototype of our photonic PCM-based memory, the energy consumption and speed achieved in our experiments compares well with pre-existing electrical counterparts. For example, current commercial PCM-based electrical memories (at the 45 nm node) typically require write pulses of 50 - 100 ns duration and read pulses of 10 ns (considerably longer than the 10ns/500ps write/read for our photonic memory), along with 5-10 pJ write energy (c.f. ~13 pJ here). Although research-level devices improve on such performance figures (e.g. 3.4pJ write energy and 20 ns write pulses in¹⁴), the performance of our photonic memories can also be further improved by operating them with shorter pulses and by moving to devices with smaller footprint, as well as through the development of new materials with faster and lower temperature switching. Higher signal to noise ratio to improve the read-out contrast could also be obtained with the use of optical cavities, which would also reduce switching energies as discussed theoretically by us previously²⁶. To reduce the device footprint, alternative architectures as for

example plasmonic antennas could be explored. Alternatively, scaling down is plausible by using photonic circuitry operating at shorter wavelengths (therefore, narrower waveguides) or by using phase-change materials with higher difference in refractive index in the C and L-band. This way, small devices will lead to reasonably good contrasts. While our multi-bit access is achieved with micro-ring resonators with relatively large footprint, alternative technologies such as ultra-compact on-chip optical multiplexer / demultiplexer^{31,32} can be employed for size reduction. In addition, optical cavities with smaller mode volume such as photonic crystal devices would localize the interaction volume of the optical mode with the memory element further and thus lead to a smaller system size for wavelength selective memory access.

In conclusion, we have demonstrated the first prototype of an integrated, all-photonic, truly-nonvolatile memory that provides multi-level (here 8 level) storage in a single cell along with multi-bit (here 3 bit) wavelength division multiplexed access (via a single waveguide). Our approach uses low-dimensional phase-change (GST) memory elements integrated with silicon nitride waveguides. The memory elements are switched between memory states by evanescent coupling to light travelling along such waveguides and are thus not restricted in size by the diffraction limit. Furthermore, we show the ability to switch readily and directly between the multiple memory levels, with accurate control of the readout signal and excellent repeatability (capabilities that require complex iteration based algorithms in electronic phase change memories). We also demonstrate the capability for fast (~500 ps), low power (~480 fJ), single shot readout of the memory state, along with repeated (x100) write/erase cycling while maintaining high readout contrast. Our hybrid phase change-photonic framework is fully scalable: large arrays of all-optical memory elements can be envisioned which are conveniently addressed, using WDM techniques, through on-chip waveguides; **such attributes are essential for the realization of a number of novel applications, including new forms of non-conventional (non-Von Neumann) computations^{33,34} and practical on-chip optical interconnects (although for the latter, an increased switching endurance beyond that currently achievable with GST would be beneficial).** These very first experimental results are not only promising, but demonstrate significantly more potential than existing integrated optical memories – high speed access, multi-level single shot write and read, wavelength selectivity as well as low power - and thus set the stage for further exciting new developments in phase change photonics.

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Author contributions:

All authors contributed substantially. WHPP and HB conceived, planned and supervised the project. CR and MS fabricated the samples, realized the reversible switching and multilevel measurements, the thermo-optical response and speed measurements. P.H. CDW and HB deposited and characterized the GST. D.W. and T.S. performed the TEM analysis of the specimen. All authors analyzed the data and helped write the manuscript.

Additional information

Supplementary information is available. Correspondence and requests for materials and devices should be addressed to W.H.P.P (wolfram.pernice@kit.edu) and H.B. (harish.bhaskaran@materials.ox.ac.uk).

Figure captions

Figure 1. Operation principle of the all-optical on-chip memory device. **a)** Information is stored in the phase-state of the GST section on top of the nanophotonic waveguide. Both reading and writing of the memory can be performed with ultra-short optical pulses since the guided light interacts with the GST by its evanescent field. In the read-out, data is encoded in the amount of optical transmission through (along) the waveguide since the two crystallographic states of GST exhibit a high contrast in optical absorption. **b)** As shown in the level scheme, less optical power is transmitted through the waveguide if GST is in the crystalline (Level 0) than in the amorphous state (Level 1). Memory is written (*Write*) and erased (*Erase*) with intensive optical pulses which initiate a phase-transition within the GST. **c)** Scanning-electron-microscope image of a fabricated device with a footprint of $0.4 \times 0.4 \mu\text{m}^2$. **d)** Waveguide cross section with simulated TE optical mode evanescently coupled to amorphous GST.

Figure 2. Reversible and reproducible single shot switching. **a)** Demonstration of binary memory operation between the crystalline (lower Level 0) and amorphous (upper Level 1) state of a $5 \mu\text{m}$ GST device with a total change in read-out transmission of 21 %. The *Write* step (blue) is initiated by a single 100 ns pulse while for the *Erase* step (red) a fixed sequence of six consecutive 100 ns pulses with decreasing powers is employed (see Methods section and Suppl. 3). Time scale is 1 min. **b)** Multiple repetition of the same switching cycle as in a). The dark and light shaded areas represent one and two standard deviations, respectively. **c)** Transmission electron microscope image of cross-section through a memory cell in the crystalline state. **d)** Fourier analysis of the TEM image for the memory device in the crystalline state from c), showing clear features of the ordered lattice structure. **e)** Fourier analysis of the TEM data from a device optically switched into the amorphous state with a pronounced halo expected for the amorphous phase.

Figure 3. A multi-bit, multi-wavelength architecture. **a)** SEM micrograph of the device under test. Light is coupled in and out of the on-chip circuitry by means of the focusing grating couplers at the lower left and right. The GST elements of $1 \times 1 \mu\text{m}^2$ footprint are embedded (dotted circles) within the (false-colored) ring resonators which are all separated from the central waveguide by a gap of 300 nm. Three different ring radii are used to ensure spectral separation of the cavity resonances. **b)** Therefore, in device transmission, groups of three distinct resonances, corresponding to the respectively colored rings, are observed. Using optical pulses close to resonance (indicated by the colored arrows), we address each cell selectively. **c)** Demonstrates the changes in transmission for an individual element after *Write/Erase* cycling (left panel) and that cells can be individually addressed, leaving other cells unaffected (right panel). **d)** Shows wavelength-selective readout of individual cells using 500 ps pulses. Switching of a

memory cell modifies exclusively the transmitted power of the pulse at the corresponding read-out wavelength. Each trace is normalized to its initial read-out level. The horizontal dotted lines indicate potential decision levels between the two states.

Figure 4. Multi-level operation of the all-photonic memory element. **a)** Four clearly distinguishable levels are reached with 100 ns *Write* pulses P_i of level-specific energy $E_{P1}=(465\pm13)$ pJ, $E_{P2}=(524\pm14)$ pJ and $E_{P3}=(585\pm14)$ pJ in a 5 μm GST device. The *Erase* step consists of a train of pulses with decreasing energy as described in methods section S4. Levels are shown to be accessible in **a)** consecutive or **b)** arbitrary ascending order by the respective *Write* pulses P_i . **c)** Each level can also be independently reached and erased. Scale bar in a)-c) is 20 s. **d)** Reducing the confidence interval of each level (shaded area) by increasing the read-out power by a factor of 10 enables to operate the same device as in a)-c) with eight levels. This also implied a renormalization in transmission that leads to different figures for the change in Read-out. In addition, it is shown that each level can be reached from a higher level by applying a partial *Erase*, denoted by R_{n-m} , which is described in the methods section S4. Therefore, each level can directly be accessed from any other level. The energies for the Pulses P_i are those leading to level i in subfigure e), following the same colour scheme ($E_{P1}=(372\pm12)$ pJ, $E_{P2}=(415\pm13)$ pJ, $E_{P3}=(465\pm13)$ pJ, $E_{P4}=(524\pm14)$ pJ, $E_{P5}=(561\pm14)$ pJ, $E_{P6}=(585\pm14)$ pJ and $E_{P7}=(601\pm15)$ pJ). **e)** Relation between used pulse energy, addressed level and corresponding change in read-out transmission for the *Write* operations used in d). Error bars show the uncertainty in the level attainability.

Methods

Device fabrication and static characterization

The photonic circuits are fabricated from 335 nm Si_3N_4 / 3350 nm SiO_2 wafers using a JEOL JBX-5500ZD 50 kV electron-beam lithography system. The structures are defined with Ma-N 2403 negative tone resist whose intrinsic surface roughness is reduced by a soft reflow process after the electron exposure. Subsequently, reactive ion etching (RIE) in CHF_3/O_2 is used to etch down 165 nm of Si_3N_4 (330 nm in case of the ring devices) followed by the complete removal of the remaining resist under O_2 plasma. All fabricated devices are designed with a waveguide width of 1.3 μm or 0.9 μm (ring devices).

The memory elements are fabricated by depositing GST and indium tin oxide (ITO) in a lift-off process. For this, a second electron-beam lithography step is carried out using positive tone PMMA resist at 8% concentration. We define rectangular openings on top of the waveguides using alignment to the previously written waveguide structures. Subsequently a 10 nm thin layer of GST is sputtered and capped with 10 nm of ITO to avoid oxidation. Finally, lift-off of the GST/ITO layers is done in hot acetone supported by soft sonication.

The overall transmission of the devices is measured before and after the GST deposition. By direct comparison the optical attenuation of the GST in both states is evaluated in cells of increasing length to determine the absorption coefficient per unit length. Exponential power decay with increasing length is obtained in good agreement with previously reported values²³.

Measurement principle and setup

Both setting and reading of our on-chip memory cell is performed directly on chip, i.e. all involved light is guided within the photonic circuit. To couple light into the integrated waveguide structure we use focusing grating couplers which are optimized for operation in the telecommunications C and L-band.

In order to study the time-resolved characteristics of our memory cell we use a pump-probe technique. For this, the GST is excited by an intense pump pulse while the response is monitored with a low-power probe beam. The measurement setup used is presented in detail in Fig. S1. To extract the small change in probe power from the much more intense pump pulse we use a bidirectional scheme where the pump and probe are guided through the cell from opposite

directions. Externally this is implemented with a set of two optical circulators which direct the light coming from the laser sources onto the chip and subsequently onto the photodetectors. In addition, we use two different colors to suppress the influence of back-reflections with an optical band-pass filter (Pritel, TFA-1550) which features 1 dB insertion loss, a 3 dB bandwidth of 2 nm and an off-resonance suppression exceeding 40 dB for wavelengths further apart than 10 nm. The pump pulse is generated from a CW-diode laser (New Focus, 6427) in combination with an electro-optical modulator (EOM by Lucent Technologies, 2623CS) which is controlled by an electrical pulse generator (HP 8131A). The pulse is further power amplified by a low-noise erbium-doped fiber amplifier (EDFA by Pritel, LNHPFA-33). With this implementation we can accurately control both pulse length and power, enabling pulses as short as 300 ps, with pulse edges in the picosecond-regime and with peak powers up to 150 mW. The response to such a pump excitation is probed with CW-light from a second laser source (Santec, TSL-510C). After propagation through the cell and the band-pass filter, the light is split into two beams which are subsequently send on a fast (New Focus, Model 1811) and a low-noise photodetector (New Focus, Model 2011). The signal of the fast detector enables recording a high-resolution time-trace of the response with a 6 GHz oscilloscope (Agilent infiniium, 54855A) while the overall-device transmission is monitored at all times with the other detector.

Initialization and erase routine

Crystallization of amorphous GST enhances optical absorption at telecommunication wavelengths by one order of magnitude. In our evanescently coupled memory cell this results in a drastic increase of absorbed energy which renders both amorphization and crystallization possible with pulses of comparable length and power. Full recrystallization with a single light pulse is challenging in practice, however, because of this rapid increase in absorption upon phase-change. If the phase transition occurs before the end of the pulse, the continued optical energy supply may heat up the GST further to the melting temperature and cause immediate reamorphization. Because of the temperature variation across the memory cell (cf. Fig. S3), however, this cannot be prevented completely since not all parts of the GST crystallize simultaneously. To circumvent this issue, we use an *Erase* scheme based on stepwise partial recrystallization which is performed by a train of consecutive pulses. In order to prevent reamorphization of already crystallized regions, the individual pulse energies, starting from the

pulse energy used for the *Write* transition, are gradually decreased from pulse to pulse by approximately 5 % of the initial pulse energy. The energy of the final pulse determines which lower transmission level is achieved. This can be the fully crystalline or an intermediate state by stopping the *Erase* scheme exactly at the same energy required to *Write* that specific level.

High reproducibility of the memory operation is ensured by an initial conditioning step. For this, the *Write/Erase* switching cycle is performed a few times on the as-deposited and subsequently annealed GST. Within the first few cycles the read-out transmissions, which initially vary slightly from cycle to cycle, stabilize to a fixed value.

TEM analysis

The TEM specimens were prepared by focused ion beam (FIB) in a FEI strata Dualbeam system. The cross sectional lamellae were cut from the GST memory device along the waveguide (see supplementary information) and thinned to a thickness of less than 50 nm for TEM imaging. The TEM specimens were examined in a FEI Titan 80-300 electron microscope equipped with CEOS image spherical aberration corrector, Fischione model 3000 high angle annular dark field (HAADF) scanning transmission electron microscopy (STEM) detector, EDAX SUTW energy dispersive X-ray spectroscopy (EDX) detector and Gatan Tridiem image filter. The microscope was operated at an accelerating voltage of 300 kV.

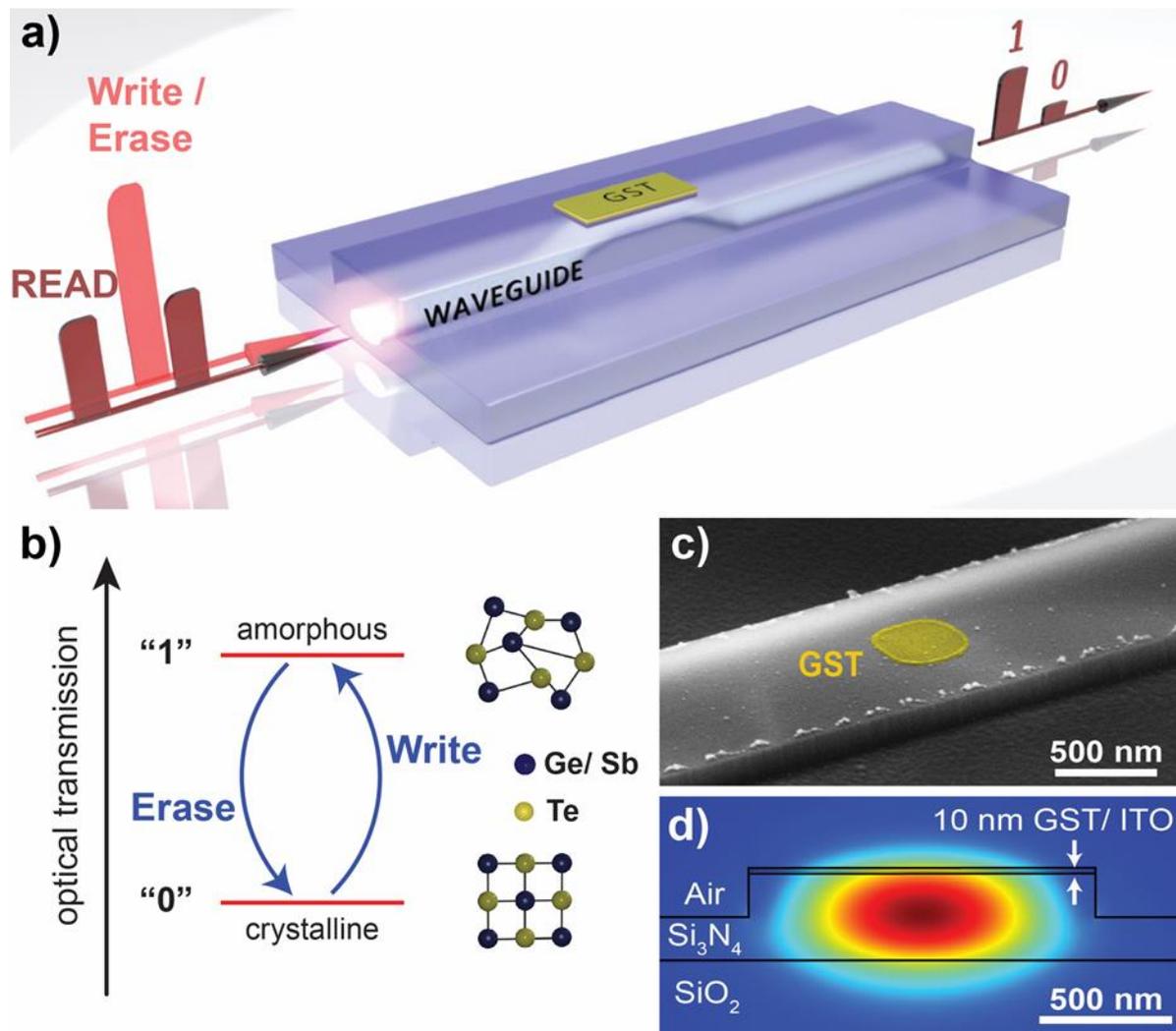


Figure 1. Operation principle of the all-optical on-chip memory device

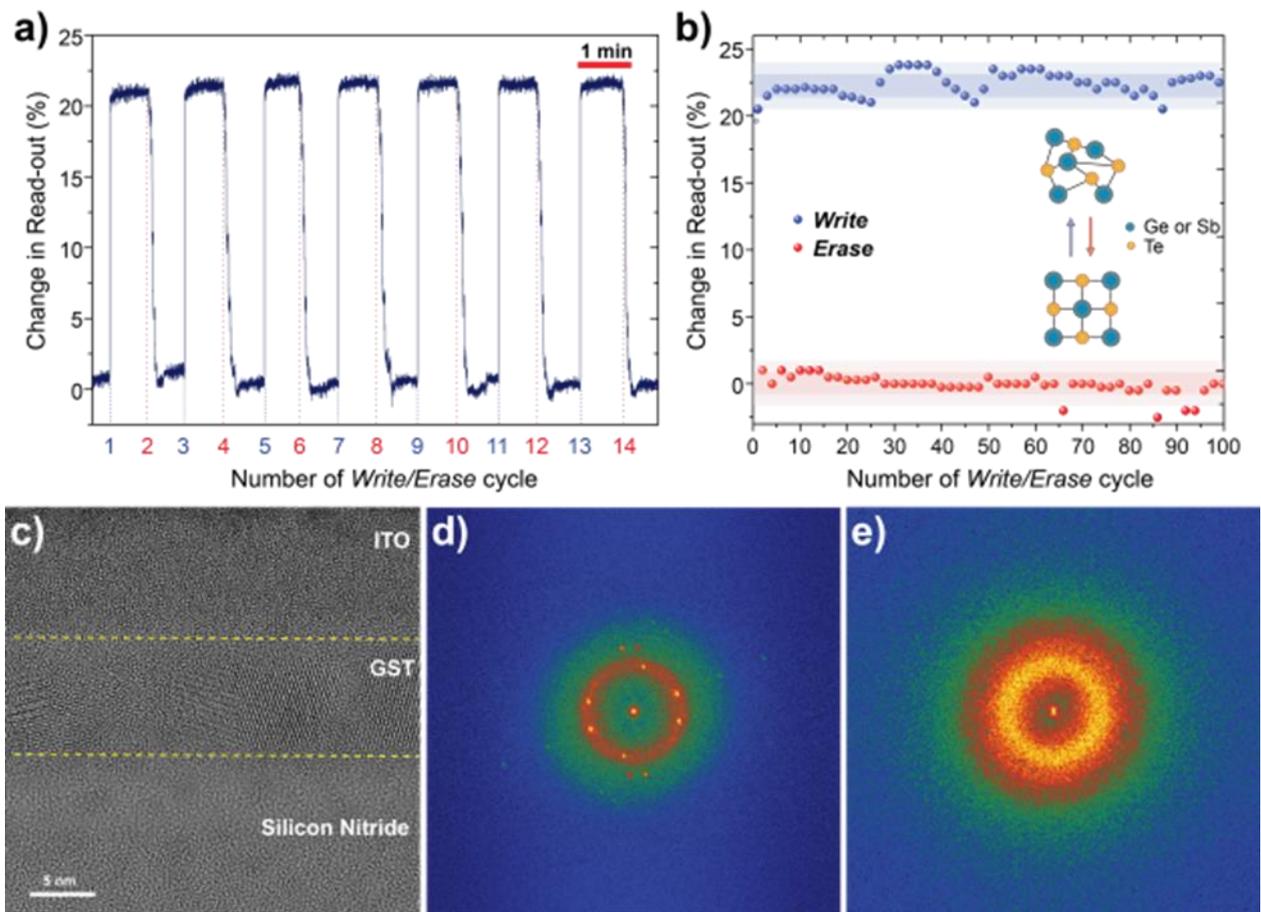


Figure 2. Reversible and reproducible single shot switching.

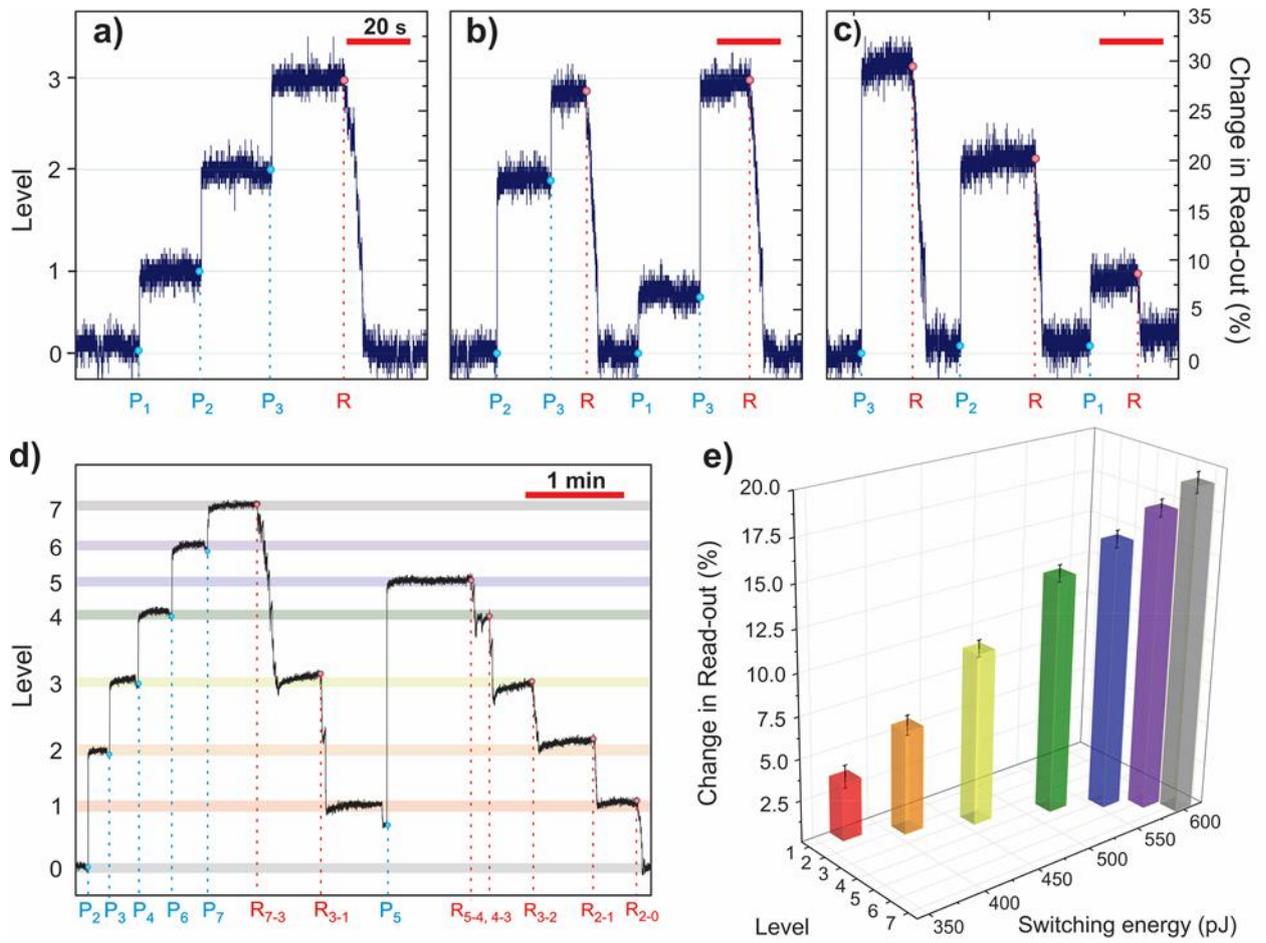


Figure 4. Multi-level operation of the all-photonic memory element