

Ultrahigh Storage Densities via the Scaling of Patterned Probe Phase-Change Memories

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Abstract—The scaling potential of patterned probe phase-change memory (PP-PCM) cells is investigated, down to single-nanometer dimensions, using physically realistic simulations that combine electro-thermal modelling with a Gillespie Cellular Automata (GCA) phase-change model. For this study, a trilayer TiN/Ge₂Sb₂Te₅/TiN cell structure (isolated by a SiO₂ insulator) was preferred, due to its good performance and practicability, over previously investigated probe-based structures such as those that used diamond-like carbon capping layers or immersion in an inert liquid to protect the phase-change layer (while still allowing for electrical contact). We found that PP-PCM cells with dimensions as small as 5 nm could be successfully amorphized and re-crystallized (RESET and SET) using moderate voltage pulses. The resistance window between the RESET/SET states decreased with a reduction in cell dimensions, but it was still more than order of magnitude even for the smallest cells, predicting that PP-PCM cells are indeed scalable and operable in the sub-10 nm region. Most importantly, it was found that the storage density could be increased by cell size scaling with storage densities as high as 10 Tb/in² being achieved, which is significantly higher than the storage densities previously reported in phase-change probe storage, and other probe-based technologies such as thermomechanical, magnetic and ferroelectric probe storage.

Index Terms—GeSbTe, phase-change materials, scanning-probe memories, patterned probe phase-change memories, scaling, terabit-per-square-inch (Tb/in²) storage density.

I. INTRODUCTION

Non-volatile, random-access phase-change memories (PCMs), based on the reversible transitions of chalcogenide phase-change materials, such as Ge₂Sb₂Te₅ (GST), between a high resistance amorphous state (binary ‘0’) and low resistance crystalline state (binary ‘1’), are one of the leading contenders to complement, or even replace, silicon-based memories in a number of technology areas, including the emerging sector of storage class memory (SCM) and established technologies such as DRAM, HDD and Flash [1].

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This is attributed to their size scalability (sub-10 nm [2-4]), ultrahigh storage densities (Tb/in² [5-7]), fast programming speeds (~ps [8]), and low programming currents (~μA [3-4]). Novel functionalities demonstrated by PCM-type devices, such as neuronal and synaptic mimics [9-11], arithmetic and logic processing [12-14], metadvice and all-photonic memories [15-16] and even the realization of non-volatile optoelectronic displays [17], have also highlighted the significance and potential of chalcogenide-based devices.

In electrical PCM, the switching of the phase-change material between the high-resistance amorphous (or RESET) state and the low-resistance crystalline (or SET) state is achieved using appropriate excitations i.e. appropriate voltage pulses. In general, a higher-amplitude short-duration RESET pulse switches the PCM cell into the amorphous state, whereas a lower-amplitude longer-duration SET pulse switches it back to the crystalline state. The state of the cell (binary 1 or 0) is then read out by sensing the resistance using a very low voltage read pulse which does not disturb the stored state.

Patterned Probe PCM (PP-PCM) cells, in which small phase-change regions (isolated from each other by an electrical and thermal insulator) are electrically switched using a scanning probe, potentially provide an efficient approach to achieve ultrahigh storage densities by scaling the cell dimensions. Although electrical switching in PP-PCM cells has been demonstrated on the micrometer scale [18], and more recently storage densities of up to 207 Gb/in² have been reported using conical PP-PCM cells [19], it is yet to be determined whether PP-PCM cells can be scaled down to single-nanometer dimensions, and whether we can achieve ultrahigh (multi-Tb/in²) storage densities, higher than those previously reported for phase-change based probe-type storage (i.e. 1.5 Tb/in² using electrical probes [7] and 3.3 Tb/in² using thermal probe storage [6]). To address this omission, in this study we carry out detailed physically-realistic simulations of the performance of PP-PCM cells down to sub-10 nm dimensions using a sophisticated phase-change model, and investigate the effects of scaling on the achievable storage densities.

II. METHODOLOGY

A. Electro-thermal and Phase-change Model

In order to understand the physical processes involved in the application of phase-change materials for electrical data storage, and to design and optimize future PCM devices, it is important to develop physically-realistic models by combining

electrical, thermal and phase-change models. Our electrical and thermal models are implemented using finite-element software (COMSOLTM) and solve, simultaneously, the Laplace equation (1) and the heat-transfer equation (2), i.e.

$$\nabla \cdot (\sigma \cdot \nabla V) = 0 \quad (1)$$

$$\rho C_p \frac{\partial T}{\partial t} - k \cdot \nabla^2 T = Q = \sigma |E|^2 \quad (2)$$

where V is the electric potential, E is the electric field, σ is the electrical conductivity, ∇ is the gradient operator, ρ is the density of the material, C_p is the specific heat capacity, Q is the heat source, and k is the thermal conductivity. These equations are solved for each time step (for any given electrical input voltage pulse) to yield the 3D (or pseudo-3D, i.e. 2D with cylindrical symmetry) temperature distribution throughout the PCM cell at each time step (with typical time steps being 1ns). This temperature distribution drives, after each time step in the solution of (1) and (2), a phase-change model that determines the phase-state (crystalline or amorphous) everywhere throughout the PCM cell and feeds back (to the electro-thermal model) the relevant material parameters (i.e. those of the crystalline or amorphous states) for each point in the cell. Our phase-change model uses the Gillespie Cellular Automata (GCA) approach that combines thermodynamic features of rate equation-based methods with elements from probabilistic cellular automata models. Our GCA model has been described previously in detail (see [20]) and in summary considers a homogeneous, isotropic material in a square lattice of size 0.82 nm (equivalent to the diameter of a spherical monomer of GST material, as calculated from the density and molar weight of GST, see [21]) and in which each site can be either amorphous or crystalline. The state of each point (i,j) in the lattice is described by two quantities; r_{ij} , the phase of the (i,j) site (which takes the values 0 and 1 for amorphous and crystalline respectively), and Φ_{ij} , which defines an orientation (with two adjacent crystalline sites belonging to same crystallite (crystal grain) if they have the same orientation). The local changes that can occur are defined by three events: nucleation, where site (i,j) and an adjacent site, originally both amorphous, become a single crystallite; growth, where site (i,j) , originally amorphous, becomes attached to an adjacent crystal; dissociation, where site (i,j) , originally crystalline, detaches from the crystal of which it is a part to become amorphous. The rate at which each of these three events occurs is determined by the system energy, which is usually described in terms of the Gibbs free energy G , where $G = (AS - Vg)$ and A and V are the surface area and volume respectively of a crystal cluster, S is the surface energy and g the bulk free energy difference between phases. The bulk energy difference term g is considered to be purely temperature dependent (for example as $g(T) = H_f (7T/T_m)[(T_m - T)/(T_m + 6T)]$ where H_f is the enthalpy of fusion and T_m is the melting point) [21].

B. Simulations of PP-PCM Cell Structure

We begin by simulating the RESET and SET processes in a cell structure consisting of a 50 nm /50 nm (TH/W_c) GST region (isolated by a 20 nm wide SiO₂ partition) sandwiched between 10 nm thick TiN top and bottom electrodes, as shown in Fig. 1 (with the material parameters used in our simulations shown in Table 1). In our simulations the PP-PCM cell is embedded into a virtual test bench consisting of an electrical pulse source and a series load resistance of 10 kΩ. A Pt C-AFM probe with a 5 nm radius is used to make electrical contact with the TiN top electrode, and trapezoidal RESET and SET voltage pulses of various amplitudes (1 – 2 V) and durations (40-100 ns) are applied to the top of the C-AFM probe, whilst the boundary of the Si substrate is maintained at ground potential (as shown previously in [5, 7]). To avoid interference between neighboring cells, the top TiN electrode is patterned to cover the GST layer only (as proposed in [18]).

C. Geometrical Scaling & Storage Density Calculations

After demonstrating electrical switching in the 50 nm GST cell, geometrical scaling is performed by reducing the GST TH and W_c dimensions simultaneously down to dimensions as small as 5 nm using a constant scaling factor of 1 (for simplicity). The storage density is then calculated using $\rho = 1/P_{\text{int}}^2$, where P_{int} is the center-to-center distance between neighboring cells aligned in a checkerboard pattern (see Figure 1).

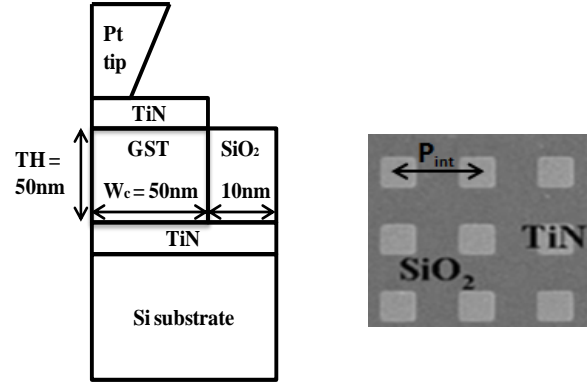


Figure 1. TiN/GST/TiN PP-PCM cell schematic (left) showing one half of the unit cell. Array of PP-PCM cells aligned in a checkerboard pattern (right).

Element	Therm.Cond. (W/mK)	Heat Cap. (J/m ³ K)	Elec. Cond. (Ωm) ⁻¹
GST (am.)	0.2	1.25 x 10 ⁶	See [5]
GST (cr.)	0.5	1.25 x 10 ⁶	See [5]
TiN	19	2.16 x 10 ⁶	5 x 10 ⁶
Pt	71.6	2.8 x 10 ⁶	0.94 x 10 ⁷
SiO ₂	1.4	3.1 x 10 ⁶	1 x 10 ⁻¹⁶
Si	149	1.65 x 10 ⁶	100

Table 1. Material parameters used in our simulations

III. RESULTS AND DISCUSSION

A. Choice of PP-PCM Cell Structure

A typical PP-PCM cell structure consists of a scanning probe and a storage media stack consisting of phase-change regions sandwiched between a capping and under layer, and isolated by insulator regions, which are deposited on a Si substrate. The choice of capping layer is crucial as it not only protects the active phase-change region from oxidation and wear, but also provides a conductive path for the current required for electrical switching, and consequently has a strong influence on the resulting temperature distributions inside the active region [5, 7].

TiN is a well-known electrode material and has previously been used in GST-based patterned PCM cells to demonstrate electrical switching [18, 19]. Amorphous to crystalline phase transitions in GST films as thin as 2 nm have also been reported in [2] using a trilayer TiN/GST/TiN structure. TiN is well suited as a capping/electrode material mainly due to its suitable electrical and thermal conductivities, and high melting temperature (~ 3250 K). In addition, good adhesion between GST and TiN has been observed at the atomic scale [22], and no evidence of a reaction between TiN and GST has been reported to date. Therefore, in this study a TiN/GST/TiN structure is preferred over other reported probe-based structures such as (i) the use of a diamond-like carbon (DLC) capping layer [5, 7], and (ii) by immersing the sample in a fluorinert liquid [23].

B. Electrical Switching & Scaling Characteristics

We start with a fully crystalline GST material (red in color in Fig. 2) and form amorphous bits (blue in color) with a minimum bit size of 2-10 nm [5] in the region under the C-AFM tip. For the 50 nm GST cell, a moderate 1.8 V, 40 ns RESET pulse forms a rounded amorphous bit (first phase diagram in Fig. 2) in the region where the GST melting temperature (~ 893 K) is exceeded. The corresponding RESET temperature distribution inside the GST layer for the 50 nm cell is shown in Figure 3. Following the completion of the RESET process, the amorphous bit is then re-crystallized using a 1.2 V, 100 ns SET pulse, a process initiated by crystal nuclei that appear in regions where high values of temperature and electric field are observed [24]. These nuclei then grow until the amorphous bit is fully re-crystallized, signifying the successful completion of the SET process.

Figure 2 shows the RESET and corresponding SET phase diagrams as the GST dimensions are scaled from 50/50 nm down to 5/5 nm (again using RESET and SET voltage amplitudes of 1.8 and 1.2 V respectively). As expected, since the top electrode width reduces with cell size, the amorphous bit also reduces in size as the cell dimensions are reduced.

The number of crystallites formed during the re-crystallization (SET) of the amorphous bits is shown in Figure 4 (corresponding to the SET phase diagrams in Figure 2). A nucleation-dominated behaviour is observed for larger cell dimensions, which is indicated by the high number of crystals formed to re-crystallize the amorphous bits. However, a

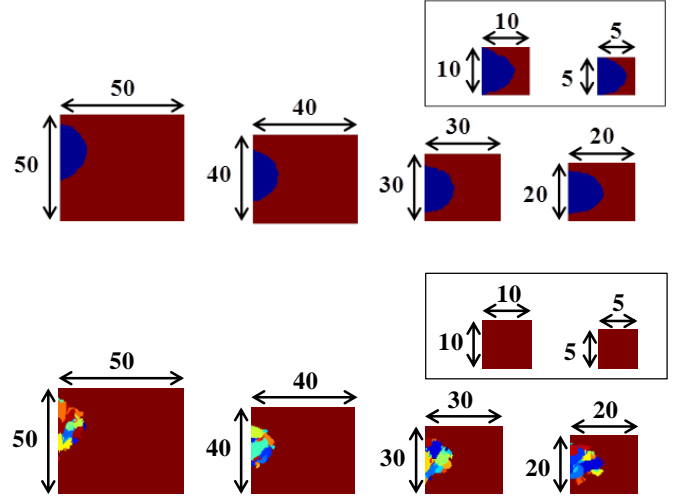


Figure 2. (top) Successful formation of amorphous bits (shown in blue) at the end of the RESET process as GST dimensions are scaled down in size (plots show one half of the GST layer and numbers at the top and side show the GST thickness, TH and width W_c (in nm)). The shape of the amorphous bit changes from a rounded shape for larger GST dimensions to ellipsoidal for smaller dimensions (shown in inset). (bottom) Re-crystallization (SET) of the amorphous bits. The crystallization for the larger GST dimensions is nucleation-dominated (indicated by the large number of crystals formed) and is driven by ‘interfacial growth’ for the smaller GST dimensions (shown in inset).

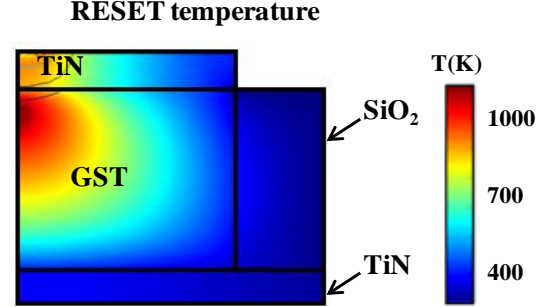


Figure 3. RESET temperature distribution inside the PP-PCM structure comprising of a 50/50nm GST region sandwiched between 10nm thick TiN top and bottom electrodes and a 20nm wide SiO_2 insulator.

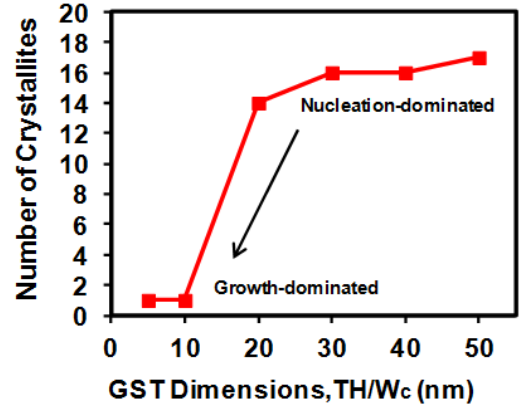


Figure 4. Number of crystal nuclei formed during the SET process as a function of GST dimensions (corresponding to the SET phase diagrams shown in Figure 2). A transition from nucleation-dominated to growth-dominated crystallization is observed as the GST dimensions are scaled to smaller sizes.

reduction in the number of crystal nuclei is observed for smaller dimensions, indicating a transition towards growth-dominated behaviour. Indeed, for the smallest cells it can be observed that a crystallization process driven purely by ‘interfacial growth’ from the crystalline-amorphous boundary occurs for GST dimensions of 10 nm and below (see inset of Figure 2), a phenomenon previously reported in pore-type PCM cells [25].

The results shown in Figures 2, 3 and 4 show that it should, using reasonable voltages, be possible to successfully amorphize and re-crystallize PP-PCM cells down to single-nanometer dimensions. However, an important characteristic we have not considered thus far is the resistance window, i.e. the difference in resistance between the RESET and SET states. The resistance window in PCM should be large enough to allow for reliable differentiation on readout between the amorphous and crystalline states in the presence of noise, cell-to-cell variability etc. We therefore plot in Figure 5 the variation of the cell resistance as a function of the GST cell dimensions. Both SET and RESET resistances increase as cells shrink (driven mainly by geometric factors) and the resistance window is observed to decrease (as also seen in conventional PCM ‘mushroom’ type cells [4]). Despite this reduction in the resistance window, at least an order of magnitude difference between the two states is observed even for the smallest dimensions predicting that PP-PCM cells are indeed scalable and operable in the sub-10 nm region.

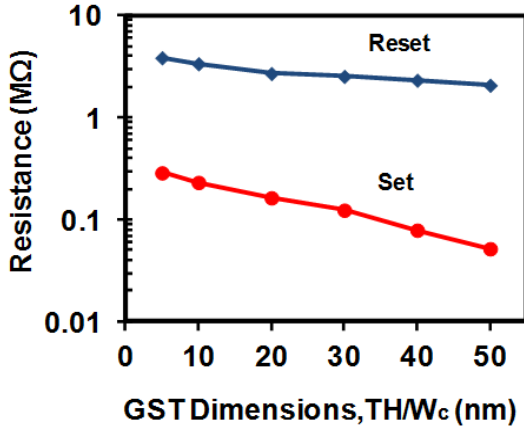


Figure 5. RESET and SET cell resistances as a function of GST dimensions.

C. Storage Densities

Finally we turn our attention to one of the main advantages of device scaling in PCM, i.e. as we reduce the cell dimensions the storage density should subsequently increase. The PP-PCM cell structure we have used thus far consists of a GST region (isolated by a SiO₂ insulator) sandwiched between TiN top and bottom electrodes. Using the storage density formula $\rho = 1/P_{\text{int}}^2$, this provides us with a storage density of 0.13 Tb/in² for a 50/50 nm GST region (with a 20 nm insulator width). From Table 2, we can see that by scaling the GST dimensions down to 5/5 nm we can potentially increase the

storage density up to 1.03 Tb/in². However, one aspect that has not been considered yet is the reduction of the insulator width, which should further increase the storage density significantly but which could lead to unwanted thermal cross-talk. Thermal cross-talk is likely to be most deleterious during the RESET process (since the highest cell temperatures are reached in this case) and when the adjacent cell (to that being RESET) is in the amorphous phase (in which case thermal interference could lead to unwanted crystallization of the adjacent cell). Thus, we applied a RESET pulse to the smallest of our PCM cells (i.e. the 5 nm cell) and calculated the temperature distribution in that cell and in adjacent cells, as the width of the SiO₂ ‘spacer’ between cells was reduced. Results are shown in Figure 6, for the point (during the RESET pulse) at which the maximum temperature occurs in the cells. The maximum temperatures seen in the adjacent cell under these conditions are found to be 293 K, 376 K and 479 K for SiO₂ spacer widths of 20 nm, 3 nm and 1 nm respectively. Even in the case of the 1 nm spacer width, the maximum temperature in the adjacent cell of 479 K would not cause any significant crystallization on the short timescales (tens of nanoseconds) used for the RESET pulse (in previous work, for example, we showed that the crystallization time for GST in the 400-500 K temperature range is hundreds of microseconds [26]). Certainly with a 3 nm spacer width the thermal cross-talk to the adjacent GST cell is negligible (the cell would take days or even months to fully crystallize at a temperature of 376 K, see [21]). Hence, using the storage density formula, a 5/5 nm GST region insulated by a 3 nm wide SiO₂ spacer can provide us with a storage density as high as 10.08 Tb/in² (as shown in Table 2).

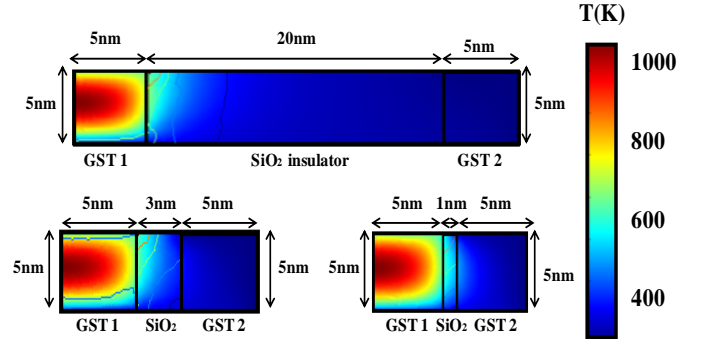


Figure 6. Electro-thermal simulations executed to determine the ultimate insulator width between GST cells before thermal interference (between cells) has any significant effect (see text). The insulator width can be reduced from 20nm (top) down to 3nm (bottom left) with very little thermal interference during a RESET pulse. Even in the case of an insulator width of 1nm (bottom right), thermal interference to the neighboring cell causes its temperature to increase only to 479 K.

These findings are extremely encouraging as they show that storage densities significantly higher than those reported in PCM electrical probe storage (1.5 Tb/in² using GST films [7] and 207 Gb/in² using PP-PCM cells [19]), can potentially be achieved. In fact, the storage density reported in this study significantly exceeds the highest storage density reported to date in PCM, i.e. 3.3 Tb/in² reported using thermal probe storage [6]. We do note however that the cylindrical

symmetry approximation inherent in our electro-thermal and phase-change simulations presents an effective lower bound (best-case estimate) of the scaling potential, since any variation in cylindrical symmetry (induced say by probe offset from the cell center) could lead to increased thermal interference between adjacent cells.

It will now be interesting to see how the storage density achieved in our study compares to those reported in other technologies, such as thermomechanical, ferroelectric and magnetic probe storage. For this we present a comparison chart in Figure 7, which shows that the storage density reported here is significantly higher than the highest storage densities of 60 Gb/in² reported in magnetic probe storage, and 4 Tb/in² reported in thermomechanical and ferroelectric probe storage [27]. Our physically-realistic simulations show therefore that PP-PCM cells can indeed deliver excellent scalability down to single nanometer dimensions and, in doing so, ultrahigh (multi-Tb/in²) storage densities can indeed be achieved using such a cell architecture.

GST Size, TH/W _c (nm)	Storage Density
50/50 (with 20nm wide SiO ₂)	0.13 Tb / in ²
40/40 (with 20nm wide SiO ₂)	0.17 Tb / in ²
30/30 (with 20nm wide SiO ₂)	0.26 Tb / in ²
20/20 (with 20nm wide SiO ₂)	0.40 Tb / in ²
10/10 (with 20nm wide SiO ₂)	0.72 Tb / in ²
5/5 (with 20nm wide SiO ₂)	1.03 Tb / in ²
5/5 (with 10nm wide SiO ₂)	2.86 Tb / in ²
5/5 (with 3nm wide SiO ₂)	10.08 Tb / in ²

Table 2. Storage densities as the PP-PCM cell dimensions are scaled down to single-nanometer dimensions

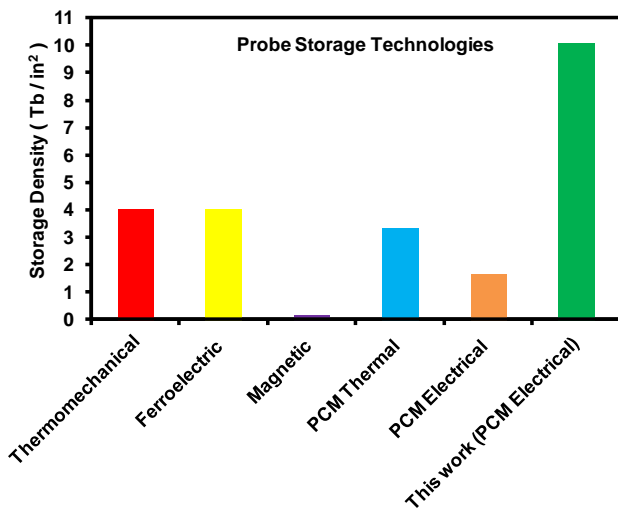


Figure 7. 10 Tb/in² storage density achieved in this work (green bar) compared to other reported densities achieved in PCM (~1.5-3 Tb/in²) and other probe-based technologies such as thermomechanical (4 Tb/in²), ferroelectric (4 Tb/in²) and magnetic (60 Gb/in²) storage (adapted from [26]).

IV. CONCLUSIONS

We have investigated, using a physically-realistic simulation approach, the scalability of probe-based PCM, specifically patterned probe PCM (PP-PCM) devices. A trilayer cell structure consisting of the active phase-change regions sandwiched between TiN top and bottom electrodes and isolated by an SiO₂ insulator was most practicable and scalable when compared to other probe-based structures such as (1) the use of a diamond-like carbon capping layer, and (2) by immersing the sample in a fluorinert liquid. We found that PP-PCM cells could be scaled down to sub-10 nm dimensions using a systematic and simplistic scaling approach, and in doing so amorphous bits could be successfully written. Such amorphous bits were then successfully re-crystallized with the crystallization process determined to be nucleation-dominated for larger cells and growth-dominated as cell dimensions were reduced. The resistance window between the RESET and SET states decreased as the cell dimensions were reduced, but it was still more than order of magnitude even for the smallest (sub-10 nm) cells. Perhaps most importantly we found that the storage densities could be increased with cell size reduction and storage densities as high as 10 Tb/in² could potentially be achieved for the smallest cells. This storage density was found to be significantly higher than those previously reported in PCM, and other probe storage technologies such as thermomechanical, magnetic and ferroelectric probe storage.

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