Control Strategy for Uninterrupted Microgrid Mode Transfer during Unintentional Islanding Scenarios

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***Abstract*—This paper presents a microgrid control strategy to unify the control topology for energy storage systems (ESS) and renewable energy sources (RES) inverters in an AC microgrid and to protect the microgrid reliability from unintentional islanding instability using control loops which use the DC link voltage as a feedback. This bounds the DC link voltage and provides reliable operation in the microgrid. Simulation validates the proposed control strategy, and experiment results extol the concept.**

***Index Terms*—Microgrids, Energy storage, Renewable energy sources, Control.**

I. Introduction

THE main concept of the microgrid is to distribute the energy sources (ES) and to decentralize the control units in order to integrate the renewable energy sources (RES). Microgrid is connected to grid for power exchange or isolated due to maintenance, available power or unintentional islanding scenarios. Islanding mode needs coordinated control to provide accurate power and seamless transfer between grid-connected and islanded mode.

Droop control [1]–[6] regulates the power flow between inverters referring to local measurements. In unintentional islanding, islanding detection takes longer time because the supervisory controller (SC) cannot quickly update the units (Fig. 1). During that time, a controller is needed to preserve the stability and reliability of each unit to achieve seamless mode transfer, which is adopted by many researchers [7]–[20]. A nonlinear sliding-mode voltage controller and adaptive power sharing controller are proposed in [7]. It employs an internal model voltage controller to reduce voltage disturbances but the stability of the DC link voltage is not addressed. A design of virtual inductance and resistance is presented in [8] and [9] to reduce the inrush current during mode transitions. Local phase locked loop (PLL) and virtual inductor [10], frequency/phase synchronization method [11], adaptive droop coefficients control [12], and master/slave communication-based control strategy [13], [14] are all proposed for smooth mode transition. [15] focuses on achieving seamless transitions by having voltage and current sources working mutually in each mode. In [16], the reference power setpoint is defined in advance. However, maximum power point tracking (MPPT) is used for varying resources like photovoltaic (PV) arrays, and reference power is not defined in unintentional islanding [17] due to grid status. The output power of PV array is bounded between zero and maximum power point (MPP) in [18] to implement power curtailment in islanded mode. A dispatch unit is chosen in [19] to facilitate the interconnection with utility and to achieve smooth transition between the operating modes. Furthermore, a hierarchical control is proposed in [20] to simplify the seamless transition. However, DC link stability has not been emphasized. [21] highlights the circulating power flow and emphasize the DC link stability but the microgrid structure does not address the DC converters dynamics. [22] suggests resistor-based DC voltage damping method. However, the resistor can not limit the DC voltage in all cases.

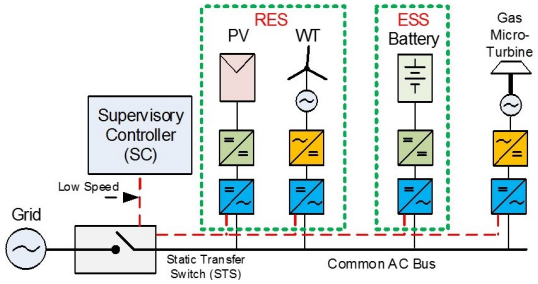

Fig. 1: General structure of microgrid.

This paper presents a DC link voltage loop to unify the control schemes. A control scheme is implemented for power management and small signal model (SSM) is developed to assess the stability. Section II of this paper presents circulating power flow between distributed generators (DGs). The proposed topology is shown in section III. DC/AC and DC/DC control loops are illustrated subsequently in sections IV and V. Sections VI and VII present simulation and experiment, whereas section VIII draws conclusions.

II. Circulating Power Flow between DGs

The common power management topology [23]–[26] sets the inverter as an AC source to control the frequency and voltage, whereas the DC/DC converter works as a DC source to control voltage across the DC link capacitor. On the other hand, RES inverter works as an AC current source to generate the available power and inject it to the grid. RES DC/DC converter is set as a DC current source to inject power to the DC link capacitor. Nevertheless, the ESS and RES have different control operation in both grid-connected and islanded mode. To overcome the circulating power flow, additional DC link voltage loop is required including the droop controller that works intermittently to save the inverter [21]. Therefore, the need for an outer DC link voltage loop including the droop control loop is necessary for reliable operation especially during unintentional islanding. Thus, all units adopt the control scheme and additional control loop is added to guarantee the stability and seamless transfer. In grid-connected mode, multi-inverters generate different power setpoints (sent by SC). The output frequency, ω, and voltage, V, are as in (1) and (2):

$$\omega = \omega_o + m(P_{ref} - F(s)P) \tag{1}$$

$$V = V_o + n(Q_{ref} - F(s)Q) \tag{2}$$

where ω_o and V_o are the nominal output voltage and frequency, m and n are the active and reactive power droop gains, P_{ref},Q_{ref} are calculated after the filter shown in (3):

$$F(s) = 1/(\tau s + 1) \tag{3}$$

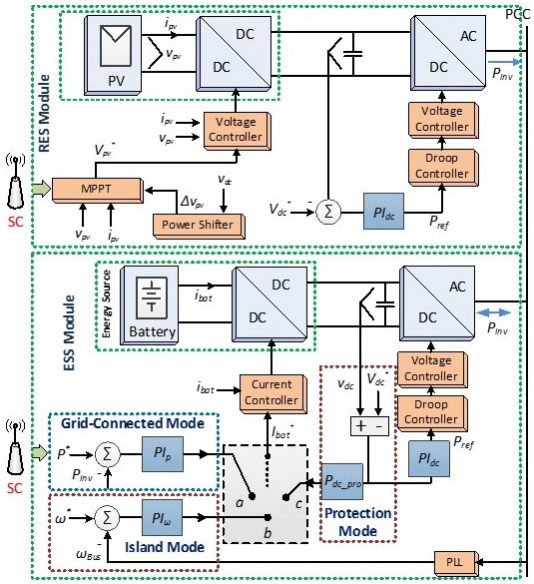

Fig. 2: Proposed microgrid control topology.

where τ is the time constant. AC microgrid frequency is linked to the grid (ω_{grid}) which equals to the nominal frequency (ω_o) and the inverters generate different power values in grid-connected mode. However, in case of grid loss, the bus frequency shifts to a new steady state value (ω_{island}) according to the DGs power references and loads (assuming a neglected network losses) [21] to be as in (4):

$$\omega_{island} = \omega_o - \frac{m}{2}(P_L - \sum_{i=0}^{n} P_{i_{ref}}) \tag{4}$$

where n is the inverters number. (4) illustrates that if the load is more than the sum of power setpoints, the islanding frequency will be less than the grid frequency, otherwise it will be greater than the grid frequency. The latter shifts the output power of each unit to another value and makes the units of lower P_{ref} importing power. The bidirectional power flow through the inverters alters the DC link voltage whereas it acts as an external disturbance in the ES DC voltage control loop. This circulating power increases the DC link voltage and causes inverter shutdown. The buck/boost controller aims to reduce the injected current to the DC link capacitor if the DC link voltage rises and the ESS has ability to reverse the current flow and switch to charging mode. However, the RES, gas-turbine and fuel cells would reduce the DC/DC current output but, as the minimum limit is zero, they can not absorb the current. As a result, the surplus DC link voltage will eventually trip the unit off.

III. Proposed Microgrid Control Topology

In Fig. 2, all ES are chosen to work as DC current sources. The inverters regulate the DC link voltages and balance the power between the DC and AC sides using PI controller to

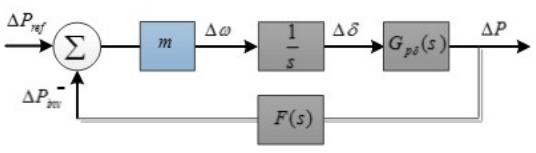

Fig. 3: SSM of power control loop.

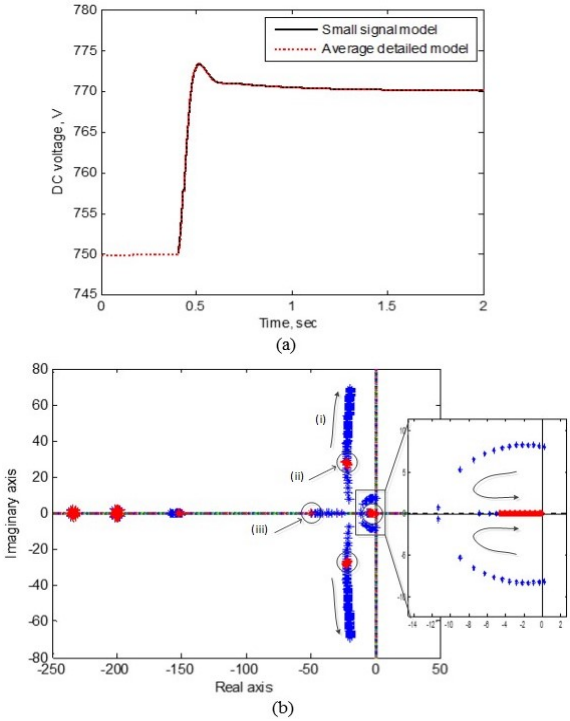

Fig. 4: (a) The DC link voltage regulator SSM compared to the average detailed model, and (b) root locus of the DC link voltage regulator.

dictate the droop control. For PV, MPPT is used to control the output current whereas the battery power setpoints are received from SC and accordingly it controls the output discharging current or receives an outer SOC controller.

A. MPPT Power shifter

In grid-connected mode, MPPT injects the maximum available power to the grid. Nevertheless, the transient circulating power during unintentional islanding might pass though the PV inverter and charge the capacitor. To immune the DC link voltage from a detrimental rising, MPPT requires an extra loop to handle the DC link voltage variation for MPP shift. Also, MPPT power shifter is used in islanded mode when the generated power is more than the demand. Therefore, enabling/disabling MPPT power shifter is subject to the DC link voltage value or to SC command.

B. ESS control

Since AC bus voltage and frequency are fixed in grid-connected mode, ESS-based DG works as AC current source receiving the reference value from SC by the communication means. The reference value through the power loop (switch a in Fig. 2) controls the DC/DC converter output current while the DC voltage is fixed by the inverter regulation loop. In normal islanded mode, the ESS module takes the master control of the bus frequency and voltage. The reactive power droop control is used to maintain the AC bus voltage. On the other hand, the active power droop control regulates the DC link voltage and the frequency regulation is implemented by controlling the DC current as in Fig. 2 (switch b).

The intentional switching between both modes is performed by SC. However, under unintentional islanding, this command can be overridden by local protection algorithm (switch c) until

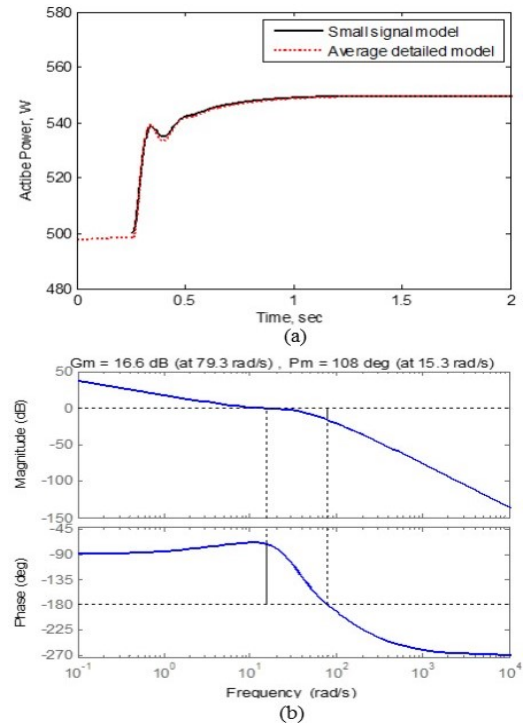

Fig. 5: The power control loop SSM (a) compared to the average detailed model, (b) bode plot when $k_{p\_p} = 0.001$ and $k_{i\_p} = 0.01$.

the SC updates its settings in order to eliminate the circulating power and mitigate the risk of unit trip. In islanded mode, the ES is driven locally by the frequency regulation loop. The DC link voltage dictates the current in the protection mode when v_{dc} exceeds the defined threshold. Finally, it dominates the control until receiving an update from SC. In all modes, the inverter acts as a DC voltage source in DC side and as a DC voltage-driven current in AC side. The DC link voltage regulation loop is activated at the time of microgrid connection after synchronization.

IV. DC/AC Control Loop Design

Small signal analysis is carried out around operating points. Output voltage controller and the ES inner current control loop, in Fig. 2, are assumed to be unity. DC/AC side control loops are studied and they are similar for both PV and battery units.

A. Inverter's power flow control

The droop control represents the inner loop of the DC link voltage regulator as in Fig. 2 whereas the real and reactive power of the inverters are calculated as in (5) and (6):

$$P = (RV^2 - RVV_{pcc}cos\delta + XVV_{pcc}sin\delta)/(R^2 + X^2) \quad (5)$$

$$Q = (XV^2 - XVV_{pcc}cos\delta - RVV_{pcc}sin\delta)/(R^2 + X^2) \quad (6)$$

where P and Q are the output instantaneous power, X and R are the equivalent output reactance and resistance of each inverter, V and V_{pcc} are the inverter output voltage and the PCC voltage, and δ is the phase angle. By linearizing equations (1), (2), (5) and (6) we obtain:

$$\Delta P = (\partial P/\partial V)\Delta V + (\partial P/\partial \delta)\Delta\delta = K_{pv}\Delta V + K_{p\delta}\Delta\delta \quad (7)$$

$$\Delta Q = (\partial Q/\partial V)\Delta V + (\partial Q/\partial \delta)\Delta\delta = K_{qv}\Delta V + K_{q\delta}\Delta\delta \quad (8)$$

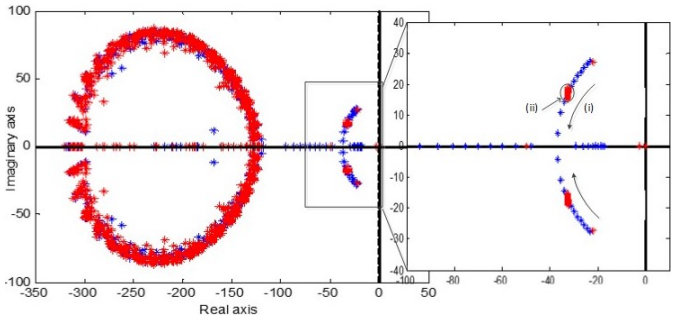

Fig. 6: Root locus in islanded mode when (i) $1 < k_{p\_\omega} < 20$ and $k_{i\_\omega} = 25$ (ii) $10 < k_{i\_\omega} < 50$ and $k_{p\_\omega} = 10$.

$$\Delta\omega = m\left(\Delta P_{ref} - F(s)\Delta P\right) \quad (9)$$

$$\Delta V = -nF(s)\Delta Q = G_{vq}(s)\Delta Q \quad (10)$$

where K_{pv}, $K_{p\delta}$, K_{qv}, and $K_{q\delta}$ are the linearization coefficients calculated at the considered operating points. By substituting for ΔQ from (10) in (8), thus ΔV is given:

$$\Delta V = (G_{vq}(s)K_{q\delta})/(1 - G_{vq}(s)K_{qv})\Delta\delta = G_{v\delta}(s)\Delta\delta \quad (11)$$

Then substituting for ΔV from (11) in (7), ΔP is given:

$$\Delta P = \left(K_{pv}G_{v\delta}(s) + K_{p\delta}\right)\Delta\delta = G_{p\delta}(s)\Delta\delta \quad (12)$$

The output frequency $\Delta\omega$ is related to $\Delta\delta$ in (13):

$$\Delta\omega = s\Delta\delta \quad (13)$$

then ΔP in (12) will be:

$$\Delta P = \Delta\omega G_{p\delta}(s)/s \quad (14)$$

The SSM for the power sharing closed loop is realized by (9), (11) and (13) as shown in Fig. 3. The closed loop transfer function can be derived as:

$$G_p(s) = (mG_{p\delta}(s))/(s + mG_{p\delta}(s)F(s)) \quad (15)$$

The droop gain m is designed to compromise between acceptable power response and accurate sharing [27], and frequency regulation. The maximum m value is subject to the unit's power rating as shown in (16):

$$m = \Delta\omega_{max}/(P_{max} - P_{ref}) \quad (16)$$

where P_{max} is the maximum power rating of the inverter and ω_{max} is the allowable maximum frequency variation.

B. Inverter's DC link voltage regulator

The inverter regulates the DC link voltage using frequency droop control (Fig. 2). Thus, the DC voltage regulator is an outer loop of the power loop controller. The DC link capacitor energy E is calculated in (17):

$$E = C_{dc}V_{dc}^2/2 \quad (17)$$

where C_{dc} and V_{dc} are the DC link capacitor and voltage respectively. Perturbing E, (18) obtains the linearized form:

$$\Delta E = C_{dc}V_{dc}^{eq}\Delta v_{dc} \quad (18)$$

where V_{dc}^{eq} is the equilibrium DC voltage point and Δv_{dc} is small DC link voltage variation around V_{dc}^{eq}. Considering that $s\Delta E = \Delta P$ then (18) is rewritten as in (19):

$$\Delta v_{dc} = \Delta P/(sC_{dc}V_{dc}^*) = G_{dc}(s)\Delta P \quad (19)$$

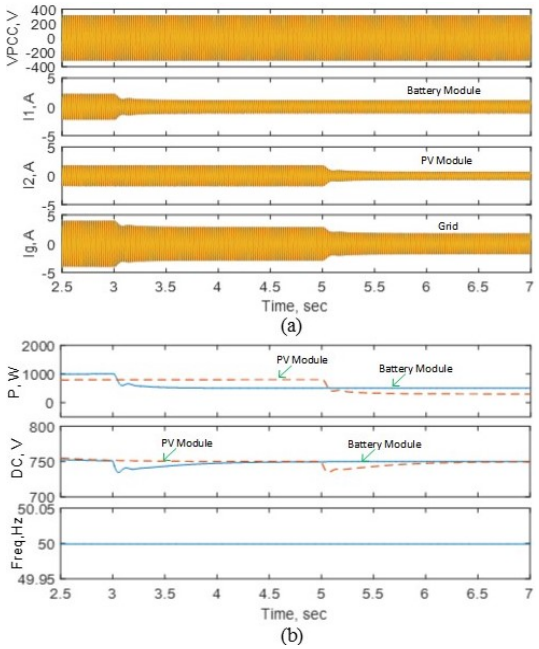

Fig. 7: On-grid: (a) PCC voltage, output current and grid current, (b) output active power, DC link voltages of both inverters and the bus frequency.

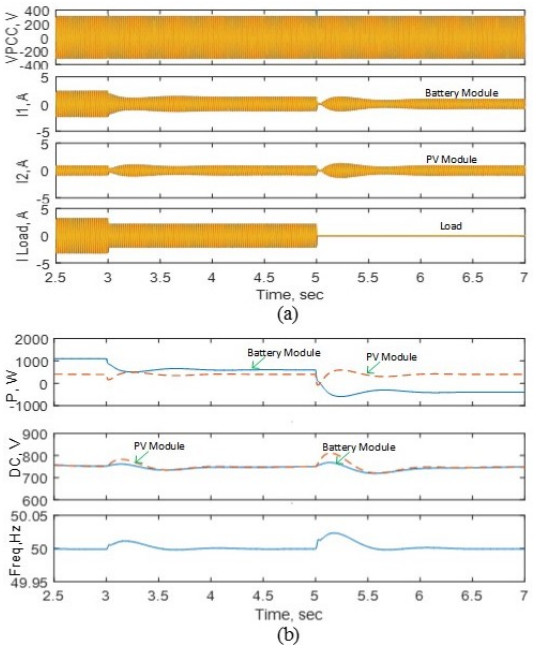

Fig. 8: Off-grid: (a) PCC voltage, output current and grid current, (b) output active power, DC link voltages of both inverters and the bus frequency.

The SSM of the DC link voltage regulator leads to the characteristic equation shown in (20):

$$1 + PI_{dc}(s)G_p(s)G_{dc}(s) = 0 \tag{20}$$

where $PI_{dc}(s)$ is the PI controller transfer function. The small signal DC link voltage response was compared to the average model response built in Matlab as shown in Fig. 4a against step input (750-770V) which confirms the validity of the developed model. The PI gains are chosen such that the dynamic response of the DC link voltage regulator is slower than the inner power flow controller in order to decouple the two controller's dynamics. The root locus of the DC link voltage loop is shown in Fig. 4b. Group (i) denotes the poles trajectory when the proportional gain k_{p_dc} is varying from 0 to 100 whereas group (ii) indicates the poles trajectory when the integral gain k_{i_dc} is varying from 0 to 100 and group (iii) locates the power sharing loop poles when the droop gain $m = 0.85 \times 10^{-4}$ in order to choose relatively slower modes for the DC regulator. The proportional and integral gains k_{p_dc} and k_{i_dc} are chosen to be 25 and 60 respectively.

V. DC/DC Control Loop Design

This section individually studies the design of DC/DC control loop design of PV and battery units shown in Fig. 2.

A. PV MPPT shifter

In PV power control loop, the inner DC/DC converter's loop dynamics is fast to be assumed unity considering the outer loop. Due to the nonlinear PV output power, the function $P_{PV}(v_{PV})$ can be approximated around the operating point where β_{PV} represents the slope of line. The characteristic equation is derived as shown in (21):

$$s + \frac{P_{PV\_PS}\beta_{PV}}{C_{dc}V^*_{dc}} = 0 \tag{21}$$

where P_{PV_PS} is the proportional controller. The characteristic equation is first order differential equation with time constant $C_{dc}V^*_{dc}/P_{PV\_PS}\beta_{PV}$ chosen to be 4ms; slower compared to the inner loops (0.86ms settling time [28]).

B. ESS Grid-connected mode controller

The ESS control loop dictates the output power of the battery in grid-connected mode according to the SC commands. The current controller can be designed to have wide bandwidth and behaves as unity. This loop disturbs the equilibrium of DC voltage regulator, hence, the inverter will react to achieve the balance by generating or absorbing power. The SSM was validated versus the average model as shown in Fig. 5 which reveals high agreement when a step power input from 500 to 550W occurs. The open loop transfer function of the ESS power control loop is calculated as shown in (22):

$$G_{ESS\_GC} = \frac{PI_P(s)G_{DC}(s)F(s)}{sC_{dc}G_{dc}(s)} \tag{22}$$

The PI controller gains are designed ($k_{p\_p} = 0.001$ and $k_{i\_p} = 0.01$) to give 15.3rad/s bandwidth which is lower than the inner loop (24rad/s) to provide acceptable stability room for gain margin (16.6dB) and phase margin (108deg) as shown in the bode plot in Fig. 5.

C. ESS islanded mode controller

The control loop in this mode masters the AC bus voltage and frequency by setting the inner converter current loop. The

TABLE I: Simulation setup parameters

Parameter	Value	Parameter	Value
X	$1mH$	k_{p_p}	0.001
R	0.08Ω	k_{i_p}	0.01
k_{p_dc}	25	k_{p_ω}	10
k_{i_dc}	60	k_{i_ω}	25
k_{pv_ps}	5	k_{dc_pro}	0.1
m	8.5×10^{-4}	v_{dc_th}	$820V$
n	8.5×10^{-4}	V	$220V$
τ	5×10^{-3}	ω	$2\pi \times 50$

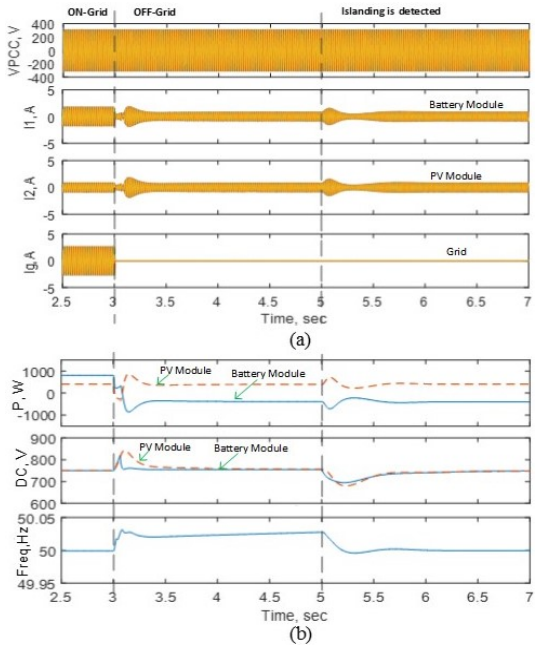

Fig. 9: Simulation results when $P_{Battery} > P_{PV}$ (a) PCC voltage, inverter output and grid current, (b) output active power and DC link voltage.

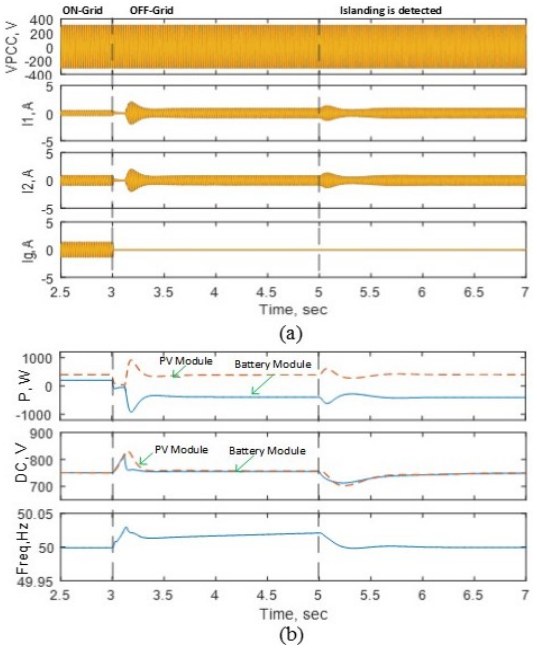

Fig. 10: Simulation results when $P_{Battery} < P_{PV}$ (a) PCC voltage, inverter output and grid current, (b) output active power and DC link voltage.

PI controller is used as a frequency regulator. Similarly, the SSM is built and the root locus is implemented as shown in Fig. 6 zooming the dominant poles. The integral gain does not significantly affect the dynamics whereas the proportional gain increment provides more damping over the tested range values. The PI controller gains are designed ($k_{p\_\omega} = 10$, $k_{i\_\omega} = 25$) to give slower response than the inner loop.

D. ESS unintentional islanding protective mode control

Protective control loop is active once the DC link voltage is beyond the triggering limits. This happens during the transient response of the inverter's DC voltage regulator. The DC link will be limited by the protective control loop while the inverter DC voltage regulator's output current will be treated as a disturbance input. P controller is chosen since the aim of this loop is limitation. Thus, the steady state error is not a concern during the unintentional islanding. The model is first order transfer function and the k_{dc_pro} gain is chosen to be 0.1 giving response time constant as 12ms.

VI. Simulation Results

A two-unit microgrid is simulated using Matlab/Simulink to validate the performance. This microgrid consists of PV and battery units. The parameters are listed in Table I. The performance has been tested in both grid-connected and islanded mode during unintentional islanding. In grid-connected mode, the PV generates MPPT reference and the battery generates reference sent by SC. Fig. 7a shows the output currents with the grid current and PCC voltage whereas Fig. 7b shows the output active power, DC link voltages, and the bus frequency. At $t = 3$s, the battery reference was changed by the SC from 1000 to 500W and at $t = 5$s the PV power reduced from 800 to 300W. In islanded mode, Fig. 8a shows the output currents, load current and voltage when the load is changed from 1500W to 1000W at $t = 3$s and from 1000W to 0W at $t = 5$s. The battery absorbs PV generated power autonomously as Fig. 8b shows the active power, frequency and DC link voltages. The function of the proposed topology against unintentional islanding cases is assessed by the circulating power figures between the inverters when grid is lost and P_L=0.

A. When $P_{Battery} > P_{PV}$

The battery unit discharges its power into the grid. In grid-connected mode, the battery is generating 800W while PV power was 400W. Fig. 9a shows PCC voltage, inverter's output current and grid current. At $t = 3$s, the grid is lost and the power flows from the battery to PV. The power shifter operates immediately to reduce this disturbance and to support the inverter's DC voltage regulator. The battery protection mode is activated at $t = 3.05$s after the DC voltage became greater than v_{dc_th}. At which, the battery was converted to a charging mode absorbing the available PV power and regulating its DC voltage as shown in Fig. 9b. At $t = 5$s, the SC detects the islanding then updates the units with islanded mode settings.

B. When $P_{ESS} < P_{RES}$

The PV maximum power is 400W exported to the grid. The battery is discharging 200W in grid-connected mode. At $t = 3$s, the grid is lost and the transient circulating power flows from PV to battery shown in Fig. 10a. However, the control loop of the battery regulates output power at its setpoint because the islanding has not been detected yet. As a result, the excess power circulates between the units and raising the DC voltage. The PV power shifter acts immediately against this transient by reducing the PV generated power. However, the protection mode in battery module is waiting for the trigger signal when DC voltage becomes greater than 820V. At $t = 3.3$s, the latter is activated automatically and the DC voltage regulation loop is in operation. The DC voltages of the units are settled at 750V and the circulating power is eliminated as shown in Fig. 10b.

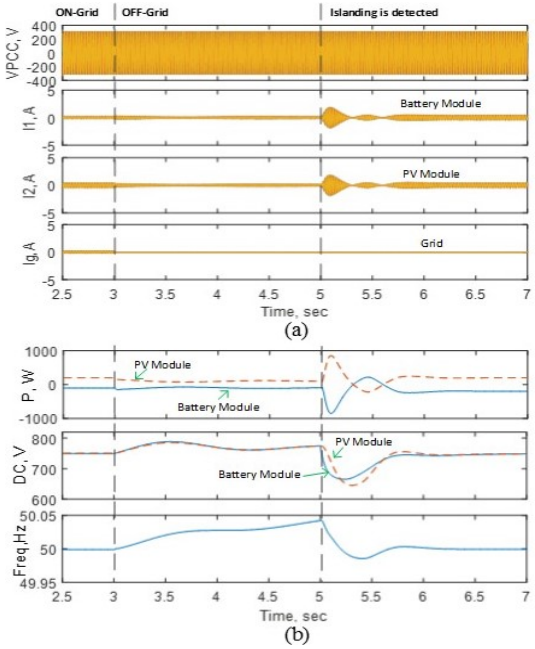

Fig. 11: Simulation results when battery is charging (a) PCC voltage, inverter output and grid current, (b) output active power and DC link voltage.

C. When Battery is charging

In Fig. 11, the PV power is 400W exported to grid. The battery is charging 200W in grid-connected mode. At $t = 3$s, the grid is lost and the transient circulating power flows from PV to battery. The control loop of the battery regulates output power and its setpoint before the islanding detection. As a result, the excess power circulates between the units and raising the DC voltages. PV power shifter acts immediately by reducing the PV generated power. However, the DC voltage of the battery unit does not reach the threshold (820V) and the protection loop is not activated. This reveals that the power shifter action is enough to bound the DC voltages and eliminate the circulating power.

VII. Experiment Implementation

A prototype has been used including two inverters and DC/DC converters. The energy sources are lead-acid battery and PV simulator. The control algorithms are realized

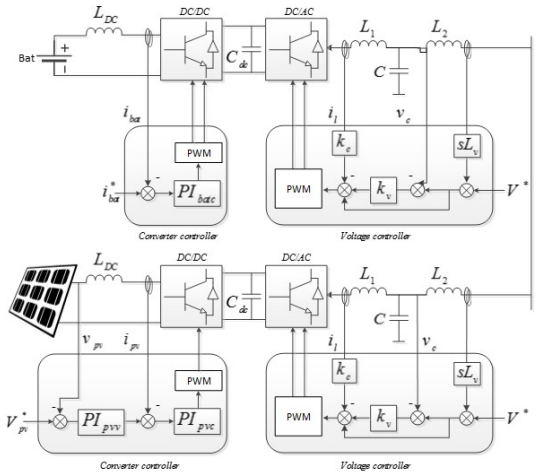

Fig. 12: Schematic diagram for voltage/current controller.

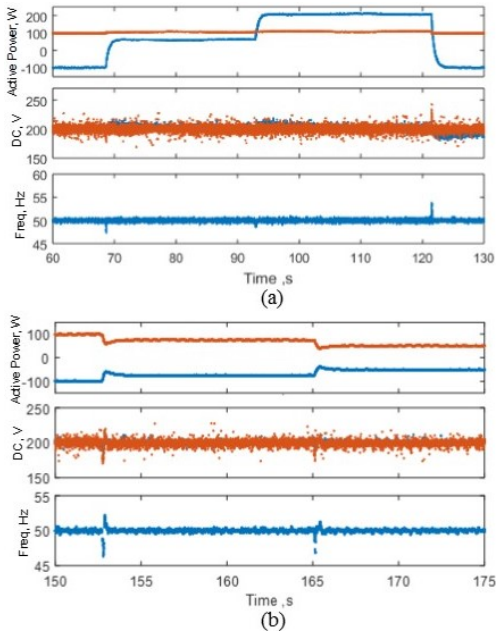

Fig. 13: Experiment results (a) under load changes in islanded mode, (b) when SC curtails the PV power operation.

by OPAL-RT. The first DC/DC converter was designed for bidirectional operation on charging and discharging modes whereas the second was designed as a boost converter with MPPT controller. The inner loops are shown in Fig. 12. The parameters are listed in Table II. The validity of the topology against unintentional islanding is examined by the same simulation cases. The test revealed the DC link voltage stability, the frequency regulation, and power flow between the inverters.

In Fig. 13a, the output power response is shown in islanded mode when 150W load at $t = 69$s was engaged and another 150W at $t = 93$s was engaged, then both were disconnected at 122s. After the detection of grid loss, the SC managed power sharing, the SOC control, the charging and discharging modes or the PV power curtailment by the communication means. Fig. 13b illustrates the power response, DC link voltage and frequency in islanded mode when the SC curtails PV power from 100W to 70W then to 50W.

Fig. 14a shows the experiment results when the battery module, in grid-connected mode, was generating 130W while the PV module was generating 100W. At $t = 5$s, the grid was lost and the PV voltage rises. The power shifter reduced the power but it was not enough to bound the voltage. Consequently, circulating power flowed between inverters ($t = [5 - 5.2]$s) charging the DC link capacitors toward the trip limits. However, the protection loop was activated automatically at 5.2s when the DC voltage exceeded 270V. This converted the battery to charging mode in order to absorb the PV power. Islanding detection was done manually at $t = 13$s to show the performance of the controllers over longer time. The frequency was regulated in islanded mode and the results confirm simulation expectations. The frequency response exceeded the 70Hz whereas the frequency is subject to the power imbalances in the microgrid as stated in (4). Practically, according to IEEE standards, only 2% is allowed and, here, the designer can switch to island mode (switch b)

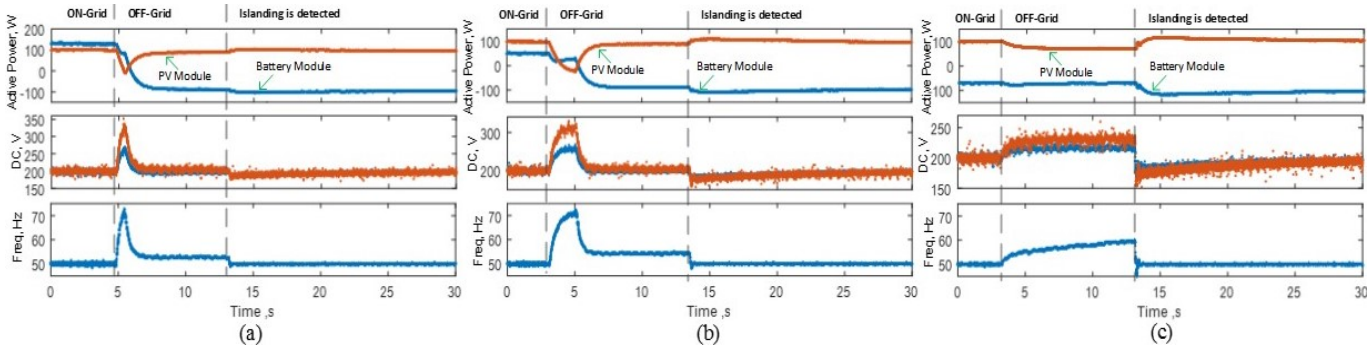

Fig. 14: Experiment results of unintentional islanding when (a) $P_{Battery} > P_{PV}$ (b) $P_{Battery} < P_{PV}$ (c) Battery is charging.

as it is one of the islanding detection techniques. However, the droop gains also can be selected smaller to reduce the frequency rise. In this paper, we chose to neglect the frequency rise just to validate the proposed protection mode operation.

In the second case, the battery and PV modules were generating 100W and 50W, respectively, as in Fig. 14b. At $t = 3$s, the grid was lost and the power flowed between the inverters. The proposed controller bounded the DC link voltages and saved the system from instability. The frequency loop regulation was enabled at $t = 13$s when the islanding was detected. In Fig. 14c, the battery module was in charging mode of 70W. After the grid lost at $t = 3$s, the DC link voltage of the PV raised and the PV power shifter reduced the generated power. However, the battery module DC voltage was under the threshold value (270V) and the frequency loop was enabled at $t = 13$s to work in islanded mode.

VIII. Conclusion

A control scheme structure for microgrid deploying battery-based ESS and PV-based RES is proposed in this paper. The new strategy aims to unify the control loops for all inverters in each mode of operation and for different energy sources to be DC voltage regulators. This structure immunizes the stability of the DC link voltage states and the overall reliability of the microgrid versus any sudden unplanned islanding. The control scheme was analyzed and tested by simulation and experiment. The limitation of the circulating current during the transition from grid-connected mode to islanded mode is achieved by the modes of ESS which is eventually supporting a smooth mode transfer and saving the DGs from any potential trip. However, the limitation of the proposed controller is the tradeoff between the selection of the frequency regulator gains and the frequency response which might exceed the standard limits. On the other hand, if the gains are selected to be high, this might destabilize the system. Furthermore, in high overshoot cases, the system switches to the protection mode which increases the transient damping from the DC converter side, but a low pass filter can be used to smooth the voltage.

TABLE II: Experimental setup parameters

Parameter	Value	Parameter	Value
L_1	$2mH$	k_v	5×10^{-3}
C	$25\mu F$	k_c	1
L_2	$1mH$	L_v	$8mH$
ω	$2\pi \times 50$	m	0.1
C_{dc}	$1100\mu F$	n	0.05
L_{DC}	$0.8mH$	k_{p_dc}	20
V_{bat}	$125V$	k_{i_dc}	2
V_{pv}	$110V$	V_{dc}	200
k_{p_batc}	5×10^{-3}	τ	0.5
k_{i_batc}	1	k_{p_p}	5×10^{-3}
k_{p_pvv}	1	k_{i_p}	5×10^{-3}
k_{i_pvv}	250	k_{p_ω}	0.1
k_{p_pvc}	0.05	k_{i_ω}	1
k_{i_pvc}	1	k_{dc_pro}	2
k_{pv_psS}	0.1	v_{dc_th}	270

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