

Memristive Effects in Oxygenated Amorphous Carbon Nanodevices

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Abstract.

Computing with resistive-switching (memristive) memory devices has shown much recent progress and offers an attractive route to circumvent the von-Neumann bottleneck, i.e. the separation of processing and memory, which limits the performance of conventional computer architectures. Due to their good scalability and nanosecond switching speeds, carbon-based resistive-switching memory devices could play an important role in this respect. However, devices based on elemental carbon, such as tetrahedral amorphous carbon or t-aC, typically suffer from a low cycling endurance. A material that has proven to be capable of combining the advantages of elemental carbon-based memories with simple fabrication methods and good endurance performance for binary memory applications is oxygenated amorphous carbon, or a-CO_x. Here, we examine the memristive capabilities of nanoscale a-CO_x devices, in particular their ability to provide the multilevel and accumulation properties that underpin computing type applications. We show the successful operation of nanoscale a-CO_x memory cells for both the storage of multilevel states (here 3-level) and for the provision of an arithmetic accumulator. We implement a base-16, or hexadecimal, accumulator and show how such a device can carry out hexadecimal arithmetic and simultaneously store the computed result in the self-same a-CO_x cell, all using fast (sub-10 ns) and low-energy (sub-pJ) input pulses.

1. Introduction

To keep pace with ever increasing computational demands and data volumes, faster and more energy-efficient memories are needed that can bridge the gap between fast but volatile DRAM and slow but non-volatile storage systems such as magnetic hard disks (HDDs). This form of bridging type memory system is commonly known as storage-class-memory (SCM) [1]. Several possible candidates for SCM applications have been reported, in particular resistive-switching, or memristive, memories using phase-change [2], metal-oxide [3] and, the focus of this work, amorphous carbon materials [4,5]. However, even if fast and reliable SCM systems were to be successfully developed, a more fundamental problem limits the performance of current computer systems, namely the need for the constant transfer of data between the central processor (CPU) and the memory in order to carry out logic and arithmetic operations. This physical separation between storage and memory, the so-called von-Neumann bottleneck, leads to limitations in computational speed and significant ‘wasted’ power; indeed, it has been estimated that over 50% of the power of modern computing systems is used simply to move data around the system [6-8].

One way to avoid the limitations caused by the von-Neumann bottleneck, or at least to ameliorate them, is carry out certain logic and arithmetic operations directly in the memory, assuming of course that the memory devices used can perform such operations. Fortunately, memristive devices have been shown to be capable of doing just this, with Boolean logic and arithmetic processing both having been successfully demonstrated in a variety of types [9,10]. The approach of using memristive devices for computation is one form of so-called memcomputing [11-14] which, as shown recently, can provide not only the same computational power as a universal Turing machine (describing all conventional digital computers), but also a range of additional and attractive properties including intrinsic parallelism, learning and adaptive capabilities [15].

A promising material that shows memristive behaviour potentially suitable for use in memcomputing applications is tetrahedral amorphous carbon (ta-C), which is of particular interest due to its scalability, chemical stability, sustainability, fast switching speed and low power consumption [16-18]. Tetrahedral amorphous carbon can be reversibly switched between high resistance (HRS) and low resistance (LRS) states by applying electrical pulses [4, 19]. In the LRS state, electrical conduction is thought to occur through a conjugated network of sp^2 -bonded carbon clusters that form a conductive filament between the device electrodes [4, 20-22]. The formation of such a filament is suggested to be a consequence of localized thermally-driven sp^3 to sp^2 bond re-hybridization [14, 23]. Switching from the LRS to the HRS state requires a breaking of the conductive filament, which is usually achieved using fast electrical pulses with very short fall times [16, 17]. However, the number of times elemental carbon memory devices can

be repeatedly switched between LRS and HRS states is fairly limited, due primarily to the strong thermodynamical stability of the sp^2 -bonded state; essentially the conducting sp^2 filament grows relatively easily and becomes hard to break after a relatively small number (tens to hundreds) of switching cycles [4, 16, 17]. To overcome this limitation, elemental amorphous carbon has recently been highly doped with oxygen to suppress the formation of C-C sp^2 bonds, with such oxygenated amorphous carbon (a-CO_x) memories demonstrating successful switching over many tens of thousands of cycles [18].

The switching mechanism in a-CO_x memories is thought to be (mainly) electrochemical in nature (rather than electrothermal, as in the case of ta-C) and involve an electrochemical reduction-oxidation (redox) of carbon. To switch from the HRS to the LRS state, a voltage pulse is applied across the device electrodes and oxygen migrates towards the positive electrode, leading to the formation of strongly reduced and highly conductive sp^2 -rich filament(s). To switch back from the LRS to the HRS state, an opposite polarity voltage pulse is applied and oxygen migrates back towards the opposite electrode, helping to disrupt the sp^2 -bonded conductive filament (by inducing carbon sp^3 hybridization –see [18] for further details of the switching mechanism). Switching in a-CO_x devices is essentially bipolar, in common with many other forms of resistive memories [3, 24, 25], whereas in ta-C devices switching is unipolar.

To date however, investigations of a-CO_x based resistive-switching type devices has been limited primarily to non-volatile binary memory applications. Here, by contrast, we examine their memristive capabilities, in particular their ability to provide the multilevel and accumulation properties that underpin memcomputing type applications [10, 11, 13, 14, 26].

2. Device fabrication and electrical testing methods

The a-CO_x devices were fabricated on top of a 500 nm thick SiO₂ electrical insulating layer, which was thermally grown on top of a silicon substrate. The bottom electrode (BE) consisted of a 60 nm thick tungsten layer, deposited on top of a 10 nm Ti adhesion layer. A further SiO₂ layer (35 nm thick) was deposited on top of the bottom electrode and patterned with cylindrical openings into which the a-CO_x layer was deposited using magnetron sputtering from a solid carbon source in a mixed O₂ and Ar atmosphere (the second SiO₂ layer provides thermal and spatial confinement of the a-CO_x region and helps to prevent any significant outgassing of oxygen). Devices with a-CO_x regions of sizes (diameters) ranging from 50 nm to 200 nm were fabricated, with the a-CO_x layer itself being 18 nm thick. A top electrode (TE) consisting of a 100 nm Pt layer completes the basic device structure. On-chip, small-footprint, resistors were fabricated in series with each device to reduce the flow of parasitic current through the device during switching events. Gold interconnects and pads are also deposited to allow for

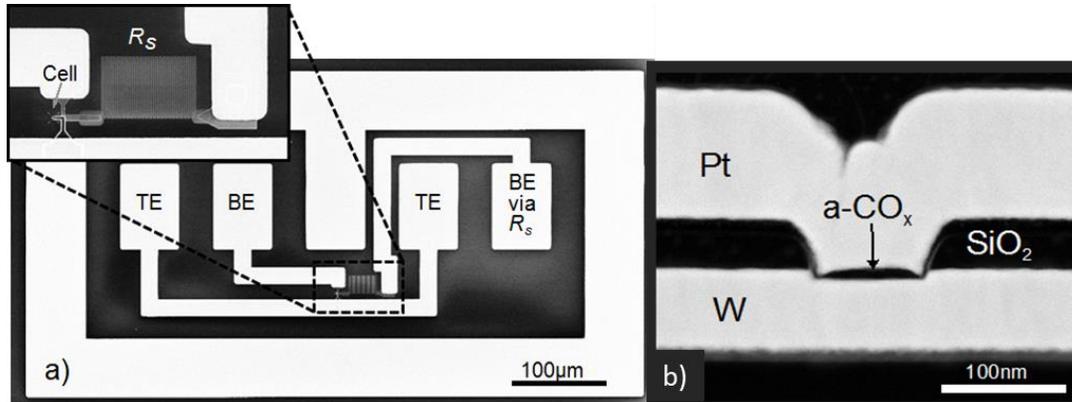


Figure 1. (a) SEM top view of the top (TE), bottom (BE) and ground electrodes, which are used to electrically probe the a-CO_x cells (R_s is the on-chip series resistor). (b) STEM cross-sectional image of an exemplar a-CO_x cell, here having a diameter of 100 nm. (Reprinted with permission and modified from [18]; copyright Nature Publishing Group 2015).

probe-testing of the devices. Electron microscope images of a complete device showing the overall cell and electrode configuration is given in Fig. 1(a); a cross-section of an individual cell is in Fig. 1(b).

The devices have a GSSGSSG (G = ground, S = signal) layout, which allows for connection via two different electrical paths. One path is via the on-chip series resistor and is used during SET processes (i.e. when switching from high to low resistances). The other path does not include the series resistor and is used for RESET switching (i.e. when switching from low to high resistances). Voltage pulses for switching were supplied by an Agilent 81150A Arbitrary Waveform Generator and captured with a Tektronix TDS3054B oscilloscope. During the application of a voltage pulse the top electrode was grounded. The read out of the device resistance was carried at 0.2 V DC using a Keithley 2400 sourcemeter. To contact the device chip pads, low capacitance Dual-Z probes (Cascade) were used. The capacitance of the device including the probing station was evaluated as being approximately 40 fF. The measurement of device characteristics at elevated temperatures was carried out by mounting the chip onto an invar block with in-built tungsten heaters, the temperature being recorded using a thermocouple and controlled by a Eurotherm temperature controller.

3. Results and discussion

3.1 Thermal annealing

As discussed in the previous section, non-volatile memories based on amorphous carbon alone (ta-C memories) suffer from a relatively poor endurance (limited number of switching cycles) due to the

propensity of the sp^2 filaments (formed during the switching to the LRS state) to grow in size during each switching cycle, leading to devices becoming ‘stuck’ in the SET (LRS) state [16, 17]. This is perhaps not surprising, since it is well-known that the electrical resistivity of ta-C films always decreases upon thermal annealing [21, 27, 28]. However, in the case of memories based on a-CO_x films, we might expect a different kind of thermal behavior, due to the role played by oxygen atoms in the switching process.

To confirm (or otherwise disprove) the expectation of a different thermal dependence of resistance for a-CO_x based devices than for ta-C films and devices, we first SET an a-CO_x device into the LRS state ($R = 3.6 \text{ k}\Omega$) via an I-V sweep (see Fig. 2(a)) and then monitored the device resistance during various heating and cooling cycles. In Fig. 2(b) we show results for a device heated from 40°C up to 300°C (at 2°C per minute), being held at 300°C for 5 minutes, and then cooled down (at the same rate). Between 40°C and 236°C the resistance decreases with temperature and shows, as previously observed [18], a thermally-activated behaviour that can be well described by $\log R \sim E_a / (k_B T)$ with E_a being the activation energy for conduction (here $E_a = 36 \text{ meV}$), k_B the Boltzmann constant and T the temperature in Kelvin. Between 236°C and 300°C however, the resistance of the a-CO_x device increases, with the increase being quite dramatic (three orders of magnitude) between 260°C and 300°C. Such increases of resistance with temperature are in stark contrast to that reported for films and devices based on elemental carbon, where the resistance decrease continuously with increasing temperatures [20, 21, 29, 30]. The resistance increase with increasing temperature in the a-CO_x case can be linked to a re-distribution of oxygen within the cell during heating, with the oxygen breaking up the low-resistivity C–C sp^2 (graphite-like) rings and inducing high-resistivity C sp^3 (diamond-like) hybridization (see [18]). Upon cooling down to 40°C, the resistance of the a-CO_x devices followed again a $\log R \sim E_a / (k_B T)$ type behavior, with an activation energy in this case of $E_a = 93 \text{ meV}$. The low value of the activation energy, together with the high resistance of the device, suggests that electrical transport mainly dominated by hopping between localised states [31-33].

The findings of Fig. 2(b) indicate that, in addition to the electrochemical mechanism already identified [18] as the main driving force for the resistive switching process in a-CO_x based devices, there is most likely also a thermal component involved in the switching, most probably as a result of thermally-driven diffusion of oxygen ions. In any case, the results of Figs. 2(a) and 2(b) indicate that, by appropriate control of a-CO_x cell excitation conditions, it should be possible to access intermediate resistance levels, lying between the LRS and the HRS states, something that has not been reported to date. We explore this possibility in the next sections.

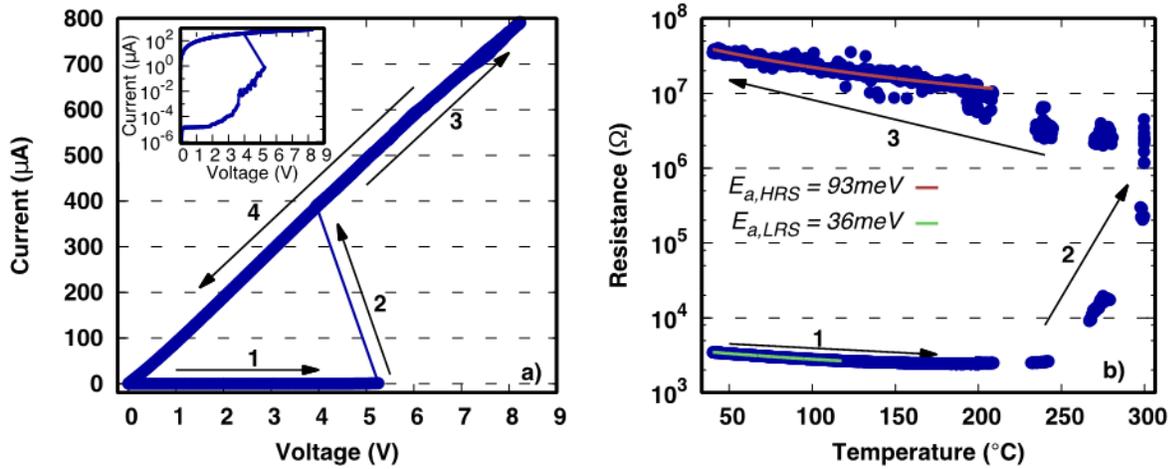


Figure 2. (a) I-V curve for an a-CO_x device (used to SET the device into LRS state for the measurements reported in (b)). The voltage was measured across the device itself (i.e. with the voltage drop across the series resistor subtracted) and the inset shows the I-V curve with the current on a log scale. (b) The variation of resistance as a function of annealing temperature for the device of (a) in the LRS state.

3.2. Multilevel states

To evaluate the possibility of accessing multilevel resistance states, a-CO_x devices were SET into the LRS state (via an I-V sweep), input excitations (voltage pulses) of various amplitudes and durations were applied, and the resulting device resistance measured. Typical results are shown in Fig. 3(a). Here, the device was first cycled six times between a partial RESET state, with a resistance of roughly (on average) 1 MΩ, and the SET state by a sequence of (partial) RESET pulses having a duration of 7 ns and an amplitude of -2.1 V (top electrode grounded) and SET pulses of 60 ns duration and 3.2 V amplitude. Following this, a sequence of seven 7 ns/-2.5 V RESET pulses was applied, again interleaved with 60 ns/3.2 V SET excitations, and a significantly higher HRS resistance of around (on average) 50 MΩ was achieved. The results of Fig. 3(a) show that multilevel states can indeed be accessed in a-CO_x devices, although in this case cycle-to-cycle variation in resistance is not insignificant. Nonetheless three distinct and readily distinguishable resistance levels are observed, equivalent to the storage of 1½ bits per cell (specifically, in this case, the 0-level (SET level) has resistances between 41 kΩ to 88 kΩ, the 1-level (partial RESET level) has resistances between 450 kΩ to 2.7 MΩ and the 2-level (full RESET) lies between 9.5 MΩ and to 59 MΩ). The multilevel resistance states are also stable with time, as can be seen in Fig. 3(b). Note that the results of Fig. 3(b) were for a different, larger device than that shown in Fig. 3(a), but one that was programmed into the same resistance levels. Also note that the resistance states did not become unstable after 10,000 seconds, it is just that we stopped collecting data after this point.

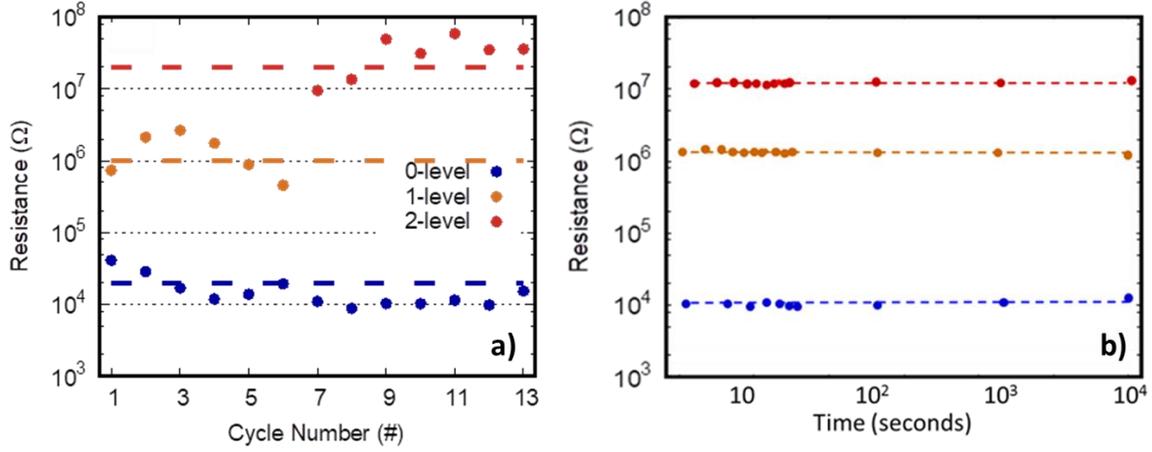


Figure 3. (a) Cycling between multilevel resistance states in a- CO_x devices. Here three programmed states are shown, one LRS (0-level) state and two HRS (1-level and 2-level) states. The 0-level is accessed (programmed) using 60 ns/3.2 V pulses, while the 1-level and 2-level states are accessed using 7 ns/-2.1 V and 7 ns/-2.5 V pulses respectively. (b) Variation of the resistance of multilevel states as a function of time. Note that the results of (b) were for a different, larger device than that shown in (a) (but one that was programmed into the same resistance levels). Note also that the dashed lines in (a) and (b) are simply guides for the eye.

3.3 Low energy accumulation-based memcomputing

The exploitation of accumulation properties has previously been used successfully in phase-change memory type devices to carry out addition, subtraction, multiplication and division directly in high-order bases (e.g. base-10), as well as more complex arithmetic processing such as parallel factorization [10, 11, 33]. Moreover, once such arithmetic computations are completed, the result is automatically stored in the device (which was in itself a non-volatile memory) that carried out the calculation. Thus, processing and memory can be carried out simultaneously by one and the same device, providing a form of computing-in-memory, or memcomputing [13,14,15]. An alternative view of this kind of processing is as a form of non-von Neumann computing, in which the need (of a conventional von Neumann computer) to constantly transfer data between the processing unit and an external memory is removed, so potentially saving significant amounts of energy and potentially increasing computation speeds.

The basic process of accumulation-based computing involves the excitation of a memory-type device by a predetermined number of identical electrical pulses. The excitation pulses are configured (in amplitude and duration) such that only after all pulses of the predetermined sequence have been applied does the resistance of the cell change significantly enough (either in transitioning from the HRS to the LRS state, or vice-versa) to cross a pre-set resistance decision threshold. The number of pulses required to pass

through the decision threshold determines the arithmetic base of the calculation. Thus, for base- n operation, a decision threshold is set between the resistance levels achieved after the input of $(n-1)$ and n pulses. Note that, unlike in the case for multilevel storage, accumulation does not require that *all* individual resistance levels are distinguishable, merely that it is possible to (reliably and repeatably) determine that the pre-set resistance threshold has been reached/passed. This in turn requires that (or at least is easier to do if) the cell resistance changes monotonically as the number of input pulses increases, and that the ‘window’ between the resistances of the cell after the input of $(n-1)$ and n input pulses is sufficiently large.

To determine if a-CO_x memory-type devices possess properties making them suitable for accumulation based computing, we first SET a device into the LRS state via an I-V sweep (in this case leading to a SET resistance of ~ 2.5 k Ω). We then applied a series of short (8 ns), low voltage (-0.9 V) input pulses, measuring the resistance after each applied pulse. The results are shown in Fig. 4(a), here for the case of 30 successive input pulses. The variation in resistance with pulse number displays a sigmoidal-like response, which is well-suited to the implementation of an accumulator [10]. Moreover, between pulses 13 and 16 the resistance changes are well separated, allowing the ready placement of a suitable detection threshold. For example we could, as shown in Fig. 4(a), place the decision threshold between state-15 and state-16 (since the resistance window between those states is relatively large) and this would yield a base-16, or hexadecimal, accumulator. Such an accumulator would also have relatively low energy consumption, since the energy consumed per input pulse is around the pJ level or lower (see Fig. 4(b)).

Methods for carrying out specific arithmetic operations (addition, subtraction, multiplication, division etc.) using such an accumulator have been described in previous work (see e.g. [10, 11, 34]), so are not repeated in detail here. However, for completeness and context we consider the process of hexadecimal addition using a response of the form shown in Fig. 4(a). For example, should we wish to add 7_{10} and 11_{10} (i.e. $7 + B$ in hexadecimal notation) we would first input 7 pulses (the augend of the addition we wish to carry out) to an a-CO_x cell having the accumulator response of Fig. 4(a); this would take the cell to state-7 on the R vs. pulse number curve. We would then input pulses equal in number to the addend (11_{10}). However, in this case after receipt of pulse #9 of this addend sequence of 11 pulses, the cell resistance would cross the pre-set decision threshold (set between state-15 and state-16), this would be detected (by additional circuitry) and the cell would be SET back to the LRS state before the remaining addend pulses (i.e. pulses #10 and #11) were inputted. After completion of this whole process the a-CO_x cell would be in state-2, and one SET process would have been carried out. By this means the cell has computed the addition $7 + B$ in hexadecimal and the result is given by the number of times the cell has been SET (due

to passing the decision threshold) along with the number stored in the cell itself. To access this stored number we input further identical pulses to the cell until it again crosses the decision threshold. Fourteen (14) pulses would be needed in this case, which is the (base-16) complement of the number we require (2). Thus $7_{10} + 11_{10} = 18_{10}$ (or in hexadecimal, $7 + B = 12$). Note that although the readout of the number stored in an accumulation cell by inputting additional pulses essentially ‘erases’ that cell, in a computing application the accumulation cell would be storing intermediate results of a calculation and its state would not necessarily need to be read during such calculations (e.g. if we add say $2 + 3 + 4$ using an accumulation cell, we do not need to readout the cell resistance at any point during this calculation). On a more general level we also note that the data stored in a cell is not in fact ‘lost’ when a cell is read, since the number of pulses needed to take a cell to threshold during reading provides a copy (albeit in the form of the complement of the stored number) of that stored data, which could be easily written back to the same (or a different cell) should this be required.

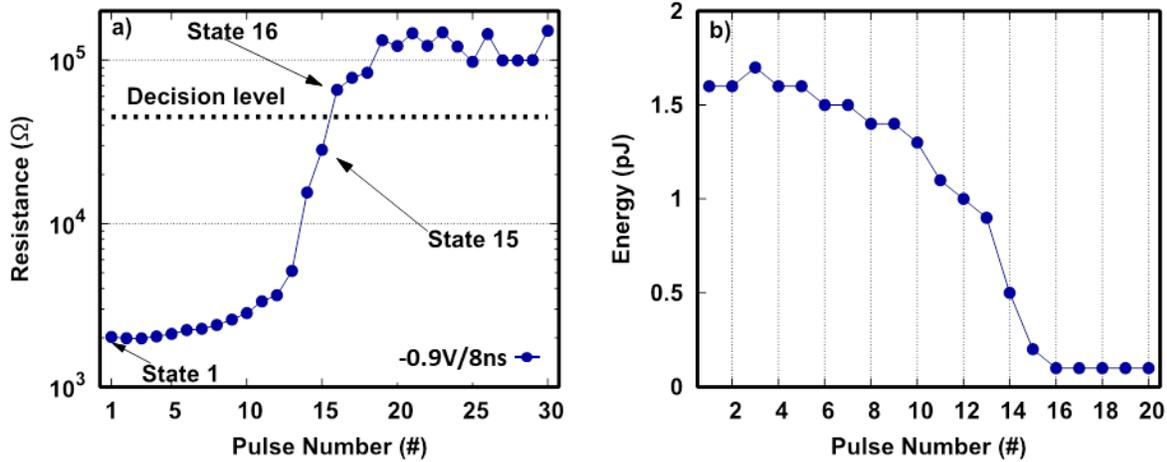


Figure 4. (a) An accumulator-type response in an a-CO_x memory cell obtained by the input of a series of identical -0.9 V/ 8 ns pulses. Also shown is position of a (resistance) decision threshold for use as a base-16 accumulator. (b) The energy consumed per pulse (first 20 pulses only shown) for the accumulator of (a).

To carry out the accumulator based computation of the hexadecimal addition ($7_{16} + B_{16}$) as above requires additional circuitry for both the detection of the crossing of the (resistance) decision threshold, the recovery of a number from its complement and the carry-over operation. However, such circuitry is not necessarily complicated; for example crossing of the decision threshold could be achieved by standard circuits used for resistive memory readout, in tandem with a comparator, while the generation of a number from its complement can be achieved by using a complementary accumulator cell (see [10]). The carry-over can be implemented simply by passing (writing) the carry-over(s) to a second cell representing

the next highest power in the base (see e.g. [35]). Moreover, we should not lose sight of the fact that the major benefit of using the accumulator approach is that a single nanoscale a-CO_x memory cell has, in the above example, carried out the core part of the task of adding two hexadecimal numbers and, importantly, stored the result in the self-same cell. Furthermore the process is relatively fast (we used 8 ns pulses here, but faster operation could no doubt be achieved), fairly energy efficient (~ 1 pJ per pulse) and easily parallelised (for the provision of multi-integer or fixed-point numbers). Thus, it would seem that a-CO_x memory-type devices are potentially well-suited to computing-in-memory, or memcomputing type operations. In comparison, the addition of hexadecimal numbers by conventional approaches would require a 4-bit full adder comprising around 20 logic gates in total, and would of course not provide the beneficial feature of simultaneous, co-located storage of the result.

While we have above used the example of an accumulator arranged for base-16 or hexadecimal operation, other bases can of course be implemented by using different input pulse amplitudes and/or durations. Indeed, since for a reliable implementation of accumulation-based arithmetic it would be important to achieve excellent repeatability in terms of the accumulator switching (i.e. the number of pulses required to reach the threshold should not vary either in a single cell from calculation to calculation or between cells in a large-scale array), then the use of accumulators designed to work with lower-order bases is likely to be more practicable (as was shown in the case of phase-change accumulators [34]).

In addition we note that programming the accumulator response as a form of gradual RESET (i.e. moving from the LRS to the HRS state) not only unlocks the high switching speeds inherent to the RESET process, but leads to a reduction in energy consumption as a computation proceeds. This is due to the decreasing current flow with increasing pulse number, as shown in Fig. 5. Indeed, after around 20 input pulses the switching current is here comparable to the noise in the measurement circuit. Of course for reliable computation using this gradual RESET approach, the intermediate resistances need to exhibit a certain degree of stability. Since, as we have shown in Fig. 3(b), the intermediate resistance states obtained for the a-CO_x cell programmed into multilevel states were stable, then it is reasonable to assume that the intermediate states in the accumulator response are also stable. However, it should also be pointed out that it is not the primary aim for the accumulation cell to provide long-term memory, rather that it provides in-situ storage of intermediate results during arithmetic calculations, so avoiding the need to transfer such intermediate results to external (or cache) memory.

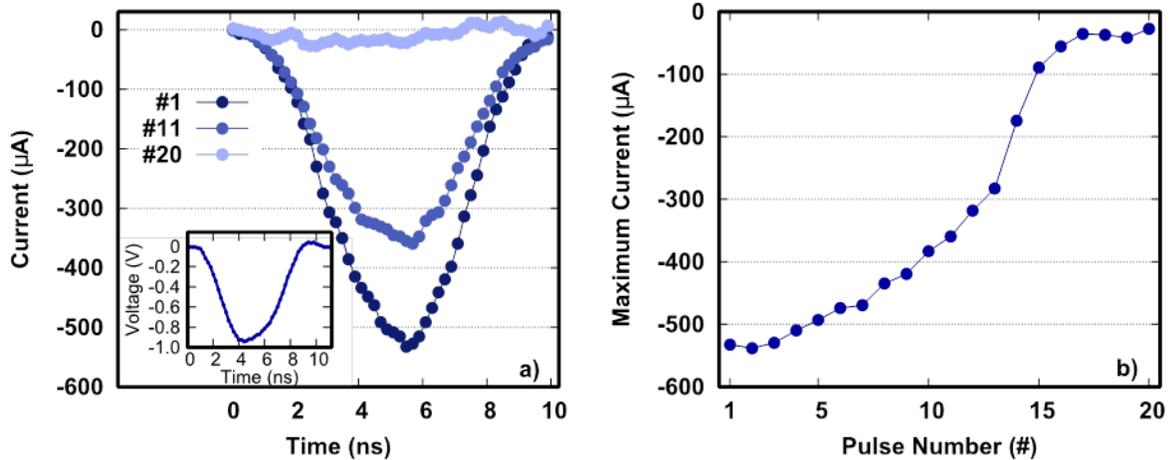


Figure 5. (a) The switching current in the a-CO_x accumulator of Fig. 4(a) for input pulse #1, #11 and #20 (inset shows the applied voltage pulse). (b) The variation of (maximum) current during accumulator switching as a function of input pulse number.

4. Conclusions

In summary, we have shown that simple two-terminal, nanoscaled, oxygenated amorphous carbon, or a-CO_x, devices, in addition to their previously demonstrated non-volatile binary memory functionality, possess memristive type capabilities including the ability to provide the multilevel and accumulation properties that underpin computing type applications. Specifically we successfully demonstrated the storage of 3-levels (1½ bits) per individual cell, as well as an accumulator-like response suited to the provision of arithmetic processing. We implemented a base-16, or hexadecimal, accumulator and showed how such a device can carry out hexadecimal addition and simultaneously store the resulting sum in a single a-CO_x cell, all using fast (sub-10 ns) and low-energy (sub-pJ) input pulses.

Acknowledgments

This work was funded by the EU Research & Innovation project CareRAMM, grant no. 309980. The authors would like to thank all collaborators and colleagues involved in this project for useful discussions.

References

- [1] Burr G W, Kurdi B N, Scott J C, Lam C H, Gopalakrishnan K and Shenoy R S 2008 *IBM Journal of Research and Development* **52** 449–464
- [2] Burr G W, Breitwisch M J and Franceschini M 2010 *Journal of Vacuum Science & Technology B* **28** 223-62.
- [3] Waser R and Aono M 2007 *Nature materials* **6** 833–840

- [4] Fu D, Xie D, Feng T, Zhang C, Niu J, Qian H and Liu L 2011 *IEEE Electron Device Letters* **32** 803–805
- [5] Bachmann T, Alexeev A, Koelmans W, Zipoli F, Ott A, Duo C, Ferrari A, Nagareddy V K, Craciun M, Jonnalagadda P, Curioni A, Sebastian A, Eleftheriou E and Wright C D 2017 *IEEE Transactions on Nanotechnology*
- [6] Backus J 1978 *Communications of the ACM* **21** 613–641
- [7] Wong H S P and Salahuddin S 2015 *Nature Nanotechnology* **10** 191–194
- [8] Borkar S and Chien A A 2011 *Communications of the ACM* **54** 67–77
- [9] Borghetti J, Snider G S, Kuekes P, Yang J J, Stewart D R and Williams R S 2010 *Nature* **464** 873–876
- [10] Wright C D, Liu Y, Kohary K I, Aziz M M and Hicken R J 2011 *Advanced Materials* **23** 3408–3413
- [11] Wright C D, Hosseini P and Diosdado J A V 2012 *Advanced Functional Materials* **23** 2248–2254
- [12] Burr G W, Shelby R M, Sebastian A, Kim S, Kim S, Sidler S, Virwani K, Ishii M, Narayanan P, Fumarola A, Sanches L L, Boybat I, Le Gallo M, Moon K, Woo J, Hwang H and Leblebici Y 2016 *Advances in Physics: X* **2** 89–124
- [13] Le Gallo M, Sebastian A, Mathis R, Manica M, Tuma T, Bekas C, Curioni A and Eleftheriou E 2017 arXiv.org arXiv:1701.04279 (Preprint 1701.04279)
- [14] Sebastian A, Tuma T, Papandreou N, Le Gallo M, Kull L, Parnell T, Eleftheriou E 2017 <https://arxiv.org/abs/1706.00511v1>
- [15] Di Ventra M and Pershin Y V 2013 *Nature Physics* **9** 200–202
- [16] Koelmans W W, Bachmann T, Zipoli F, Ott A K, Dou C, Ferrari A C, Cojocaru-Mirédin O, Zhang S, Scheu C, Wuttig M, Nagareddy V K, Craciun M F, Alexeev A M, Wright C D, Jonnalagadda V P, Curioni A, Sebastian A and Eleftheriou E 2016 Carbon-Based Resistive Memories 2016 *IEEE International Memory Workshop (IMW)* 1–4
- [17] Kreupl F, Bruchhaus R, Majewski P, Philipp J B, Symanczyk R, Happ T, Arndt C, Vogt M, Zimmermann R, Buerke A, Graham A P and Kund M 2008 *IEEE International Electron Devices Meeting (IEDM)* 1–4
- [18] Santini C A, Sebastian A, Marchiori C, Jonnalagadda V P, Dellmann L, Koelmans W W, Rossell M D, Rossel C P and Eleftheriou E 2015 *Nature Communications* **6**, 8600
- [19] Xu J, Xie D, Feng T, Zhang C, Zhang X, Peng P, Fu D, Qian H, Ren T I and Liu L 2014 *Carbon* **75**

255–261

[20] Takai K, Oga M, Sato H, Enoki T, Ohki Y, Taomoto A, Suenaga K and Iijima S 2003 *Physical Review B* **67** 214202–11

[21] Ferrari A C, Kleinsorge B, Morrison N A, Hart A, Stolojan V and Robertson J 1999 *Journal of Applied Physics* **85** 7191

[22] Sebastian A, Pauza A, Rossel C, Shelby R M, Rodríguez A F, Pozidis H and Eleftheriou E 2011 *New Journal of Physics* **13** 013020

[23] Grierson D S, Sumant A V and Konicek A R 2010 *Journal of Applied Physics* **107** 033523

[24] Ielmini D and Waser R 2015 *Resistive switching: from fundamentals of nanoionic redox processes to memristive device applications* (Somerset: Wiley).

[25] Wouters D J, Waser R and Wuttig M 2015 *Proceedings of the IEEE* **103** 1274–1288

[26] Traversa F L and Di Ventra M 2015 *IEEE Transactions on Neural Networks and Learning Systems* **26** 2702–2715

[27] Sullivan J P, Friedmann T A and Baca A G 1997 *Journal of Electronic Materials* **26** 1021–1029

[28] Silva S R P 2003 *Properties of Amorphous Carbon* (IET)

[29] Adkins C J, Freake S M and Hamilton E M 1970 *Philosophical Magazine* **22** 183–188

[30] Robertson J 2002 *Materials Science & Engineering R-Reports* **37** 129–281

[31] Godet C 2002 *Journal of Non-Crystalline Solids* **299** 333–338

[32] Godet C 2003 *Philosophical Magazine Letters* **83** 691–698

[33] Baranovski S 2006 *Charge Transport in Disordered Solids with Applications in Electronics* (Chichester, UK: Wiley).

[34] Hosseini P, Sebastian A, Papandreou N, Wright C D and Bhaskaran H 2015 *IEEE Electron Device Letters* **36** 975–977

[35] Feldmann J, Stegmaier M, Gruhler N, Ríos C, Bhaskaran H, Wright C D, Pernice W H P 2017, *Nature Communications*, doi: 10.1038/s41467-017-01506-3 (in press)