Nanoscale Carbon-Based Memory Devices

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to my family

List of Publications

- W. W. Koelmans, T. Bachmann, F. Zipoli, A. K. Ott, C. Dou, A. C. Ferrari, O. Cojocaru-Mirédin, S. Zhang, C. Scheu, M. Wuttig, V. K. Nagareddy, M. F. Craciun, A. M. Alexeev, C. D. Wright, V. P. Jonnalagadda, A. Curioni, A. Sebastian, and E. Eleftheriou, "Carbon-Based Resistive Memories," in 2016 *IEEE* 8th *International Memory Workshop (IMW)*, pp. 1–4, IEEE, 2016. *DOI: 10.1109/IMW.2016.7493569*

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Abbreviations

Central Processing Unit	CPU
Static-Random Access Memory	SRAM
Dynamic-Random Access Memory	DRAM
Storage-Class Memory	SCM
International Technology Roadmap for Semiconductors	ITRS
Metal-Oxide-Semiconductor Field-Effect Transistor	MOSFET
Ferroelectric Random-Access Memory	FeRAM
Phase-Change Random-Access Memory	PRAM
Ovonic Threshold Switch	OTS
Magnetic Random-Access Memory	MRAM
Magnetic Tunnel Junction	MTJ
Spin Transfer Torque Random-Access Memory	STT-MRAM
Multi-Level Cell	MLC
Conductive Bridging Memory	CBRAM
Redox-Based Resistive Random-Access Memory	ReRAM
Low Resistance State	LRS
High Resistance State	HRS

Valence Change Memory	VCM
Thermochemical Memory	TCM
Amorphous Carbon	a-C
Tetrahedral Amorphous Carbon	ta-C
Diamond-Like Carbon	DLC
Filtered Cathodic Vacuum Arc	FCVA
Pulsed Laser Deposition	PLD
Mass Selected Ion Beam	MSIB
Direct Current	DC
Radio Frequency	RF
Ultra-Violet	UV
Density-Of-States	DOS
Variable-Range Hopping	VRH
Trap-Limited Band (Transport)	TLB
Molecular Dynamic	MD
Seventh Framework Programme	FP7
Carbon Resistive Random Access Memory Materials	CareRAMM
Oxygenated Amorphous Carbon	a-CO_x
Device-Under-Test	DUT
Finite Element	FE
Energy-Dispersive X-ray Spectroscopy	EDX

(Scanning) Transmission Electron Microscope	(S)TEM
High-Angle Annular Dark Field	HAADF

Abstract

Amorphous carbon-based memories have gained traction in recent years due to their good scalability and switching performance and are an important contender to close the performance gap between fast but volatile DRAM and slow but non-volatile flash memory. A writing and erasing process driven by the electrically induced formation and rupture of a conductive filament permits switching times in the range of a few nanoseconds. Further, the memristive property of amorphous carbon allows the implementation of beyond von Neumann computation paradigms. However, 'pure' amorphous memories have a low cyclic endurance. To overcome this and to exploit beyond von Neumann computation, devices based on oxygenated amorphous carbon were employed here.

The first part of this thesis evaluated the switching performance and data retention capabilities of tetrahedral amorphous carbon memories. Switching times below 10 ns were achieved for the SET as well as for the RESET times. An energy consumption below 1 pJ was obtained, while data could be retained for more than 300 s at 450 °C. Further, evidence was provided that the SET process is not induced by an electric field alone.

A finite-element simulation was employed in the second part of this thesis to reproduce the experimentally determined conductivity of tetrahedral amorphous carbon (ta-C) memory devices and to shine light on the conditions at the onset switching from the high to low resistance states (dielectric breakdown). The maximum temperature observed at dielectric breakdown was 1615 K. It was found that a reduction of the lateral cell radius from

25 nm to 15 nm and 10 nm increases the switching performance by reducing the switching current from 34 µA to 20 µA and 8 µA.

The third part of this thesis evaluated the switching performance, temperature stability, multilevel storage and memcomputing capabilities of oxygenated amorphous carbon. Switching times below 10 ns for both, SET and RESET were demonstrated. A 3-level (1½ bits) data storage was achieved using three different resistance states. Further, a memcomputing approach was implemented using a base-16 accumulation response with energy consumptions as low as <100 fJ per pulse. Additionally, a finite element simulation of a device in the low resistance state (LRS) was used to illustrate the correlation between device resistance and Joule heating effects.

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Chapter 1

Introduction

1.1 Motivation

In recent years, the extent to which electronic communication devices have revolutionised our daily life in the form of smartphones, laptops, on demand streaming services, to name a few, is truly striking. This technological revolution was only possible due to ever increasing computational power being available at lower costs, lower energy and power consumption and in smaller and smaller dimensions. The driving force behind this success story is the doubling of the number of transistors that can be integrated in chips every 18 months to 24 months, which has been described as Moore's law [1, 2].

With electronic devices pervading almost every aspect of our lives, the demand for high density, cheap, fast and energy efficient data storage becomes increasingly important. To balance the trade-off for cheap, high density data storage on one hand, and the need for fast access, high performing storage devices on the other hand, different types of memories are currently employed. The size of a given memory design is expressed by its lateral dimensions in multiples of F^2, where F is the smallest lithographic feature size [3]. An often used criterion that allows one to split different types of memories into two categories is the capability to retain data.

High performance memory is located in close proximity to the central processing unit (CPU) and requires constant power supply to retain the data and hence, falls into the category of volatile memory. The volatile memory that is typically used for fast CPU access and caching is static-random access memory (SRAM) [4]. One level lower in the hierarchy of memories is dynamic-random access memory (DRAM) which is more compact in comparison to SRAM, but slower due to periodical refresh operations that have to be carried out to account for charge leakage [3, 5].

One step lower in the memory hierarchy are memories that fall into the second category and are non-volatile. Non-volatile memories have longer read, write and erase times, but can retain data without refreshing cycles or a constant power supply [6]. They are cheaper in fabrication and offer a higher storage density due to a compact design.

The most ubiquitous current non-volatile memory devices are those based around CMOS Flash technology. However, the speed difference between accessing DRAM and the write-cycle time of Flash is around 4 orders of magnitude, which causes a significant delay between performing logic operations (CPU) and storing the resulting data [7]. The access time for different memory technologies is given in a memory hierarchy diagram in Figure 1.1 [7].

In addition to the speed limitations of Flash-based memory, also the number of re-write processes (endurance cycles) is limited to around 1000 [8]. To fill the performance gap between DRAM and Flash in the memory hierarchy a new class of memory is required. This class of memory is referred to as storage-class memory (SCM) [7]. The limitations of DRAM and NAND Flash are compared in Table 1.1, together with the demands for SCM.

The most promising memory candidates that have the potential to bridge the performance

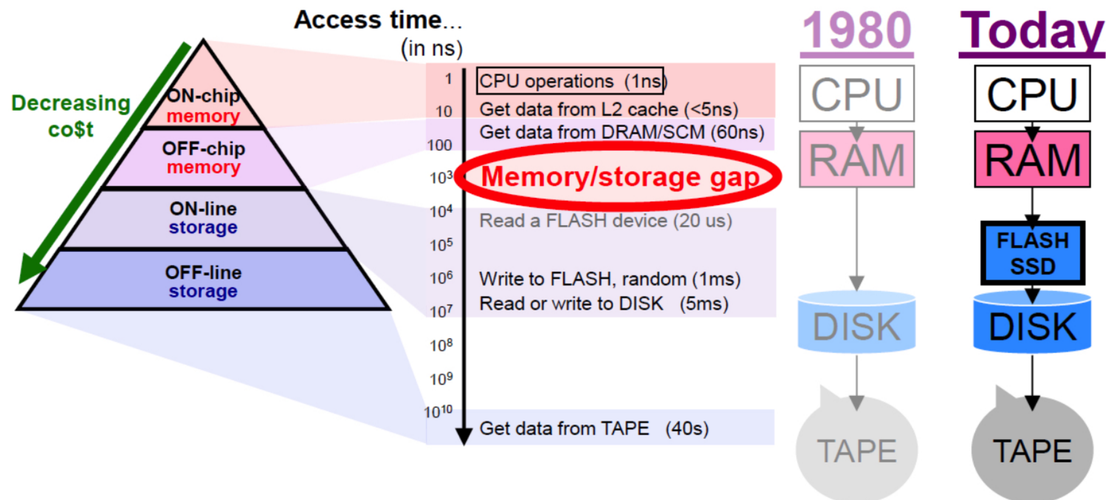


Figure 1.1: Memory hierarchy and target application for storage-class memory (SCM) [11, 12].

gap between fast, but volatile memory and traditional non-volatile memories are shown in the memory taxonomy in Figure 1.2, which is an adapted version of the International Technology Roadmap for Semiconductors (ITRS) [9, 10]. The non-volatile memories are split according to their current development state into prototypical and emerging memories. An overview of prototypical and emerging SCMs is provided in Sections 1.3 and 1.4, with the focus on technical approach, performance, data storage characteristics, energy consumption and scalability.

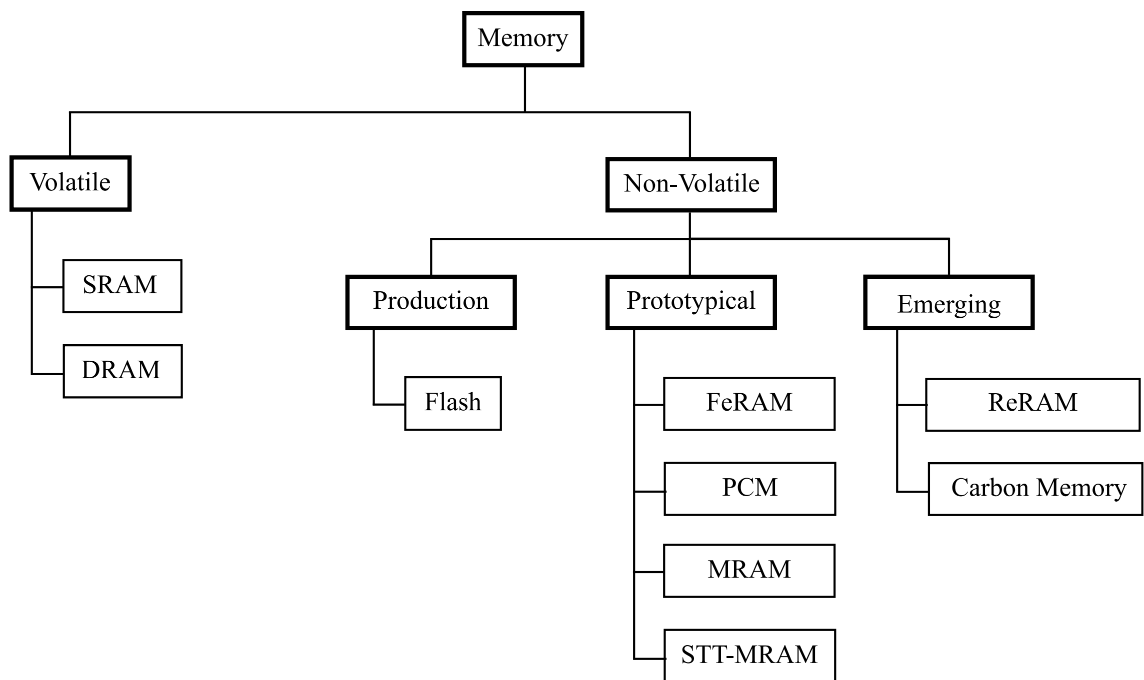


Figure 1.2: Memory taxonomy showing the most relevant memories according to the International Roadmap for Semiconductors [modified from [9, 10, 12]].

Table 1.1: Comparison of DRAM and NAND Flash and requirements of SCM [adapted from [12]]

	DRAM	NAND Flash	Memory (SCM)
Maturity	Production	Production	—
Read/Write Latency	<100 ns	100 µs Block Erase 1 ms	5 µs
Retention Time @ 85 °C	64 ms	10 yrs	10 yrs
Endurance Cycles	$>10^{16}$	10^{3}–10^{5}	10^{6}
Write Energy per Bit	100 pJ	100 pJ	100 pJ
Scalability	poor	limited (3D)	—

1.2 Traditional Memory Technologies

Dynamic Random-Access Memory (DRAM) Dynamic random-access memory (DRAM) is based on charge stored in a capacitor [3]. The access to the storage capacitor is controlled by a transistor to which the (conducting) wordline is connected. During the writing process, the transistor is in forward bias, which allows one to store charge in the capacitor (logic '1') [3, 4]. The erase process discharges the capacitor (logic '0') [3]. The read out of the state of the device is done by applying a reference voltage to the (conducting) bitline – which is orthogonal to the wordline – and sensing the voltage change of the bitline when the capacitor is accessed [3, 4]. In the case that no charge was stored on the capacitor (logic '0'), charge is drawn from the bitline, thus reducing the voltage on the bitline (and vice-versa in the case that the capacitor was charged) [3]. Since the read out is destructive, the addressed cell has to be re-written in the case that a logic '1' was stored [3]. Due to leakage current from the capacitor, cyclic re-freshing of the device state is also required [13].

Flash Flash memory is commercially available in two main categories, NOR Flash and NAND Flash [14]. NOR Flash allows one to access stored data randomly, which is in contrast to NAND Flash where data blocks are accessed sequentially. However, NOR Flash has slower writing times and storage density and is therefore commercially less relevant for large data storage applications [14]. Similar to DRAM, Flash memory is based on stored charge in a capacitor [13]. The top electrode (control gate) is connected to the word line and the bottom electrode (floating gate) is surrounded by an insulating oxide on top of a metal-oxide-semiconductor field-effect transistor (MOSFET) channel [14]. To store electrons in the floating gate, a positive bias is applied to the control gate (logic '0') which allows electrons to tunnel through the dielectric [14]. The erase process (logic '1')

requires a positive bias applied to the substrate to discharge the capacitor [14]. To read out the device state, a positive bias (smaller than used for programming) is applied to the control gate and the current response through the transistor channel is sensed [14].

1.3 Prototypical Storage Technologies

Ferroelectric Random-Access Memory (FeRAM) Memory based on ferroelectric materials (FeRAM) is based on the polarisation of the ferroelectric [15]. A typical FeRAM cell is composed of a capacitor cell, whereby the polarisation of the dielectric is altered by charging/discharging cycles of the capacitor during the write and erase procedures [15]. The device selection is carried out using a transistor [15]. The read out of the device state is done by draining the capacitor and evaluating the charge flow, which depends on the polarisation of the ferroelectric and hence, allows the determination of the stored logic state [16]. Due to the destructive nature of the read out process, it is necessary to re-write the data if the read out bit was ‘1’ [13].

Phase-Change Random-Access Memory (PRAM) Phase-change random-access memory (PRAM) is based on the phase switching of chalcogenides from an amorphous to a crystalline phase [17]. The amorphous phase has a high electrical resistance in comparison to the crystalline phase [18]. The write process that switches the device from logic ‘0’ in the high resistive amorphous state to logic ‘1’ in the low resistive crystalline state is achieved using short electrical pulses that heat the material above its crystallisation temperature but below the melting temperature [7]. The erase process is carried out by applying short electric pulses that heat the material above its melting temperature, followed by rapid cooling which re-amorphises the material [19, 20]. The highly non-linear current-voltage dependence ensures that the temperatures remain low during the read out

processes [21]. The device access is typically done using a transistor, a diode [22] or an Ovonic Threshold Switch (OTS) [23].

Despite progress in the fabrication of sublithographic PRAM structures [24], the main drawback of PRAM remains its high power consumption which is necessary to melt the material during the switching process [25].

Magnetic Random-Access Memory (MRAM) Traditional magnetic random-access memory is based on a magnetic tunnel junction (MTJ) or spin valves formed by an insulating layer that is sandwiched between two magnetic layers [16, 26]. One of the two magnetic layers is ferromagnetic and has a fixed spin orientation, while the spin orientation of the free layer can be manipulated. The magnetisation of the free layer is changed by passing sufficiently large currents through two lines ('bit' and 'digit') that are adjacent to the stack and induce a sufficiently large magnetic field to change the magnetisation of the free layer [26, 27]. This allows one to store data by using the electron spin orientation [5]. The read out is done by measuring the resistance across the MTJ stack, which depends on the orientation of the magnetic moments of the fixed layer and the free layer. A parallel orientation of the magnetic moments has a high tunnelling probability and hence, a low resistance corresponding to logic '1', while an antiparallel orientation of the magnetic moments results in a high electric resistance which corresponds to logic '0' [16].

The advantages of MRAM are fast switching, comparable to SRAM and high cyclic endurance [26]. The main challenges are related to scaling, due to the potential overlap of the induced magnetic fields that are required for the writing process, which can, aided by the low resistance contrast between the high resistive and low resistive state, lead to writing errors [13, 28].

Spin Transfer Torque Random-Access Memory (STT-MRAM) Instead of the magnetic field used in conventional MRAM, a polarised current is directly applied to the MTJ cell [29]. For writing, the control of the magnetisation of the free layer using a polarised current means that STT-MRAM is much better suited than conventional MRAM to downscaling, since 'free-space' fields are no longer required for switching [29].

To employ STT-MRAM as SCM, the main challenge is to reduce the cost per bit and to achieve a high density integration [15]. The main difficulties in these respects are the need for a transistor as device selector and the low on/off ratio (i.e. high resistance contrast between LRS and HRS) which makes MLC data storage, i.e. the storage of several bits per cell, in STT-MRAM difficult [15].

1.4 Emerging Storage Technologies

Conductive Bridging Memory (CBRAM) Conductive bridging memory (or electrochemical metallization memory [25]) belongs to the class of redox-based resistive random-access memories (ReRAMs). The characterising feature of ReRAMs is the movement of ions that combined with local structural changes lead to the formation and rupture of a conductive filament. This change in electrical resistance is non-volatile and typically reversible. In CBRAM the resistance change is based on the formation of a conductive metal filament that forms a percolation path within a solid electrolyte that separates two electrodes [13, 15]. The conductive filament starts to form in the presence of an electric field as a consequence of a redox reaction at the active metal electrode / electrolyte interface [25]. The metallic filament grows from the cathode towards the anode, due to the diffusion of mobile metal cations to the inert metal cathode, where they are reduced

[25]. The device is switched into a low resistance state (LRS) (logic '1'), when the metallic filament formed bridges the two electrodes. The device is switched back into a high resistance state (HRS) (logic '0') by reversing the polarity of the applied electric field, which dissolves the filament or at least a part of it [30]. This bipolar operation mode is in contrast to the unipolar operation mode, where SET and RESET processes are induced by voltage pulses of the same polarity (the switching process from the HRS into the LRS is called SET process, while the reversible switching process from the LRS into the HRS is referred to as the RESET process). The device state is read out using small voltages that do not affect the state of the device [30].

Due to the solid electrolyte, CBRAM has a good on/off ratio and offers good scaling capabilities [25]. However, the bipolar operation mode makes high density integration challenging. Furthermore, endurance and retention properties still show a large variability from device to device, which is partly due to the chemical potential gradients in the cell that can shift the voltages that are required to switch the cell into the LRS or HRS [25, 31].

Valence Change Memory (VCM) Another type of ReRAM is valence change memory (VCM), which is based on the formation of a conductive filament due to the movement of mobile anions in a thin oxide layer that is sandwiched between two inert electrodes [25, 32]. The filament starts to form at the cathode where the formation of oxygen vacancies leads to a valence change and a reduction of the metal cations, which then form a conductive path that grows towards the anode [30, 33]. The conductive filament is typically based on the formation of oxygen vacancies, which is in contrast to CBRAM. The device is switched into the LRS (logic '1'), when the conductive filament connects the two electrodes. Typically, the first switching into the LRS requires a forming pulse using a high voltage to establish the conductive filament. The device is RESET into the HRS

(logic ‘0’) using a reverse polarity [32]. As a consequence of the rupture of the conductive filament (and not complete dissolution) during the RESET process, the HRS has typically a lower resistance than pristine devices [34]. Recently however, forming-free devices were reported [35, 36]. The device state is read out using small voltages that do not affect the state of the device.

If one (chemically) active electrode is used, the switching mechanism changes from filamentary to interface dominated due to the redox reaction taking place at the oxide/active metal interface, and the resistance of the LRS scales with the active electrode area [32].

Thermochemical Memory (TCM) Another branch of ReRAMs are thermochemical memories (TCMs), which are based on thermally controlled diffusion and redox processes [37] and thus can be operated in a unipolar manner [25]. The unipolar operation mode sets TCM apart from VCM, which require a bipolar operation mode. Thermochemical memories typically consist of a binary oxide that is sandwiched between two inert metal electrodes [25]. During the SET pulse two conductive filaments start forming from both electrodes and the device is set into the LRS when both conductive filaments merge, creating a conductive percolation path between the two electrodes [25]. The conductive filaments consists of either an oxygen vacancy defect chain or a metallic filament due to the formation of oxygen vacancies along with a reduction of the metal cations [25, 38]. The reverse switching from the LRS into the HRS occurs then due to oxygen diffusion and local re-oxidation of the conductive filament or by the thermally induced rupture of the metallic filament [37]. A disadvantage of TCMs is the strong dependence on experimental parameters, and the inherent large variability in the device properties [32]. This, and the high energy consumption led to a drop in research activities in recent years [32].

Carbon Memory Resistive switching phenomena were also reported in different carbon allotropes, like nanotubes, thin graphitic structures and amorphous carbon (a-C) which are included under the umbrella of carbon memory [12, 39–42]. Carbon memories based on insulating, tetrahedally bonded amorphous carbon (ta-C) have recently gained traction due to their good scalability and simple deposition techniques [43]. They are based on the reversible formation of a conductive sp^2 network, in an otherwise amorphous, insulating carbon matrix [43]. The π bonds of the sp^2 bonded carbon form a delocalised or ('conjugated') network [44]. The amorphous carbon matrix is sandwiched between two electrodes. The conjugated sp^2 network forms a conductive filament within the insulating matrix, when the device is biased with a sufficiently high voltage to induce a dielectric breakdown [45]. The establishment of the conductive filament during the dielectric breakdown event switches the device into the LRS (logic '1'). The SET process leading to the formation of a conductive filament in an otherwise insulating carbon matrix was not well understood at the time when the work leading to this thesis was started. The current understanding, to which this work contributed significantly (see Sections 4.4, 4.6, 5.4 and publications [46], [47]), is that the formation of a conductive filament in a spatially confined memory cell is temperature activated and triggered by a local re-hybridisation from sp^3 to sp^2 carbon. The SET process is discussed in more detail in Section 2.5.1.

Reverse switching is induced by applying a short electric pulse which leads to the rupture of the conductive filament and resets the device into the HRS (logic '0') [43]. The RESET process that causes the reverse switching is less understood in comparison to the SET process. A large contributor to the difficulty in understanding the RESET process is the thermodynamical stability of the LRS. The current understanding, to which this work again contributed significantly (see Section 4.6 and publications [46], [47]), is that the rupture of the conductive filament is induced by the large temperature gradient that arises at the electrode / conductive filament interface during the RESET pulse. The RESET pro-

cess is discussed in more detail in Section 2.5.2. Similar to other filamentary memories, the HRS after a RESET is typically lower than the resistance of pristine devices [45].

The device state is read out using small voltages that do not affect the state of the device [43]. Carbon memories are typically distinguished from ReRAMs due the formation of a conductive sp^2 percolation path, rather than an oxygen-vacancy formation (in VCM) or metal filament (in CBRAM) [9].

1.5 Comparison of Non-Volatile Memory Technologies

The key characteristics of the most studied data storage memory technologies were introduced in Section 1.4 and are presented with their key attributes in Table 1.2. To avoid a misleading impression about the capabilities of each storage technology, typical specifications that were available from a single device of each type (rather than for devices in large arrays) were taken. The best specifications for each attribute are provided additionally in brackets [48]. The correlation between the energy consumption during the writing process as a function of the writing time and cell area of a device, are also provided in Figure 1.3 and Figure 1.4, respectively [48]. In both figures VCM and TCM are grouped together as ReRAM, meanwhile CBRAM is shown separately (cf. [32]).

Table 1.2: Specifications of single device performances for selected storage class memories SCMs. VCM and TCM are grouped together as ReRAM, meanwhile CBRAM is shown separately (cf. [32]); the best characteristics for each attribute are given in brackets [adapted from [48]].

	PRAM	STT-MRAM	CBRAM	ReRAM
Maturity	Prototypical	Prototypical	Emerging	Emerging
Film Thickness	10 nm(1) (2 nm)	≈5 nm(2) (≈2 nm)	—(3) (2 nm)	<5 nm(4)
SET Times	30 ns(1) (10 ns)	0.5 ns(2) (0.2 ns)	5 ns(3)	5 ns(4) (0.3 ns)
RESET Times	30 ns(1) (6 ns)	0.5 ns(2)	1 ns(3)	5 ns(4) (0.3 ns)
Retention Time	10^4 s @ RT(1) (10 yrs @ 220 °C)	30 $[E_b/k_bT]$(2) (120 $[E_b/(k_bT)]$)	10 yrs @ RT(3) (10 yrs @ 150 °C)	10 h @ 200 °C(4) (10 yrs @ 85 °C)
Endurance Cycles	10^5(1) (1.25×10^{12})	—(2) (10^{15})	10^7(3)	10^6(4) (10^{12})
Write Energy per Bit	<0.1 pJ(1)	6 fJ(2)	<2 pJ(3) (<1 pJ)	<1 pJ(4)

(1) Taken from [49]
(2) Taken from [50]
(3) Taken from [51]
(4) Taken from [52]

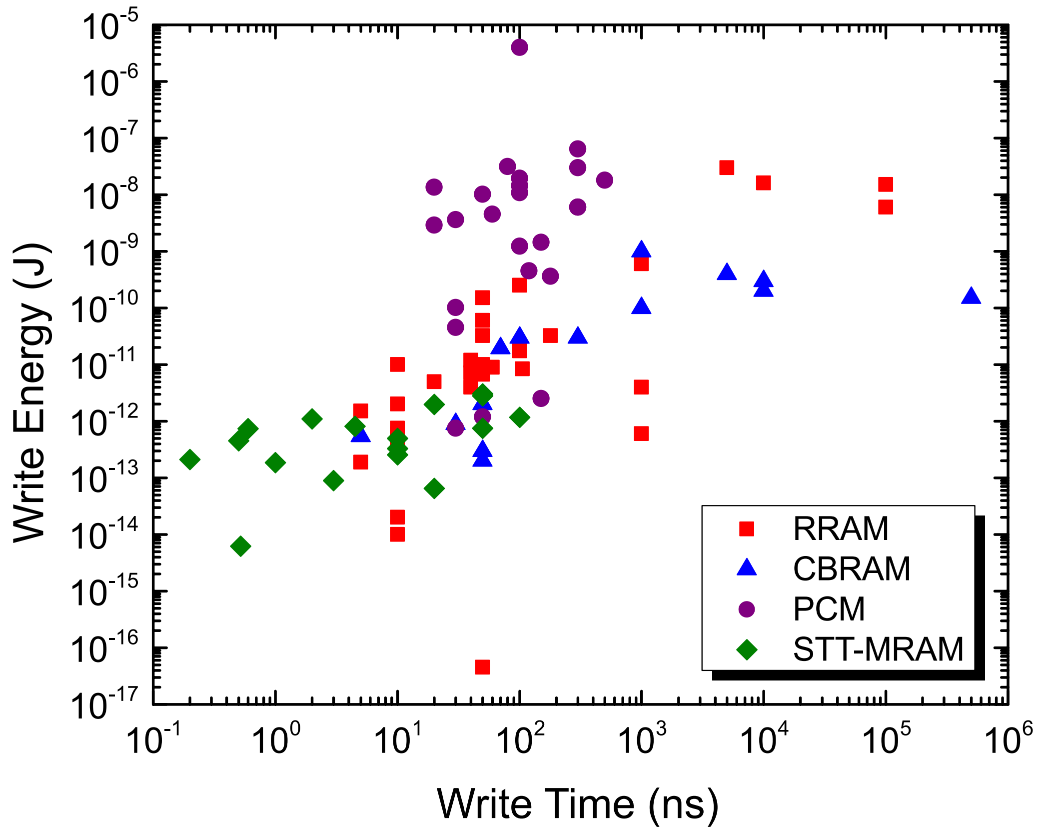


Figure 1.3: Writing energy as function of writing time for selected storage class memories (SCMs) [taken from [53]]; VCM and TCM are grouped together as ReRAMs, meanwhile CBRAM is shown separately (cf. [32]).

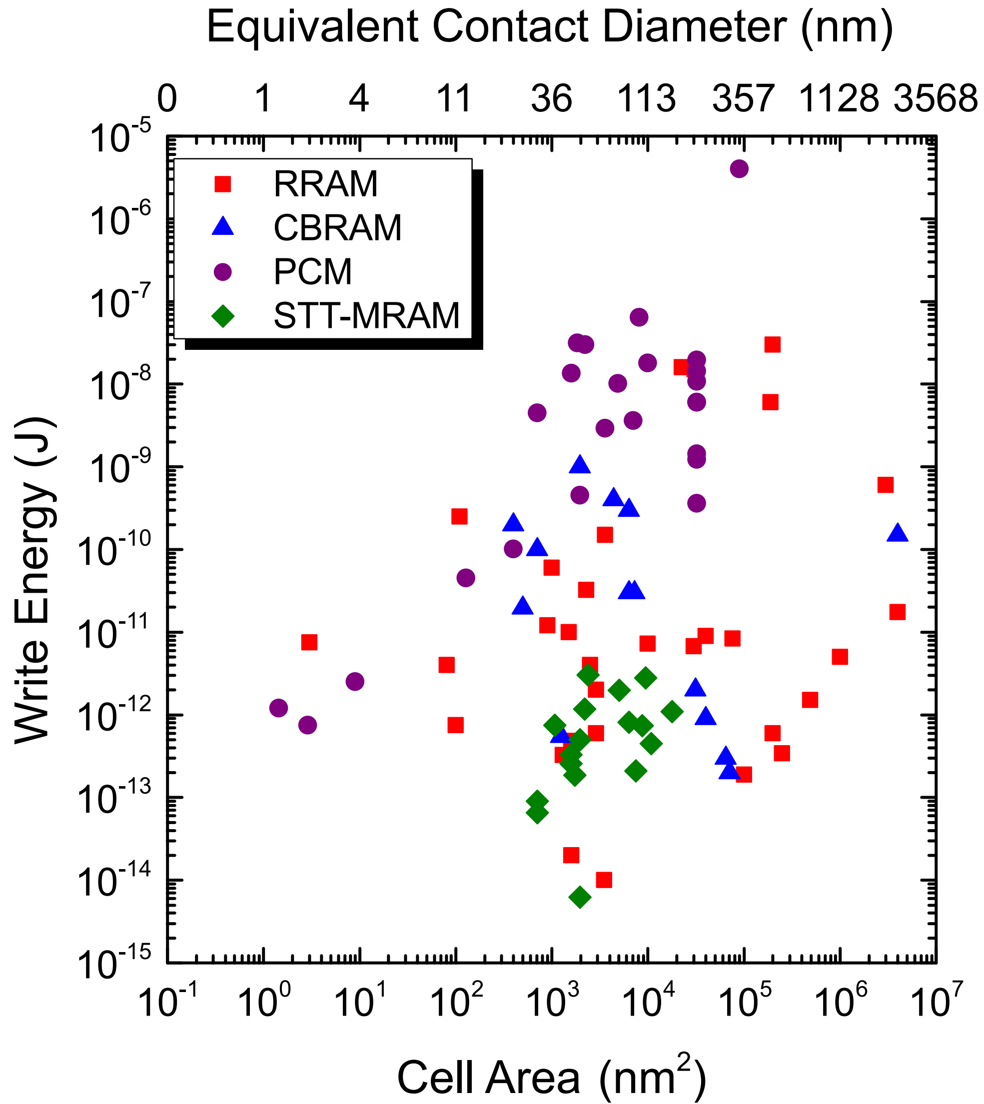


Figure 1.4: Writing energy as function of the cell area for selected storage class memories (SCMs) [taken from [53]]; VCM and TCM are grouped together as ReRAMs, meanwhile CBRAM is shown separately (cf. [32]).

1.6 Beyond von Neumann Computation

Modern computers are based on the von Neumann architecture where logic and memory operations are physically separated [19]. Logic and arithmetic operations are performed in the CPU from where the data has to be transferred to the memory and retrieved for further computation [19]. This separation between logic and memory is currently a large performance limiting factor and known as the von Neumann bottleneck [19, 54]. To overcome this performance limitation, this separation can be abandoned to perform logic/arithmetic operations and data storage within the same physical unit using a computing-in-memory or memcomputing approach [19, 55, 56]. Concepts to address this issue include the translocation of arithmetic operations from the CPU to the SCM [19, 57]. These concepts can be realised using so-called memristive devices, where the electrical resistance of the device is related to the charge flow through the devices, examples of which are non-volatile resistive switching memories (such as ReRAM, PRAM, CBRAM etc.) [58–61]. Arithmetic operations can be implemented using multiple pulses to change the resistance state gradually from the LRS into the HRS or vice-versa, as it was shown for phase-change memory devices [19, 57]. The excitation pulses are configured (in amplitude and duration) such that only after all pulses of the predetermined sequence have been applied does the resistance of the cell change significantly enough (either in transitioning from the HRS into the LRS, or vice-versa) to cross a pre-set resistance decision threshold. Thus, for base-n operation, a decision threshold is set between the resistance levels achieved after the input of (n-1) and n pulses. The number of pulses required to pass through the decision threshold determines the arithmetic base of the calculation. When the accumulator exceeds the decision threshold a carry forward is recorded and the device is set back to its starting state and the input pulses are continued until all the remaining input pulses have been sent [19, 62]. More details for carrying out accumulator-based arithmetic op-

erations (addition, subtraction, multiplication, division etc.) are provided in [19, 57, 62]. In contrast to MLC data storage, where the different resistance levels have to be precisely sensed, this arithmetic approach solely requires the distinction of two resistance states that are separated by a decision level [19].

For the remainder of this thesis the focus is on amorphous carbon-based memories, which have the potential to play an important role as non-volatile SCM as well as in beyond von Neumann computation due to their simple structure, cheap manufacturing processes, good scalability, fast switching times and biocompatibility [43, 63, 64].

1.7 Thesis Objectives

Memory devices based on ta-C have promising properties, such as nanosecond switching times, a good scalability (possibly to the single bond level), cheap and easy manufacturing processes [43]. The key performance achievements of memory devices based on ta-C are summarised in Table 2.2. Motivated by these promising characteristics, the unipolar switching and data retention capabilities of ta-C devices were investigated in Sections 4.2 and 4.3. The effect of different pulse lengths and amplitudes on the SET process was investigated in Section 4.7 to correlate the switching times with power and energy consumption. Preliminary experiments have shown a low cycling endurance (see Section 4.4), which could be linked to the thermodynamical stability of the LRS. In Section 4.6 this was found to be exacerbated by the unipolar operation mode and the fast switching times, which give rise to large capacitive currents that manifest in large conductive filaments [43]. This led to an intensive investigation into the conditions at the dielectric breakdown event, when the switching from the HRS into the LRS occurs, see

Sections 4.6, 5.1, 5.2, 5.3, 5.4. This work contributed to the current understanding of the SET process in ta-C memories, as discussed in Sections 1.4 and 2.5.1.

To address the difficulty of a low cycling endurance, memory devices based on oxygenated amorphous carbon (a-CO_x), which have shown high cycling endurance in bipolar mode due to oxygen aiding the reset process [63], were investigated in Chapter 6 with respect to data retention, switching time, multi-level storage and beyond von Neumann computation.

The motivation of this work is therefore threefold. Firstly, the switching performance of devices based on elemental amorphous carbon and oxygenated amorphous carbon were evaluated with respect to the switching time, energy consumption and temperature stability. Secondly, a computational model was developed to help shine light on the switching process, in particular on the conditions at dielectric breakdown, especially on the temperature distribution due to the Joule heating effect. Thirdly, the memristive properties of oxygenated amorphous carbon were investigated. As part of this study, a multi-level approach was realised, which allows a significant increase of the storage density. Additionally, a simple base-16 accumulator was implemented to demonstrate some of the beyond von Neumann capabilities of oxygenated amorphous carbon.

1.8 Thesis Outline

Chapter 1 The first chapter introduces the memory taxonomy and identifies the performance gap in the memory hierarchy that is located between fast, but volatile memory on one side and slow, but non-volatile memory on the other side. The working principles of current memory storage technologies are presented and compared with the most promising and emerging memory storage technologies as identified by the International

Roadmap for Semiconductors (ITRS) [9]. The concept of memcomputing to perform arithmetic operations within a memristive device is briefly introduced as means to overcome the speed limitation of the von Neumann architecture.

Chapter 2 The second chapter reviews the most common deposition techniques for amorphous carbon thin films and provides a brief description of the working principle of each. The most typical spectroscopic characterisation methods are reviewed with respect to their capability to determine the sp^2 and sp^3 content of deposited films. A key emphasis is put on Raman spectroscopy which allows one to get insights in the local arrangement of sp^2 bonded carbon, which is a key factor in determining the electric properties of amorphous carbon-based films. Further, the key concepts of electronic transport in localised states is reviewed for low electric fields, together with trap-limited band transport for high electric fields. Additionally, a literature review about the current understanding of the physical origins of the SET and RESET processes in insulating amorphous carbon is provided.

Chapter 3 The third chapter presents the deposition methods and parameters used for the ta-C and a-CO_x films and devices used in this thesis, along with the results of the material analysis of ta-C and a-CO_x films. Further, the design of the ta-C and a-CO_x memory devices is provided, together with descriptions of the experimental device test setups that were used to investigate the switching and retention properties of the ta-C and a-CO_x memory devices, and the low temperature conduction properties of the ta-C memory devices. Additionally, the material parameters and electric pulses used within the framework of the computational modelling are provided. It is pointed out that the experimental pulses to be modelled have to be long enough to avoid a time lag between the maximum voltage achieved and onset of the dielectric breakdown. This finding aids

to the understanding of the SET process since the observed time lag suggests that the electric field alone is not sufficient to switch the device from the HRS into the LRS.

Chapter 4 In chapter four, the switching performance, energy consumption and data retention capabilities of tetrahedral amorphous carbon based memories are investigated experimentally. The fastest switching times and lowest power consumptions achieved to date are reported.

Chapter 5 The fifth chapter presents the results of the experimentally determined field- and temperature dependent conductivity of pristine ta-C, which is fed into the computational modelling. The results of the simulated conductivity is then presented and compared with experimental data, which allows one to draw conclusions about the temperature distribution at the onset of dielectric breakdown. The obtained high temperatures, exceeding 1500 K, suggests that temperature activation is important to SET the device, which aids to the understanding of the SET process. The obtained insights are used in an optimisation study that aims to provide a guideline to reduce the energy consumption.

Chapter 6 The sixth chapter present the switching performance, energy consumption and data retention capabilities of devices based on oxygenated amorphous carbon. The memristive effects are evaluated for the first time, and a 3-level ($1^1/_2$ bits) data storage approach is presented. Additionally, a base-16 accumulator response is successfully achieved. The chapter concludes with a thermal analysis that aims to provide insights into the temperature distribution within a filament during the reset process.

Chapter 7 In Chapter 7, the key findings are summarised and a future outlook on research on carbon-based materials for memory applications is presented.

In terms of original contribution to knowledge, the work of this thesis achieves this via both significantly improved device performance aspects as well as contributions to the understanding of the switching mechanism in ta-C and a-CO_x devices. Notable contributions include the following:

- Fastest switching in a-CO_x memory devices reported to date (40 ns).
- Fastest switching in ta-C and a-CO_x memory reported to date (7 ns).
- Data retention of 300 s @ 450 °C achieved in ta-C memory devices.
- Lowest writing energy per bit in a-CO_x memory devices reported to date (≈2 pJ).
- First time multi-level storage achieved in a-CO_x memory devices.
- First time accumulator response (base-16) realised in a-CO_x memory devices to demonstrate beyond von Neumann capabilities.
- First complete computational modelling of experimentally obtained conductivity in ta-C memory devices ranging from Ohmic conduction until the onset of the dielectric breakdown.
- Realisation that large electric fields in the absence of high temperatures do not suffice to induce a dielectric breakdown in ta-C memory devices.
- Localised Joule heating is captured in the computational model by introducing a random distribution of conductive sp^2 clusters in an otherwise insulating sp^3-rich matrix.
- Realisation that high temperatures exceeding 1500 K are present in ta-C memory devices at the onset of the dielectric breakdown.

- Highlighting that temperature plays an important role during the RESET process in a-CO_x devices.

Chapter 2

Insulating Amorphous Carbons

2.1 Introduction

Resistive switching phenomena can be observed in various carbon allotropes, as outlined in Section 1.4. Probably the most promising allotropes with regards to ease of fabrication, scaling, fast switching speeds and the prospective application in beyond von Neumann computation, are based on amorphous carbon and amorphous carbon derivatives [63]. The different a-C derivatives such as diamond-like carbon (DLC) have a large variation in optical, electrical and mechanical properties [65]. These differences arise due to the inherent differences between graphite-like sp^2 bonding and diamond-like sp^3 bonding [65, 66]. The main attributes that affect the electrical properties and hence, influence the resistive switching performance in a memory device, are the sp^3 content, the clustering of the sp^2 phase into conjugated sp^2 rings or networks, the orientation of the sp^2 phase, the cross-sectional nanostructure and the content and bonding of any additional elements, such as hydrogen [67] (or oxygen [63]) [46, 65, 66]. Amorphous carbon with a significant fraction of sp^3 bonds is referred to as diamond-like carbon (DLC) or tetrahedral amorphous carbon (ta-C), in the case of a very high sp^3 C-C bonding content [65, 66, 68]. The relation (in terms of sp^3, sp^2 and H content) between graphitic carbon, diamond-like carbon and hydrogenated carbon is shown in the ternary phase-diagram in Figure 2.1.

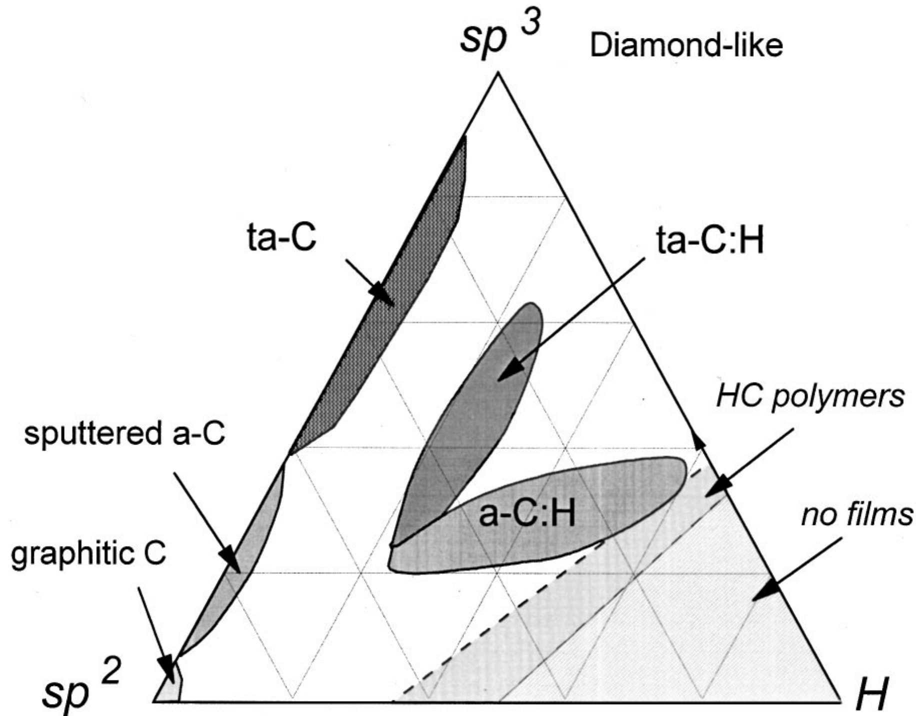


Figure 2.1: Ternary phase diagram of amorphous carbon and amorphous carbon-based alloys (*here* a-C:H) [taken from [69]].

For the use of amorphous carbon as an active material in memory devices, it is necessary to disrupt any existing conjugated (delocalised) π networks (see Section 1.4) to achieve reversible switching from the LRS into the HRS [43]. The current densities that are required for this RESET process were reported to be $\approx$350 MA cm^{-2} [43]. In amorphous carbon containing a high sp^2 content, these current densities translate into large currents that are required to disrupt the large extended conjugated sp^2 networks connecting the electrodes. This is power and energy inefficient, and in the case of conductive carbon only feasible for areal cross-sections with diameters below 10 nm [43, 45]. The reason for this is that practically the entire volume has to be amorphised. Thus, a more viable route is the use of ta-C or a-C-based alloys that reduce C=C sp^2 bonding, (such as hydrogenated amorphous carbon (a-C:H) or oxygenated amorphous carbon (a-CO_x)).

2.2 Deposition Methods

Filtered Cathodic Vacuum Arc (FCVA) The filtered cathodic vacuum arc (FCVA) method is based on the creation of a plasma, which in the case of a graphite target, contains a high ion density of C^+ species [65]. The plasma is created through an electric arc discharge between a graphite target and a small striker anode in a high vacuum environment [65, 70]. To remove large ion clusters, the plasma is guided through a curved magnetic filter before hitting the substrate [70]. To control the energy range of the impinging ions, a DC or RF bias can be applied to the substrate [65, 70]. The plasma net charge is neutral which allows the deposition of ta-C films on insulating substrates [65]. A schematic of a single bend FCVA apparatus is shown in Figure 2.2. The FCVA is the most commonly used method for producing high-quality ta-C films, and as such is used widely for e.g. ta-C coatings of magnetic hard disks [70–72]. The FCVA method was also used to prepare the ta-C films for the resistive switching investigations that are presented in this thesis.

Pulsed Laser Deposition (PLD) The pulsed laser deposition (PLD) method uses short, high energetic laser pulses which create a plasma by vaporising carbon particles from a graphite target. [65]. The plasma consists of ionised and neutral carbon species that condense on the substrate as a consequence of the plasma expansion [73]. For industrial application, the high initial costs and the requirement for homogeneous depositions on the wafer-scale, are the biggest obstacle to the widespread adaption of PLD for a-C deposition [73]. A schematic of a PLD system is shown in Figure 2.3.

Mass Selected Ion Beam (MSIB) The mass selected ion beam method (MSIB) is based on the extraction of C^{+} ions from a graphite target or a carbon containing gas [74]. To select only C^{+} species, the ion beam is accelerated to around 40 keV and guided through a 90° bent magnet for mass selection [75]. The ion beam is decelerated before reaching the substrate [75]. Although ta-C films produced with the MSIB method are of high quality, the deposition rate is too low (0.001 Å/s) for industrial applications [65, 70, 74]. A schematic of an MSIB system is shown in Figure 2.4.

DC Magnetron Sputtering The sputtering method is widely used in industry due to its capability to deposit electrically conductive as well insulating materials on a large scale [65]. Conductive materials are deposited using direct current (DC) sputtering, whereas insulating materials have to be deposited using radio frequency (RF) sputtering to avoid charge build-up [70]. Amorphous carbon thin films are usually deposited from a graphite target using the DC magnetron sputtering technique. The DC magnetron sputtering technique is based on the creation of a plasma in a noble-gas, typically argon, atmosphere [70]. The Ar^{+} ions are accelerated towards a conductive target, where typically lumps of particles are released as consequence of the Ar^{+} ions' impact on the target [70]. The particles are then deposited on the substrate. To increase the yield, magnets are placed behind the target [65]. The magnetic field increases the ion path, which leads to a higher ion density, and ultimately to a higher yield [65]. A schematic of a magnetron sputtering system is shown in Figure 2.5. Although a-C films of high quality can be produced using this method, the deposited carbonaceous species are of low energy (several eV) and consequently, the resulting film has a low sp^3 content [65, 70]. The high sp^2 content (>80 %) inhibits their use in resistive switching applications (see Section 1.4) [76]. The sp^3 content can be increased by adding a reactive gas like oxygen during the deposition process which produces a-CO_x films, whereby the ratio of sp^3 and sp^2 bonded carbon

varies as function of the oxygen partial pressure [63, 65, 70]. The deposition of carbon from a graphite target in an O_2 atmosphere was used in the work of this thesis to produce a-CO_x films for resistive switching studies.

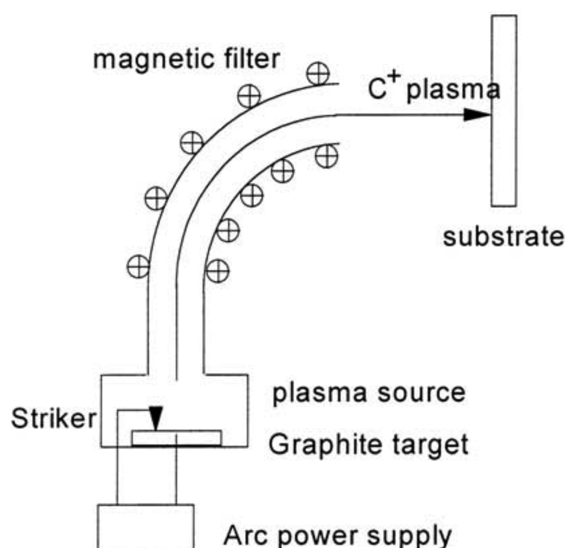


Figure 2.2: The FCVA method: Single bend filtered cathodic vacuum arc deposition technique; the plasma arc is ignited by touching the cathode (graphite target) with a striker. The high energy plasma is then filtered for neutral species using a magnetic filter, before impinging on the substrate. The net-charge is neutral which allows the deposition on insulating substrates [modified from [65].

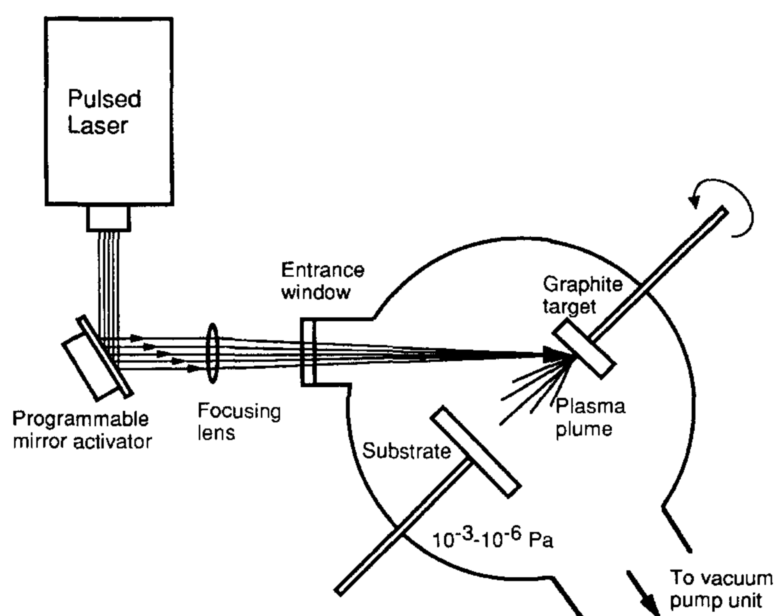


Figure 2.3: The PLD method: A laser beam is focused on a graphite target inside the vacuum deposition, which leads to the evaporation and condensation of carbonaceous species on a substrate. The energy density of the laser beam is directly correlated to the kinetic energy of carbon ions, which in turn affects the sp^3 content of the resulting carbon film [65, 73] [taken from [73]].

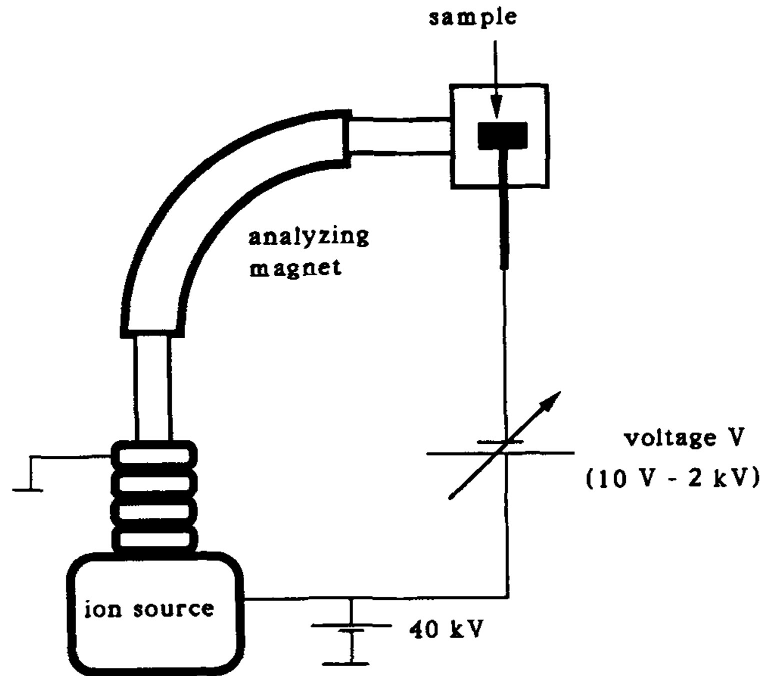


Figure 2.4: The MSIB method: The C^+ ions extracted from an ion source are accelerated up to $40\,\mathrm{keV}$ and guided through a $90°$ bend magnet for mass selection [75]. The ion energy is decreased prior to the deposition on the substrate [taken from [75].

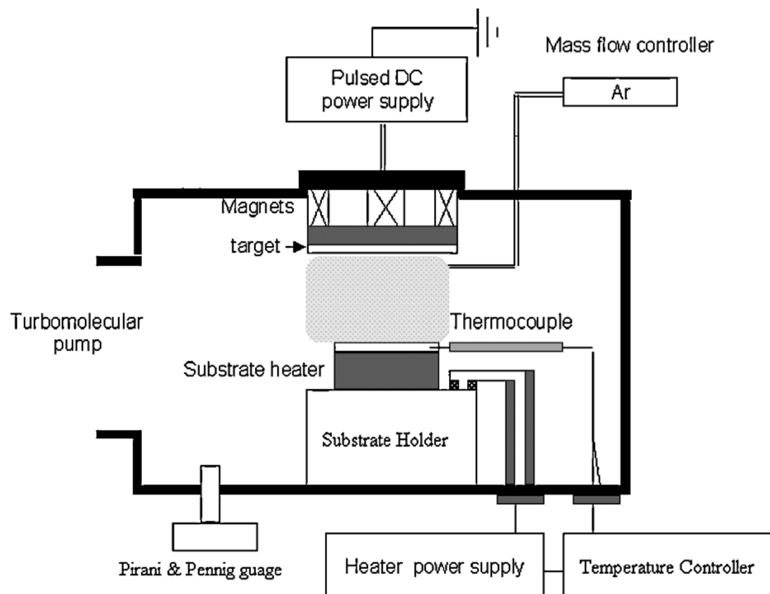


Figure 2.5: The magnetron sputtering method: Noble-gas ions (typically Ar^+) are accelerated towards a cathodic graphite target, which leads to the release of lumps of carbonaceous species from the target and deposition on a substrate [70]. Some neutralised noble-gas ions are incorporated into the deposited film [70] [modified from [77].

2.3 Spectroscopic Characterisation

It is important to characterise the structural and chemical composition of the deposited carbon-based films with respect to their use in resistive switching applications. An overview of the typical characterisation methods and their key characteristics is presented in Table 2.1. The state-of-the art methods are explained in more detailed in the following.

Raman Spectroscopy Raman spectroscopy is based on the inelastic scattering of photons in matter [78]. Raman spectroscopy is a non-destructive method to characterise the chemical and structural properties that influence the switching performance of carbon-based memories [65, 66]. The amorphisation of carbon from a crystalline graphitic form to tetrahedral amorphous carbon can be described in Raman spectroscopy by a three-stage model as originally introduced by Ferrari et al. [69]. The first stage involves the transition from graphite to nano crystalline graphite, the second from nano crystalline graphite to a-C and the last stage describes the transition from a-C to ta-C and the inherent increase of the sp^3 content [69]. The three-stage model is visualised in Figure 2.6.

The Raman spectra of amorphous carbons are dominated by sp^2 bonded carbon atoms due to the larger scattering cross-section in comparison to sp^3 bonded carbon atoms [65]. The difference of the cross-section is related to the larger polarisability of π bonds, and

Table 2.1: Characterisation methods for amorphous carbon-based films [adapted from [65]].

Method	Remarks
ESCA (XPS)	Small shifts for homopolar bonding
Raman	Multi-wavelength (including uv) analysis
EELS	Time-consuming, destructive

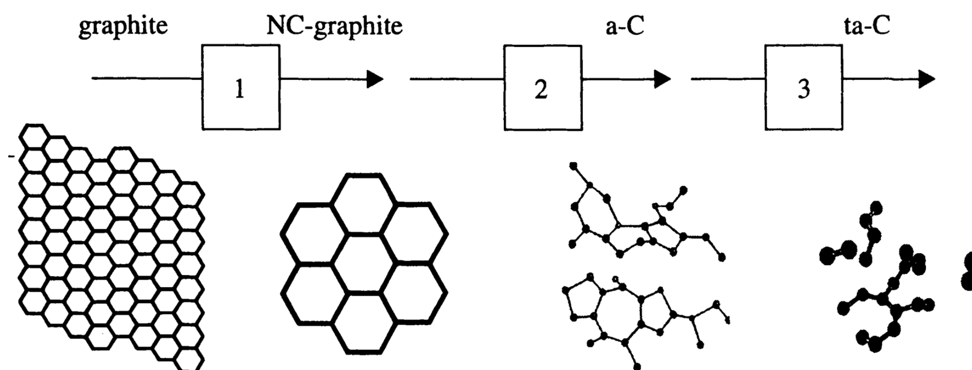


Figure 2.6: Variation of the sp^2 configuration as function of the amorphisation trajectory according to the 3-stage amorphisation model [66] [taken from [66]].

the lower energetic position of π states [65, 69]. To characterise the structural properties the intensity and position of the Raman G and D peaks are relevant for all three-stages in the transition from graphite to ta-C [69]. The G peak originates from bond stretching of sp^2 coordinated pairs [69]. The D peak is a breathing mode for benzene rings (sp^2 bonded carbon) and is only active within defective 6-fold rings [69].

The transition from graphite to nano crystalline graphite in stage one leads to a shift in the G peak position from 1581 cm^{-1} to 1600 cm^{-1} due to phonon confinement [65, 69]. The D peak also appears and consequently, the ratio of the intensities of the D and G peaks ($I(D)/I(G)$) increases [65, 69]. Stage two involves a weakening of the sp^2-sp^2 bonds due to the rearrangement of sp^2 bonded atoms from sixfold rings into odd membered rings, which leads to a decrease in the G peak position from 1600 cm^{-1} to 1510 cm^{-1} and at the same time the $I(D)/I(G)$ ratio approaches zero [69]. Stage three involves the transition from sp^2-rich a-C to sp^3-rich ta-C [69]. This transition causes an upward shift in the G peak position from 1510 cm^{-1} to 1570 cm^{-1} [69]. The origin of this G peak position shift is caused by two counteracting effects, namely the rearrangement of the sp^2 bonded atoms into olefinic chains leads to shorter bonds and thus higher vibrational frequencies, and the mixing of sp^2 vibrational modes with sp^3 vibrational modes, which are at lower frequency

[65, 69]. A Raman spectrum of the amorphisation trajectory is shown in Figure 2.7 for a 514 nm illumination wavelength [69]. Thus, the combined study of the G peak position shift and the change of the $I(D)/I(G)$ ratio can be used to determine the sp^3 content, in the absence of thermal annealing effects [69].

Upon annealing or deposition at elevated temperatures, a clustering process sets in which causes the sp^2 sites to form aromatic, sixfold rings [69]. The clustering process causes the appearance of the D peak and leads to a shift in the G position, when using a laser with a wavelength in the visible range [69]. This upward shift in the G position is a direct consequence of the larger cross-section of aromatic rings in comparison to chains [79]. The second effect of annealing is the conversion from sp^3 bonded carbon to sp^2 bonded carbon. The larger cross-section of clusters outweighs the influence of the conversion on the shift in the G peak position [69]. As a consequence, there is no unique relationship anymore between G peak position, $I(D)/I(G)$ peak ratio and the sp^3 content for visible wavelength Raman spectra [69]. This leads to a hysteresis between the G peak position and the $I(D)/I(G)$ peak ratio as a function of the sp^3 content, which prevents an accurate and unambiguous determination of the sp^3 content using solely visible Raman spectroscopy [69]. It has to be noted that while the variation of the G peak full width half maximum shows a unique relation with the sp^3 content even for one (visible) wavelength, it is advisable to perform further measurements in order to minimise experimental uncertainties [66]. The hysteresis is schematically shown in Figure 2.8.

However, to determine the sp^3 content it possible to use the fact that the G peak position is dispersive, i.e. wavelength dependent, in amorphous carbon [69, 80]. The an upward shift in the G position with increasing wavelength is caused by the stronger weighting of olefinic bonded sp^2 groups, which have a higher vibrational frequency [65, 69]. This causes the G peak position to be shifted to higher wavenumbers than the G peak position

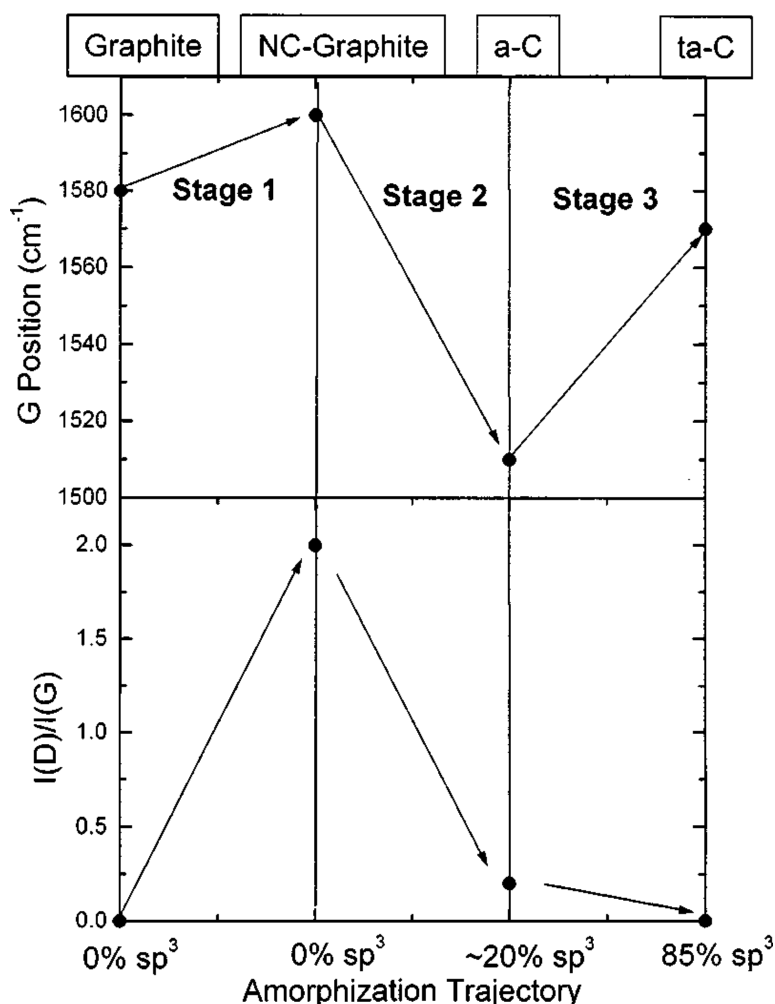


Figure 2.7: Raman spectrum of the G peak position and the $I(D)/I(G)$ peak ratio as a function of the amorphisation trajectory for a 514 nm laser wavelength [69] [adapted from [69]].

of graphite and leads to an inversion in the G peak position between ultra-violet (UV) Raman spectra and visible Raman spectra [79]. Upon annealing, the G position (under UV illumination) is shifted downwards to the G peak position of graphite due to clustering of the sp^2 bonded carbons, which is in contrast to the upwards peak shift in visible Raman [79]. It is this inversion that allows the determination of the sp^3 content unambiguously, as shown in Figure 2.9. Hence, the G peak dispersion, i.e. the rate of change of the G peak position as function of the illumination wavelength, allows the evaluation of important structural parameters such as the sp^3 content [66]. Multi-wavelength Raman spectroscopy

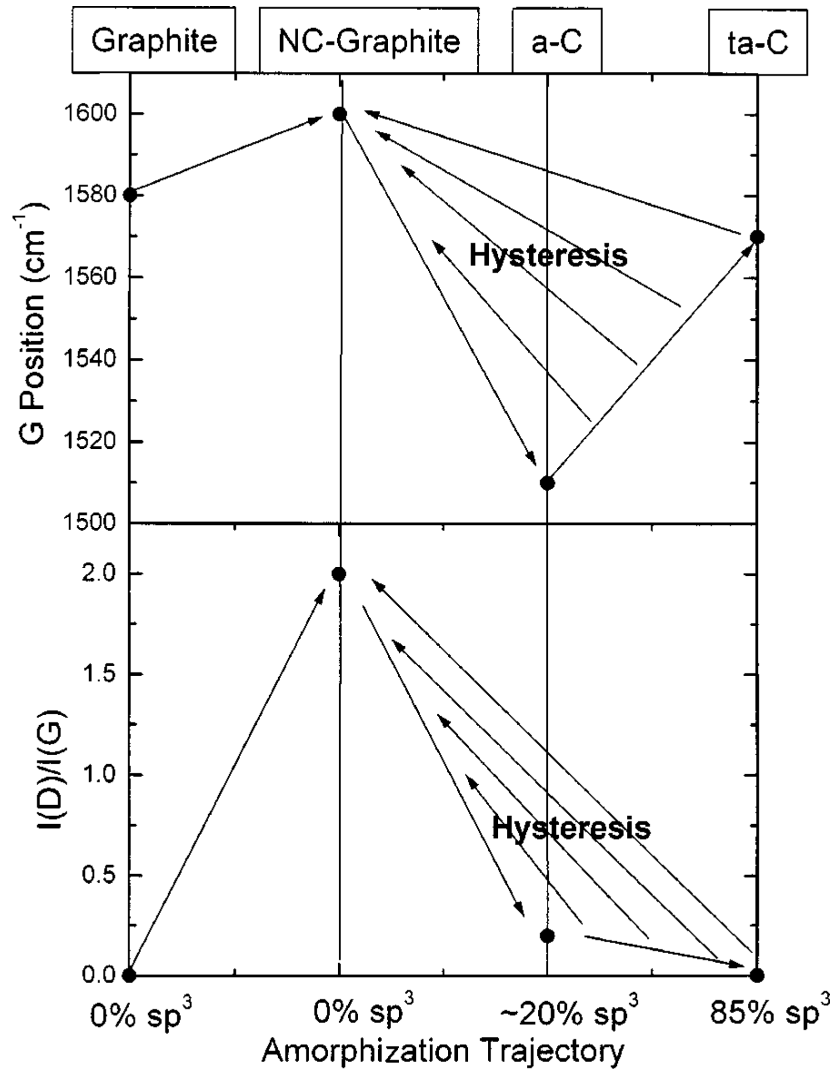


Figure 2.8: Hysteresis of the G peak position and the $I(D)/I(G)$ peak ratio due to cluster formation of sp^2 bonded carbon [69] [taken from [69]].

(UV and visible) was used extensively to characterise ta-C films used in the work of this thesis.

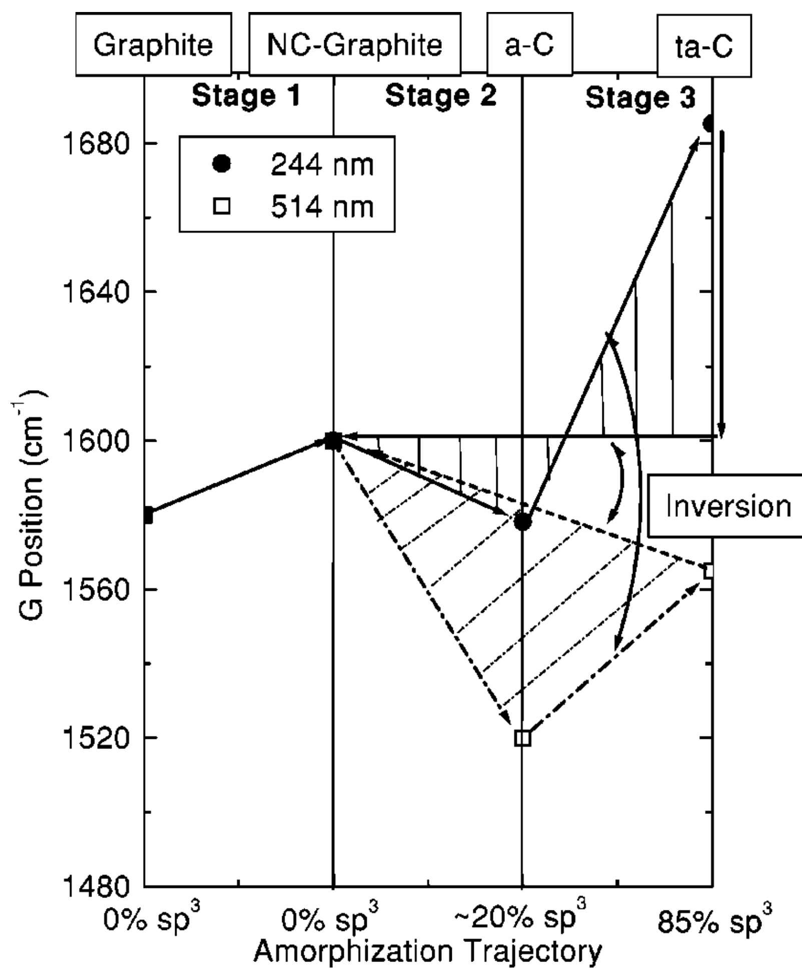


Figure 2.9: The stronger weighting of olefinic bonded sp^2 groups in UV-Raman spectroscopy leads to an inversion in the G peak position and $I(D)/I(G)$ peak ratio in comparison to visible Raman spectroscopy [79] [taken from [79]].

X-ray Photoelectron Spectroscopy (XPS) Another popular method to determine the sp^3 content is X-ray photoelectron spectroscopy (XPS), also known as electron spectroscopy for chemical analysis (ESCA) [65]. X-ray photoelectron spectroscopy is based on the interaction between X-rays and the core electrons of the material under study and is typically performed in ultra-high vacuum (UHV) [81]. The material is irradiated with X-rays of a well defined energy $h\nu$ that is above the ionisation threshold of the material [82]. The energy of the X-ray photon is completely transferred to a core electron, whereby the specific binding energy E_b of the electron is significantly lower than $h\nu$, which causes the electron (photoelectron) to overcome the work function and to potentially leave the surface of the solid [81]. The binding energy is not only element specific, but also depends on the chemical environment [81, 82]. The emitted photoelectron is then detected, and its kinetic energy E_k analysed by a spectrometer, which allows the obtaining of information about E_b and hence, about the chemical environment [81]. The relation between E_b and E_k is given in equation 2.1, where ϕ_a is the work function of the material [81]. A conventional XPS set-up is schematically shown in Figure 2.10.

$$E_b = h\nu - E_k - \phi_a \tag{2.1}$$

The analysis of the binding energy of the $1s$ core electron of carbon allows the determination of the bonding type, and hence, the sp^3/sp^2 ratio [82, 83]. The binding energy of the $1s$ core electron depends on the hybridisation of the C atoms, whereby the binding energy for sp^3 hybridised carbon is $\approx 0.9\,\text{eV}$ higher than the binding energy of sp^2 hybridised carbon [82].

The advantage of XPS in comparison to visible Raman spectroscopy is that the ionisation cross-sections are independent of the chemical state (bonding) and therefore, the sp^2/sp^3

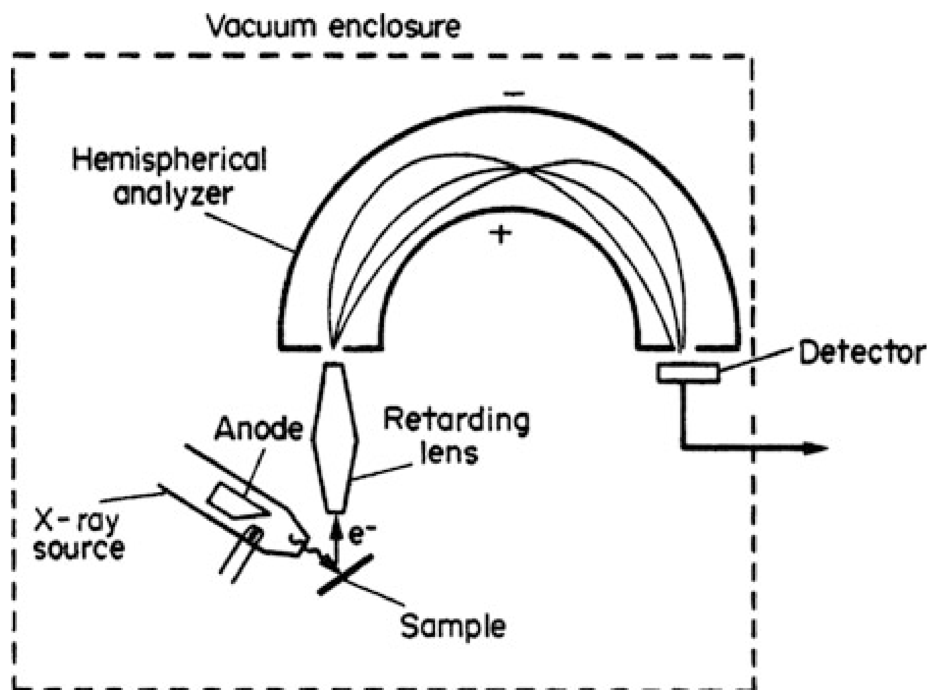


Figure 2.10: XPS set-up: The energy of X-ray photons to core electrons leads to the emission of the latter. The core electrons are then energetically filtered through the hemispherical analyser prior to arriving at the detector. The kinetic energy of the arriving photo electron allows to draw conclusions about the hybridisation specific binding energy of the photo electron [taken from [81]].

ratio can be determined by comparing their relative peak intensities [82]. The performance of single elemental amorphous carbon in resistive switching memories, however, is largely dependent on the organisation of sp^2 bonded carbon into clusters of sixfold rings. This favours multi-wavelength Raman spectroscopy over XPS as a tool to characterise ta-C thin films. However, XPS can be successfully employed to characterise amorphous carbon alloys like a-C:H and a-CO_x for resistive switching purposes, where — depending on the composition — no or little C-C sp^2 bonds are present [63, 69]. XPS spectroscopy was used to determine the composition and the sp^3 content of the a-CO_x films used in the work of this thesis (see [63]). Exemplar XPS results are given in Figure B.3 of Appendix B.4 and were obtained by collaborators at IBM Research Zurich. For further details regarding the XPS analysis of the a-CO_x thin films see [63].

Electron Energy Loss Spectroscopy (EELS) Electron energy loss spectroscopy (EELS) allows the reliable determination of the sp^2/sp^3 ratio by evaluating the energy loss of electrons that undergo inelastic scattering when transmitted through a thin film of the order of 10 nm to 20 nm (to avoid multiple scattering) [65, 70, 84]. The $2p$ orbitals in ta-C are degenerated into delocalised and localised bonding bands (π and σ), and into anti-bonding bands (π^* and σ^*) [70]. The Fermi level (E_f) in ta-C is pinned between the filled π and the empty π^* states [70]. The π and π^* bands are absent in purely sp^3 bonded carbon [70]. The sp^2/sp^3 ratio can then be determined by evaluating the energy loss of electrons that excite $1s$ core electrons in the ta-C film into either the π^* or σ^* band [70]. The π and π^* excitation is around 5 eV lower than the $1s$ to σ^* excitation [70]. Assuming sp bonding is negligible, the sp^2 content is then evaluated by comparing the ratio of the peak area A_{π^*} corresponding to the $1s$ to π^* excitations divided by the total excitation peak area $A_{\pi^*} + A_{\sigma^*}$, with the peak area ratio of 100 % sp^2 bonded carbon (like graphite) [70]. This relation is given by equation 2.2, where G_{π^*} and G_{σ^*} are the peak areas for the $1s$ to π^* excitation and the $1s$ to σ^* excitation in graphite [70]. An indirect estimate of the sp^3 content can be obtained by evaluating the position of the plasmon energy peak at the low-energy end of an EELS spectrum [85]. The EELS analysis was used to characterise the sp^2/sp^3 ratio in ta-C films used in the work of this thesis. The results of the EELS characterisation are presented in Sections 3.1.2 and 4.6.

$$sp^2\,[\%] = \frac{A_{\pi^*}}{A_{\pi^*} + A_{\sigma^*}} \cdot \frac{G_{\pi^*} + G_{\sigma^*}}{G_{\pi^*}} \cdot 100\% \tag{2.2}$$

2.4 Electronic Transport

The difference in conductivity between the HRS and LRS in amorphous carbon arises due to changes in the density of states (DOS). The main difference in conductivity arises from

the transition from localised π states in the vicinity of E_f in ta-C, into ordered clusters [68].

2.4.1 Density of States

A feature of the DOS in disordered materials is the presence of defect states within the band gap, which separates the valence band and the conduction band [65]. The defect states closer to the band edges originate from distortions in bond lengths and angles [65]. Deep defects originating from a different bonding configuration are typically located in the middle of the band gap [65, 86].

The extended, i.e. delocalised, states (valence and conduction band) in ta-C are comprised by σ and σ^* states, whereas the deep defects arise from π and π^* states of sp^2 bonded carbon within the sp^3-rich matrix [65]. The Fermi level in ta-C is pinned between the π and π^* states and the low conductivity of as-deposited ta-C originates[5] from the localisation of the charge carriers in the π and π^* states as schematically shown in Figure 2.11 [65].

The change from localised to delocalised (extended) states occurs at the mobility edge (E_m) [86]. In the case of isotropic orbital interactions (s and σ states), E_m can be related to the DOS via the insulator-metal transition as first described by Mott [86, 87].

The insulator-metal transition describes the transition of an electrically insulating material to an electrically conducting material once the DOS is high enough [86, 87]. The insulator-metal transition can be described by equation 2.3. This equation is an approximation which states that once the DOS at the mobility edge ($N(E_m)$) is high enough

[5] ta-C has to be deposited at temperatures low enough to avoid cluster formation [69].

(the cubic root of the DOS equals a constant c divided by the Bohr radius (a_0)), then the material becomes conductive (i.e. insulator-metal transition) [86, 88, 89].

$$\sqrt[3]{N(E_m)} = \frac{c}{a_0} \tag{2.3}$$

However, it is important to note that this approximation of metal-insulator transition does not apply for ta-C, where the interaction of π-π states depends on their projected dihedral angle ϕ [65]. This leads to the strong localisation of π states that is observed in ta-C [65]. The DOS for ta-C is schematically shown in Figure 2.11 together with the dihedral angle ϕ. This is important as it explains why as-deposited a-C is insulating even at high sp^2 contents [90]. A measure for the π states localisation is the inverse participation ratio P which describes the localisation of a state and varies between 1 for strong localisation and $1/N$ for delocalisation over N sites [65, 90]. The DOS and the inverse participation ratio are shown in Figure 2.12 for sp^3 concentration of 20 %, 80 % and 92 % [90]. The calculations were performed using atomistic modelling [90].

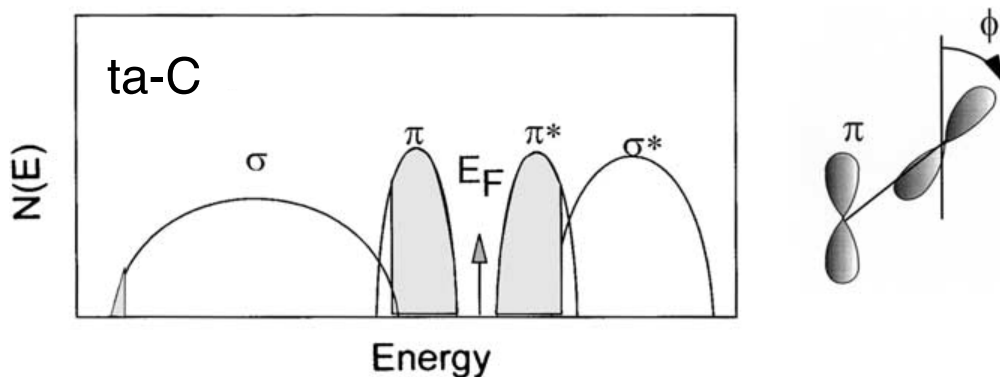


Figure 2.11: The dependence of the delocalisation of π states on the dihedral angle ϕ leads to a strong localisation of π states within the band gap [65] [modified from [65]].

The localisation of π states can be observed (see Figure 2.12) even for an 80/20 sp^2/sp^3 ratio [90]. This exceeds the percolation limit and explains why resistive switching can be observed in amorphous carbon films that contain a high sp^2 content [64, 90]. Also, this makes clear that an effective media approach [91], which would aim to link the electrical conductivity to the sp^2 content in an otherwise insulating sp^3 matrix, is not suitable to capture the conductivity change during the switching from the HRS into the LRS. The attempts — part of which were made in collaboration with the work of this thesis — to obtain insights into the HRS to LRS transition are presented in Section 2.5. These insights, were also taken into account in the computational model developed in the work of this thesis. The computational model allows the investigation of the temperature distribution at the onset of the dielectric breakdown, where the switching process from the HRS into the LRS sets in, and is presented in Sections 3.2 and 5.

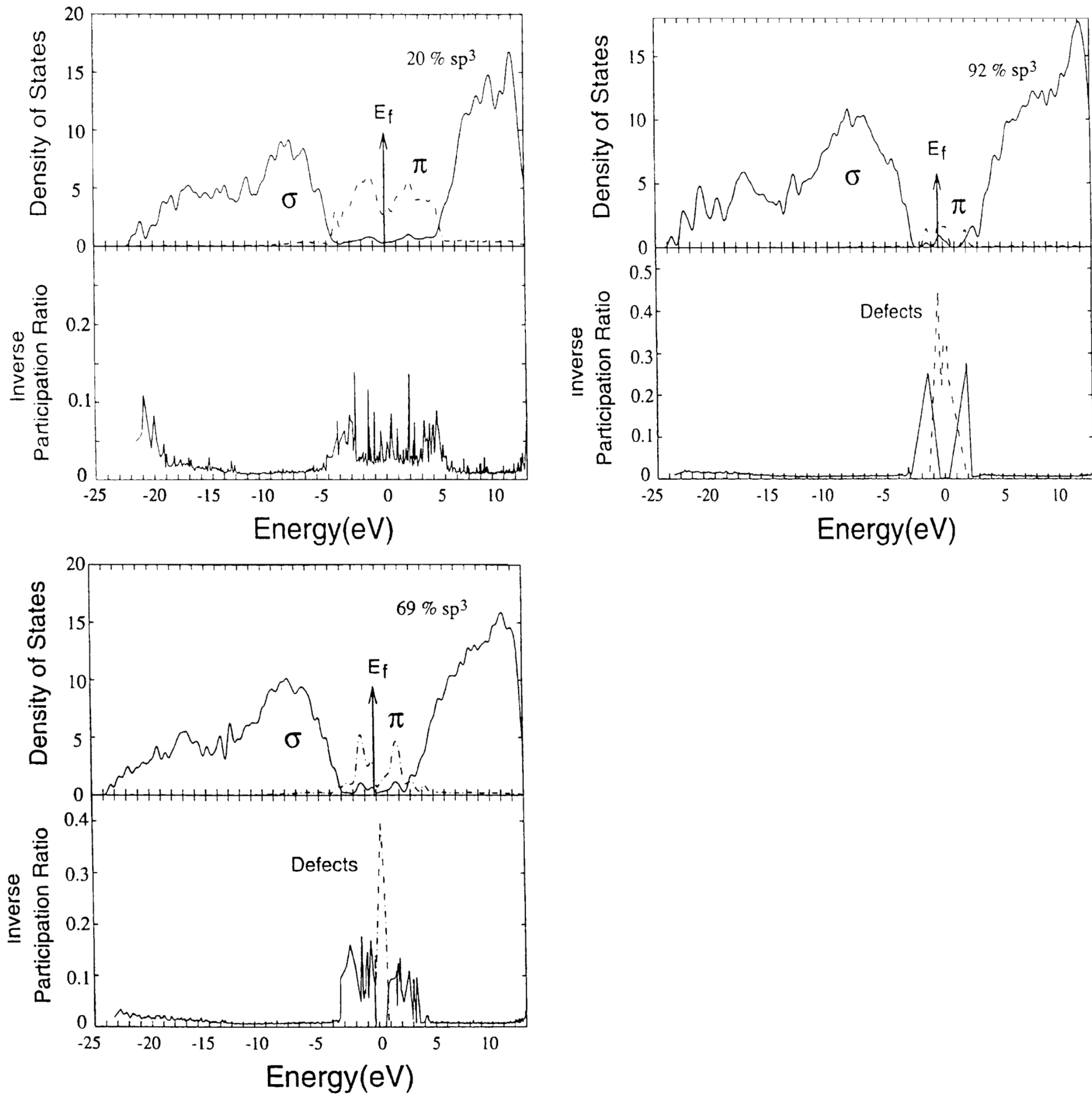


Figure 2.12: The density of states and the participation ratio are shown as a function of the sp^3 content [65] [taken from [65]].

2.4.2 Low Electric Field Transport

At low electric fields, electronic transport in amorphous carbon is reported to be governed by variable-range hopping (VRH) in localised states within the mobility gap [92–95].

Variable-range hopping describes the quantum mechanical tunnelling from occupied localised states into nearby unoccupied localised states of similar energies [86, 96, 97]. The conductivity scales inversely with the mean tunnelling distance, which in turn depends on the DOS close to E_f [86, 98, 99]. The VRH conductivity is significant in ta-C due to the high defect density ($\approx 10^{20}\,\mathrm{cm}^{-3}$) in the vicinity of E_f, which is a consequence of the strong localisation of π and π^* states within the band gap [65]. The hopping conductivity is temperature dependent since the hopping probability from occupied states into unoccupied states requires thermal activation if the final state is at higher energies than the initial jumping site [86, 96, 100]. The hopping conductivity can be described by a power law as depicted in equation 2.4, whereby σ_0 is constant at low electrical fields and the exponent, T_n is a constant and n is typically smaller than unity [44].

$$\sigma = \sigma_0 \cdot \exp\left(-\frac{T_n}{T}\right)^n \tag{2.4}$$

The VRH process is schematically visualised in Figure 2.13, where it is also contrasted with trap-limited band transport (TLB) which describes the conductivity through release and capture events of charge carriers into extended states and becomes relevant at high electrical fields [95].

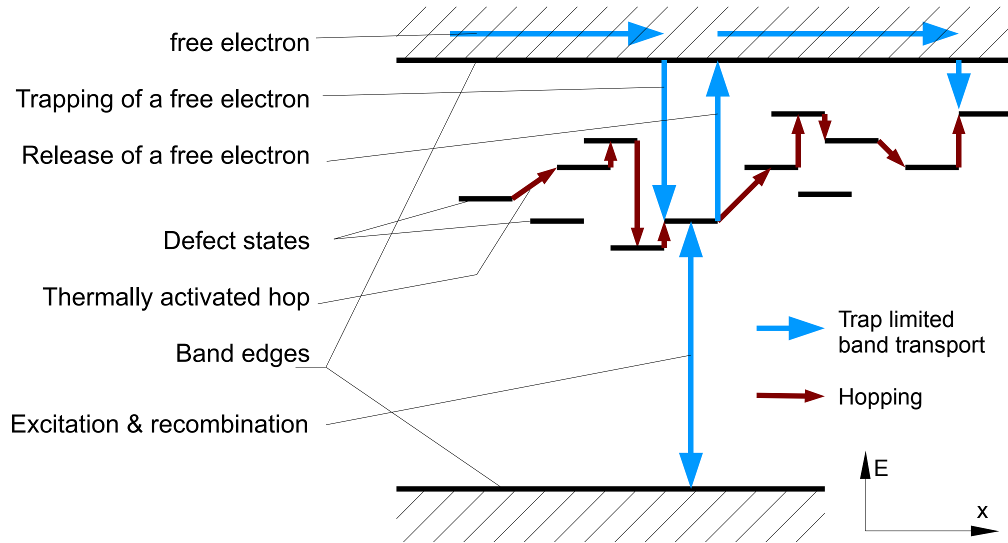


Figure 2.13: Illustration of the variable-range hopping (VRH) and trap-limited band transport (TLB) processes [adapted from [101]].

2.4.3 Field Enhanced Transport

The conductivity of ta-C shows a field-dependent conductivity at high electric fields and can be described by equation 2.5 in the case of bulk limited conduction, whereby F is the field, F_n is a constant and the exponent n depends on the conduction mechanism [95].

$$\sigma = \sigma_0 \cdot \exp\left(\frac{F}{F_n}\right)^n \tag{2.5}$$

Variable-range hopping can be distinguished from TLB at high electric fields by different values for the exponent n [95]. For field-assisted variable-range hopping $n \leq 1/2$ at high electrical fields, whereas $n \geq 1/2$ in the case of Poole-Frenkel emission [95, 102]. For the ta-C devices investigated in the work of this thesis an exponent of $n = 1$ was determined at high electric fields (see Section 5.2).

Poole-Frenkel Effect The Poole-Frenkel (PF) effect describes the thermal emission and capture events of trapped charge carriers into extended states [103, 104]. The PF effect is based on the formation of a Coulomb potential by charged empty defects [103–105]. In the presence of an electric field, the Coulomb interaction between the charged empty traps leads to a lowering of the energy barrier between them [103]. The original PF equation describes a field-lowering of the energy barrier of $\log \sigma \sim F^{1/2}$ as denoted in equation 2.6, with the constant σ_0^{PF}, the temperature T, the Boltzmann constant k_B and $\beta = \sqrt{e^3/(\pi\epsilon\epsilon_0)}$. The constant β depends on the elementary charge e, the vacuum permittivity ϵ_0 and the high-frequency dielectric constant ϵ [95, 103].

$$\sigma_{PF}(F) = \sigma_0^{PF} \cdot \exp\left(\frac{\beta F^{1/2}}{k_B T}\right) \tag{2.6}$$

In the case of a high defect density, the Coulombic potentials can interact [104, 106]. This field-dependence can be described using a two-centre Coulomb potential with a field-lowering of the energy barrier of $\log \sigma_P \sim F$ (Poole law) as denoted in equation 2.7, with s being the conductivity-dominating spatial distance between Coulomb centres [21].

$$\sigma_P(F) = \sigma_0^P \cdot \exp\left(\frac{eFs}{2k_B T}\right) \tag{2.7}$$

The barrier lowering described in equations 2.6 and 2.7 takes only the lowering in the field direction into account, which leads to an overestimation of the barrier lowering [95, 104, 107, 108]. The barrier lowering for the corrected angular dependence of the potential is thus described by equation 2.8 for the Poole law and in equation 2.9 for the Poole-Frenkel law [20, 21]. The additional parameters are the mobility μ, a constant K and the activation energy for conduction E_a [20, 21]. In the case where the electric field F is large enough ($F \gg \beta^2/(es)^2$) that there is no significant overlap of the two Coulombic centres, a transition from the Poole to the Poole-Frenkel law is observed [21, 109]. The barrier

lowering is schematically shown in Figure 2.14 for the case of a two-centre Coulomb potential in the direction of the electric field $\theta = \pi$ and $\theta = 0$ [109].

$$\sigma_{P'}(F) \simeq \frac{2K\mu k_B T}{Fs} \exp\left(-\frac{E_a}{k_B T}\right) \sinh\left(\frac{eFs}{2k_B T}\right) \tag{2.8}$$

$$\sigma_{PF'}(F) \simeq K\mu e \frac{k_B T}{\beta F^{1/2}} \left(1 - \frac{k_B T}{\beta F^{1/2}}\right) \exp\left(-\frac{E_a}{k_B T}\right) \exp\left(\frac{\beta F^{1/2} - \beta^2/(es)}{k_B T}\right) \tag{2.9}$$

Therefore, the application of either the Poole or Poole-Frenkel law depends on the strength of the applied electric field and the defect density. In in the work of this thesis, a Poole-type conduction behaviour was identified for the field-dependent conduction of ta-C (see Section 5.2). This is in agreement with reports of a high defect density in ta-C [65]. Therefore, a Poole-type conduction was used in the computational model to describe the field-dependent part of the conductivity of the ta-C devices (see Section 5.2). Since the primary aim of the computational model developed in the work of this thesis was to reproduce the experimentally determined conductivity prior to dielectric breakdown, and s, μ and E_a are unknown, a simplified model was used in Section 5.2 to capture the $\sigma \sim \sinh(F/F_0)$ dependence (see equation 5.2). In the case of a small electric field, equation 2.8 describes constant (Ohmic) conductivity [21].

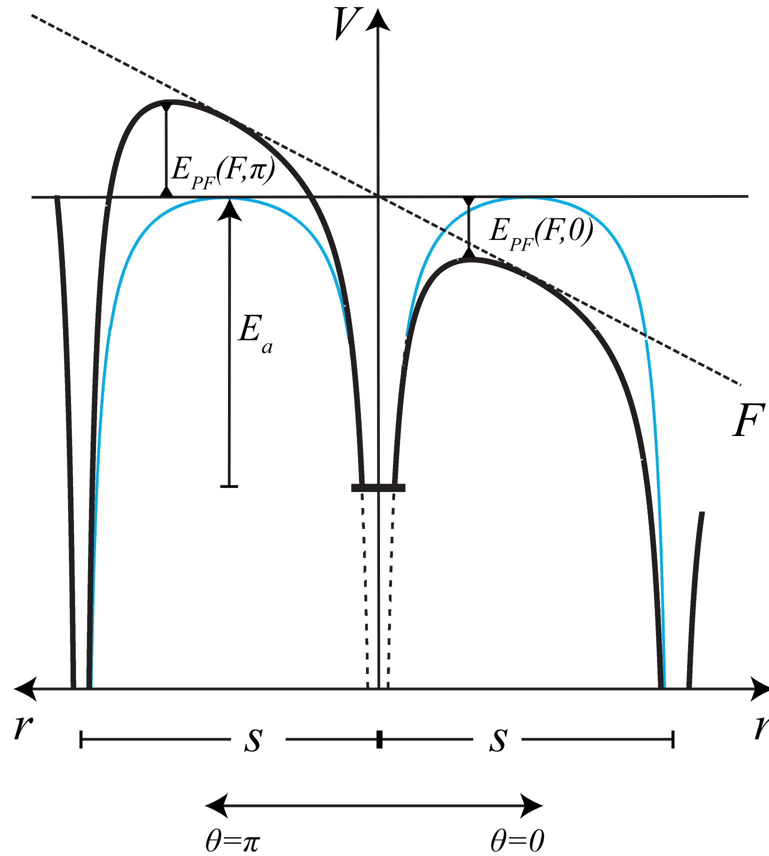


Figure 2.14: The Poole-Frenkel effect leads to a lowering of the activation energy E_a by E_{PF} due to the presence of an electric field F in direction $\theta = 0$ [109]. The dominating spatial distance between Coulomb centres is denoted as s [109] [taken from [109]].

2.5 Resistive Switching Mechanism

The physical mechanisms causing the switching process in amorphous carbon from the HRS into the LRS and the reverse switching process from the LRS into the HRS are still under debate [46, 110–112]. The following subsections provide an overview about the suggested mechanisms that lead to the formation (SET process) and rupture (RESET process) of a conductive filament in elemental amorphous carbon-based memories. The key difference between memories based on ta-C and alloyed amorphous carbon is that an additional element, like oxygen, aids the RESET process in the bipolar operation mode

[63]. Both types of memories are based on the formation and rupture of an sp^2-rich carbon filament [63]. However, the addition of oxygen was found to increase the cyclic endurance due to oxygen aiding the RESET process by reacting with the conductive filament [63]. It was found in the work of this thesis that oxygen assists the RESET process, even in the absence of large, aiding electric fields. The results of this investigation are presented in Section 6.2. This sets devices based on a-CO_x apart from devices based on elemental amorphous carbon [63]. Devices based on elemental amorphous carbon solely rely on a RESET process induced by Joule heating effects [63]. Note that the following discussion is limited to elemental amorphous carbon, but also relates to memories based on alloyed amorphous carbon when operated in a unipolar manner [63].

2.5.1 SET Process

The means to obtain information about the SET process in amorphous carbon include experiments, circuit simulations, finite element simulations and atomistic simulations. The main challenge to obtain insights into the switching process directly from electrical switching experiments arises from the fast switching speed (≈1 ns), which is usually accompanied and overshadowed by a parasitic capacitive discharge, along with the extremely small size (nanometres) of the switched regions [43].

An entirely field dependent switching mechanism in the absence of high temperatures was conjectured in [113] using a simulation based on a random circuit breaker model. However, no detailed switching mechanism was proposed. On the other hand, annealing [114] and pulsed laser experiments [64] on pristine amorphous carbon films indicate that a substantial reduction of the resistivity can be achieved thermally.

Two possible scenarios for the formation of a conductive graphitic filament in an sp^3-rich

matrix comprise the formation of sp^2 clusters through the re-arrangement of sp^2 sites and direct conversion of carbon atoms from sp^3 hybridisation to sp^2 hybridisation [113]. Electrothermal switching experiments and pulsed laser experiments (1 µs to 100 µs pulse lengths) and subsequent analysis of the sp^3 content revealed the formation of graphitic clusters, while the sp^3/sp^2 ratio remained constant, suggesting that the SET process is driven by the re-arrangement of sp^2 sites [64].

This view is in agreement with reports that assign the direct conversion process a significantly higher activation energy in comparison to clustering (3.5 ± 0.9 eV [115] and ≈3.3 eV [72] vs. ≈0.28 eV [72]).

The time scale of both processes (clustering and conversion) were evaluated in a study using a quantum molecular dynamic simulation approach [110]. The study found that at a temperature of 2000 K the direct conversion process takes a few hundred femtoseconds and the clustering of sp^2 sites requires tens of picoseconds, indicating that both processes can occur fast enough, at least at 2000 K, to explain nanosecond switching [110, 111].

Another molecular dynamic (MD) simulation study [46] deployed a device sized simulation box and a constant volume approach to replicate the experiments that where undertaken in the work of this thesis. In this device design, the amorphous carbon layer was confined between a SiO_2 thermal insulation barrier and the two electrodes (W and Pt). The device design is shown in Figure 3.2. In this study, the authors found the formation of a conductive filament only at temperatures above 1500 K and attributed the SET process to local re-hybridsation from sp^3 carbon to sp^2 carbon, meanwhile the sp^3 content of the surrounding matrix increased slightly as a consequence of the constant volume approach used in the simulation [46]. The overall sp^3/sp^2 ratio showed only little variation (1 % to 2 %) [46]. The required temperatures of >1500 K are around the temperatures reported in annealing experiments (1000 °C to 1300 °C) for the direct conversion from to sp^3

to sp^2 bonding in amorphous carbon [114–116]. Similar temperatures were reported in finite-element simulations of electrical switching of ta-C through localised Joule heating effects ([47] and this work). The findings of the MD investigations that were carried out in tandem, and in collaboration, with work of this thesis are presented in Appendix A.

2.5.2 RESET Process

The underlying physical mechanisms of the RESET process are less understood in comparison to the SET process. Finite element simulations suggest that the confinement of the current to the conductive filament leads to high temperatures, via Joule heating, of around 2100 K [67]. This localised heating consequently causes large temperature gradients within the device [67, 113]. Insights from molecular dynamic simulations that were carried out in tandem with the work of this thesis suggest that the large temperature gradient is vital to induce the reverse switching process, as no reversible switching occurred in the absence of a large temperature gradient between the conductive filament and its surroundings [46]. Similar findings are reported from quantum molecular dynamic simulations were the instant cooling of a metastable graphite-like liquid from 5000 K to 300 K lead to the formation of a DLC structure [110]. A similar result was also obtained from *ab initio* simulations where cooling from 5000 K to 300 K resulted in a higher sp^3 content for higher cooling rates [117]. It is conjectured that the large temperature gradient leads to thermally induced compressive stresses that trigger the transition from sp^2 bonded carbon to sp^3 bonded carbon [113]. This is similar to reports stating that local compressive stresses may aid in the stabilisation of the metastable sp^3 phase during deposition [72, 114, 118]. The findings of the MD investigations that were carried out in tandem, and in collaboration, with work of this thesis are presented in Appendix A.

2.6 State-of-the Art Benchmarks

The key characteristics of memory devices based on ta-C and a-CO_x are presented with their key attributes in Table 2.2. To avoid a misleading impression about the capabilities of each carbon-based storage technology, the best specifications that were available from one type of device were taken. The key characteristics presented in Table 2.2 are those existing at the start of, or emerging during, the work of this thesis. They are updated with the results obtained in the work of this thesis in Table 7.1 in Section 7.1. In addition to these key characteristics, MLC and the use of memristive effects for memcomputing purposes were investigated in Sections 6.3, 6.4 and 6.5.

Table 2.2: Specifications of device performances for ta-C and a-CO_x.[6]

	ta-C	a-CO_x
Maturity	Emerging	Emerging
Film Thickness	22 nm(7)	18 nm(8)
Device Diameter	240 nm(7)	50 nm(8)
SET Speed	50 ns(7)	50 ns(8)
RESET Speed	10 ns(7)	10 ns(8)
Retention Time	10 h @ 300 °C(7)	10^4 s @ 85 °C(8)
Endurance Cycles	10^3(7)	4×10^4(8)
Write Energy per Bit	<1 pJ(7)	≈10 pJ(8)

(7) Taken from [119]
(8) Taken from [63]

[6] An updated version is provided in Section 7.1.

Chapter 3

Experimental & Simulation Methods

The ta-C and a-CO_x confined-cells and the ta-C cross-bar devices investigated in this thesis were fabricated under the auspices of the Seventh Framework Programme (FP7) project Carbon Resistive Random Access Memory Materials (CareRAMM). The fabrication of the confined-cells and cross-bar devices was carried out by V. P. Jonnalagadda at IBM Research Zurich, whereas the ta-C deposition and characterisation was carried out by Dr. A. K. Ott at Cambridge University.

Partial results of the presented work in this chapter have been published in:

- ”Joule Heating Effects in Nanoscale Carbon-based Memory Devices,” in 2016 *IEEE Nanotechnology Materials and Devices Conference (NMDC).*, pp. 1–2, IEEE, 2016. *DOI: 10.1109/NMDC.2016.7777081*
- ”Temperature Evolution in Nanoscale Carbon-Based Memory Devices due to Local Joule Heating,” in 2017 *IEEE Transactions on Nanotechnology.* IEEE, 2017. *DOI: 10.1109/TNANO.2017.2674303*

3.1 Experiments

3.1.1 Tetrahedral Amorphous Carbon (ta-C)

To identify the most promising film thickness for the application as non-volatile memory, different film thicknesses of ta-C ranging from 5 nm to 100 nm and different deposition parameters were explored. For each ta-C film thickness, one chip was fabricated. The devices on each chip were available with three different diameters (50 nm, 100 nm and 200 nm) and three different on-chip load resistor values, thus giving a total of 9 different combinations per tested chip. Each chip contained more than 500 devices.

Material Deposition & Characterisation All the ta-C films used in this thesis were deposited using the FCVA method (as described in Section 2.2). The active material, ta-C was deposited into openings (of confined-cell devices) with diameters ranging from 50 nm to 200 nm. The deposition parameters that were used to deposit the ta-C films are provided in Table 3.1.

To determine the sp^3 content, films with different thicknesses were directly deposited on

Table 3.1: Deposition parameters of the ta-C layers.

Ion energy	28 eV
Coil current	7 A/8 A
Temperature	RT
Diameter of cathode	9 cm
Density of cathode	2.3 g cm^{-3}
Purity of graphite target	99.999 %
Deposition rate	0.39 nm s^{-1}

a silicon substrate and the sp^3 content was determined using multi-wavelength Raman spectroscopy (as described in Section 2.3) [114]. The multi-wavelength Raman spectra of a 5 nm thick ta-C film is exemplarily shown in Figure B.1 of Appendix B.1. The obtained G peak dispersion allows the determination of the Young's modulus, the density and the sp^3 content of the ta-C thin films (as described in Section 2.3). The Raman analysis of 5 ± 1 nm, 10 ± 1 nm, 15 ± 1 nm and 20 ± 1 nm thick as-deposited ta-C films is provided in Figure B.2. The sp^3 content of ta-C thin films deposited on Si substrates, as determined via Raman analysis, is shown in Figure 3.1 as a function of the film thickness of film thickness over the thickness range from less than 1 nm to 10 nm. The uncertainty in the determination of the sp^3 content is ± 5 %.

It can be seen from Figure 3.1 that the sp^3 content increases with increasing film thickness until a maximum of ≈70 % is reached for thicknesses of 5 nm or larger. The initial

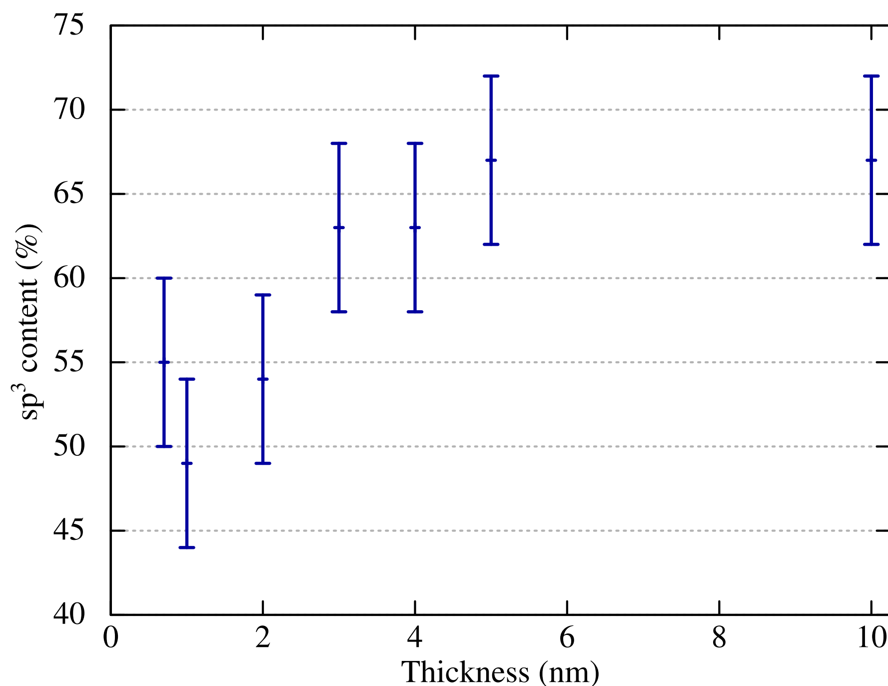


Figure 3.1: The carbon sp^3 content for ta-C thin films in this thesis is shown as a function of the film thickness. Films were deposited using the FCVA method onto Si substrates.

dependence of the sp^3 content on the thickness is reported to be a consequence of the film composition [71]. The middle 'bulk' layer is sp^3-rich and is sandwiched between an sp^2-rich outer surface layer ≈0.5 nm and an interfacial layer of 1 nm to 2 nm thickness [71]. Hence, the contribution of the 'bulk' layer to the sp^3 content is reduced at small thicknesses. The sp^3 content of carbon thin films is higher when deposited directly onto the Si substrate (see Figure 3.1) than when deposited onto the Pt bottom electrodes of the confined-cell devices used for electrical testing (see Table B.2), due to Si suppressing the formation of sp^2 bonds at the Si-C interface [120].

The best experimental results in terms of switching voltage, endurance and switching speed (see Sections 4.4 and 4.6) were obtained on 5 nm confined-cell devices (having the cell structure shown in Figure 3.2). The mechanical properties of the 5 nm confined-cell, as well as the density and the sp^3 content was determined using multi-wavelength Raman spectroscopy [114] and is presented in Table 3.2.

The sp^2 content of the ta-C layer deposited on platinum (the material used as a bottom electrode layer in this study) is lower than when directly deposited on a silicon substrate, due to silicon only forming σ bonds with carbon (cf. Figure 3.1). The confined-cell architecture is schematically schematically in Figure 3.2a. The ta-C layer is spatially confined between silicon dioxide on the sides, and the top and bottom electrodes. The cross-section of a device is depicted in an SEM micrograph in Figure 3.2b.

In total 108 ta-C thin films were deposited and characterised under the auspices of the

Table 3.2: Properties of a 5 nm thick ta-C layer deposited into a confined memory cell.

Young's modulus	439 GPa
Density	2.66 g cm^{-3}
sp^3 content	0.5

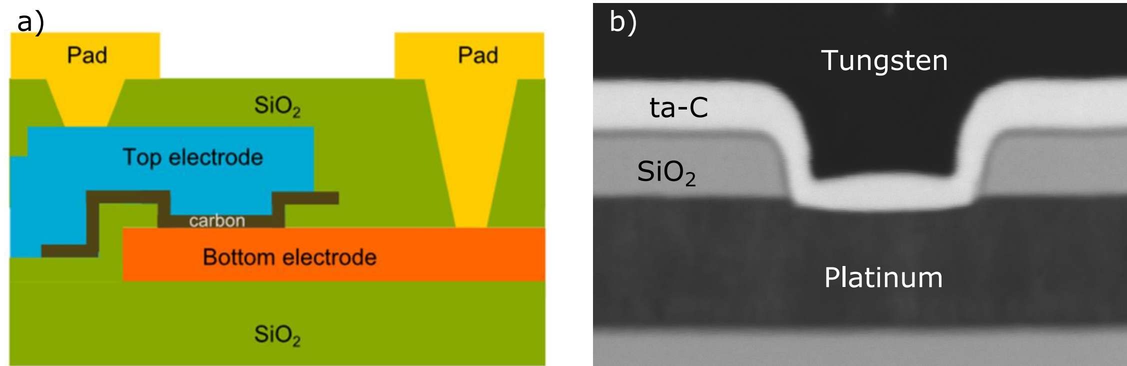


Figure 3.2: **a)** Schematic of the ta-C confined memory cell architecture. **b)** Cross-section of a ta-C confined-cell depicted in an SEM micrograph. [adapted from [46]].

FP7 project CareRAMM. In the work of this thesis approximately 1000 devices based on ta-C thin films were studied.

3.1.2 Oxygenated Amorphous Carbon (a-CO$_x$)

The memory devices based on the confined-cell architecture with a-CO$_x$ as active material were fabricated by collaborators at IBM Research Zurich. The films were deposited using the DC magnetron sputtering technique [63].

Material Deposition & Characterisation All the a-CO$_x$ films used in this thesis were deposited using the DC magnetron sputtering method (as described in Section 2.2) [63]. To identify the most promising film composition for the application as non-volatile memory, the oxygen partial pressure was varied from 0 µbar to 3.5 µbar [63]. The best switching results were obtained with 18 nm thick a-CO$_x$ films, deposited using an oxygen partial pressure of 1.5 µbar and a combination of a W bottom electrode and a Pt top electrode (other investigated electrode combinations consisted of W bottom electrode and W or Ti top electrode [63]) [63]. The deposition parameters that were used to deposit the a-CO$_x$

Table 3.3: Deposition parameters of the a-CO_x layer [63].

DC Plasma Power	600 W
Total Flow Rate	20 sccm
Oxygen flow rate	3 sccm
Total Pressure	10 µbar
Oxygen Pressure	1.5 µbar

films are provided in Table 3.3. The active material, a-CO_x was deposited into openings with diameters ranging from 50 nm to 200 nm (in a device configuration identical to the one for the ta-C devices shown in Figure 3.2). Oxygenated amorphous carbon is deposited into the openings from a solid carbon source in an O_2//Ar atmosphere.

A combined EDS and EELS (as described in Section 2.3) of a cross-section of a device was undertaken to confirm a uniform distribution of a-CO_x, and to exclude the presence of interfacial WO_x (which itself has resistive switching properties [121]). This analysis was done by correlating the intensity of the different element edges obtained from the EELS/EDS spectra with the spatial distribution inside the cell. The cross-section is shown element specific in Figure 3.3a, whereby the largest intensities are shown brightest. The RGB map is coded with red corresponding to O, green for C and blue for W. This confirms that there is a clear separation between the a-CO_x resistive switching layer and the W bottom electrode (i.e. no WO_x layer is formed). This is shown in more detail in Figure 3.3b, where the elemental distribution is shown as a function of the depth profile from the Pt top electrode to the W bottom electrode.

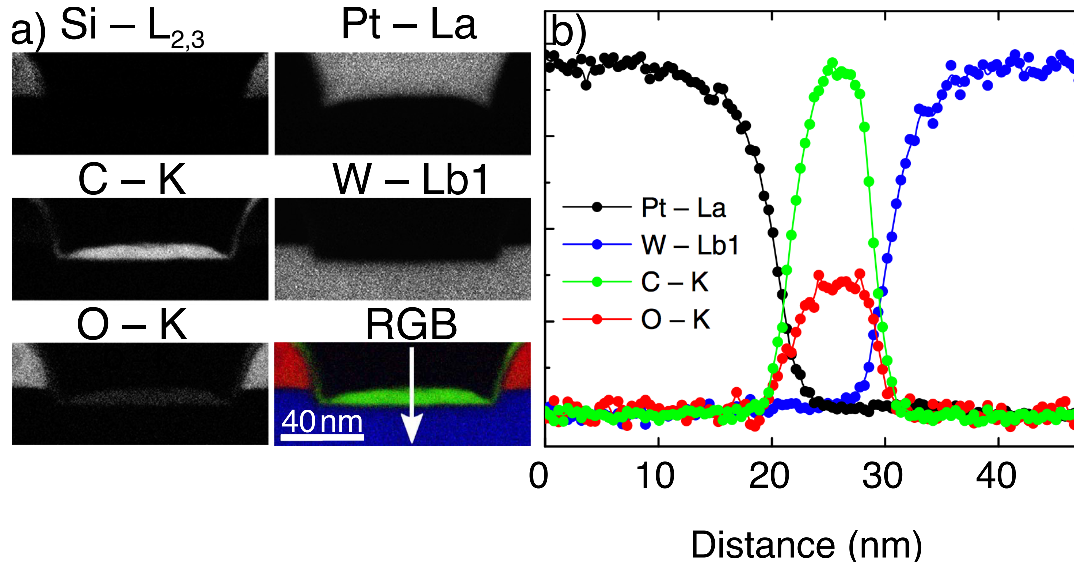


Figure 3.3: **a)** Elemental maps of cross-sectioned a-CO_x devices indicating the presence of Pt, W using EDS spectra and Si, C and O using EELS spectra. RGB map is coded with red corresponding to O, green for C and blue for W. **b)** Distribution of Pt, W, C and O [taken from [63]].

3.1.3 Device Design

The devices used in this thesis have a GSSGSSG (G = ground, S = signal) layout, which allows them to be contacted by two different electrical paths. One path uses an on-chip load resistor and limits the current flow during the SET process. The load resistors are written (via e-beam lithography) in series next to the device and have a small footprint (e-beam lithography) to reduce the flow of parasitic current through the device after dielectric breakdown (i.e. at the switch from HRS to LRS). The load resistors have values between 3 kΩ and 14 kΩ for the ta-C-based devices and ≈10 kΩ for devices based on a-CO_x as the active material [47, 63]. Gold interconnects and pads are deposited to probe the devices. More fabrication details can be found in [63]. The second path is used for the reverse switching process from the LRS into the HRS (which does not require the series on-chip resistor). A typical device with the active material sandwiched between the two electrodes is depicted in a scanning electron micrograph in Figure 3.4.

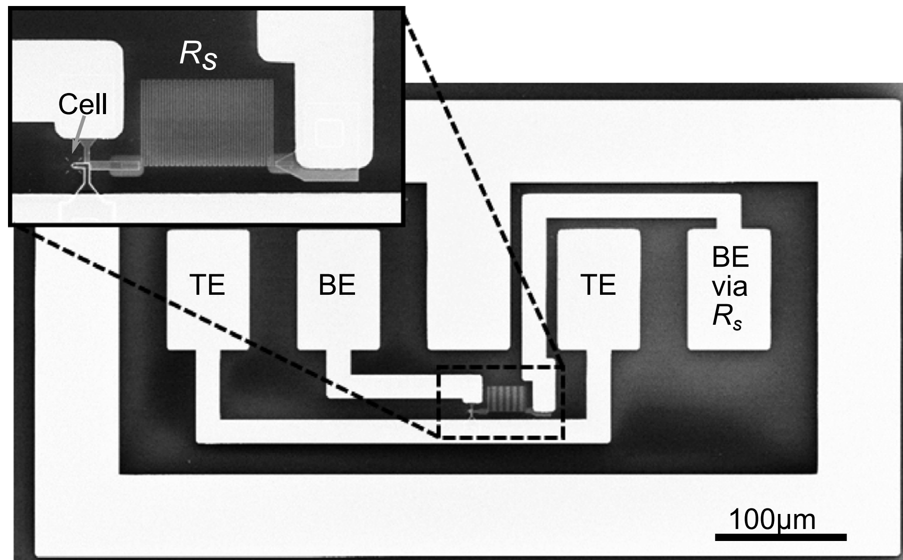


Figure 3.4: Scanning electron micrograph of a memory device with ta-C or a-CO_x as active material, sandwiched between the top (TE) and bottom (BE) electrode. The load resistor R_s is shown as inset [modified from: [63]].

3.1.4 Device Test Setup

To characterise the devices a benchtop setup was used for electrical switching and data retention measurements, and a cryogenic probing station was used to measure the conductivity at low temperatures.

Electrical Switching Setup The device-under-test (DUT) was mounted onto an invar block which was heated by in-built tungsten heaters. Depending on the type of experiment that was performed, either the path having the load resistor connected in series was used, or the path connecting the DUT directly to the probes. The electrical contact was done using high frequency Dual-Z probes (Cascade Microtech®). The AC voltage outputs to switch the devices between the LRS and the HRS were supplied by an arbitrary waveform generator (Agilent 81150A) and captured with an oscilloscope (Tektronix TDS3054B). A 50 Ω termination was placed close to the DUT during to application of fast (ns) pulses

to reduce voltage reflections due to the resistance mismatch at the DUT-transmission line interface, as well as to reduce parasitic current flowing through the DUT after dielectric breakdown occurred. To reduce the time constant τ of the parasitic current, another 50 Ω termination was placed after the DUT. The relation between the time constant of the voltage drop caused by the parasitic capacitive discharge, and the resistance R of the DUT and the capacitance C of the device test setup (including the DUT) is shown in equation 3.1) [122].

$$\tau = R \cdot C \tag{3.1}$$

The read out of the resistance state was done at 0.2 V using an SMU (Keithley 2400). The low side potential of the SMU was connected to ground. The 50 Ω next to the DUT was removed during the read out of the resistance (using the SMU) the 50 Ω. A schematic of the memory device and the electrical circuit used for electrical switching measurements is shown in Figure 3.5.

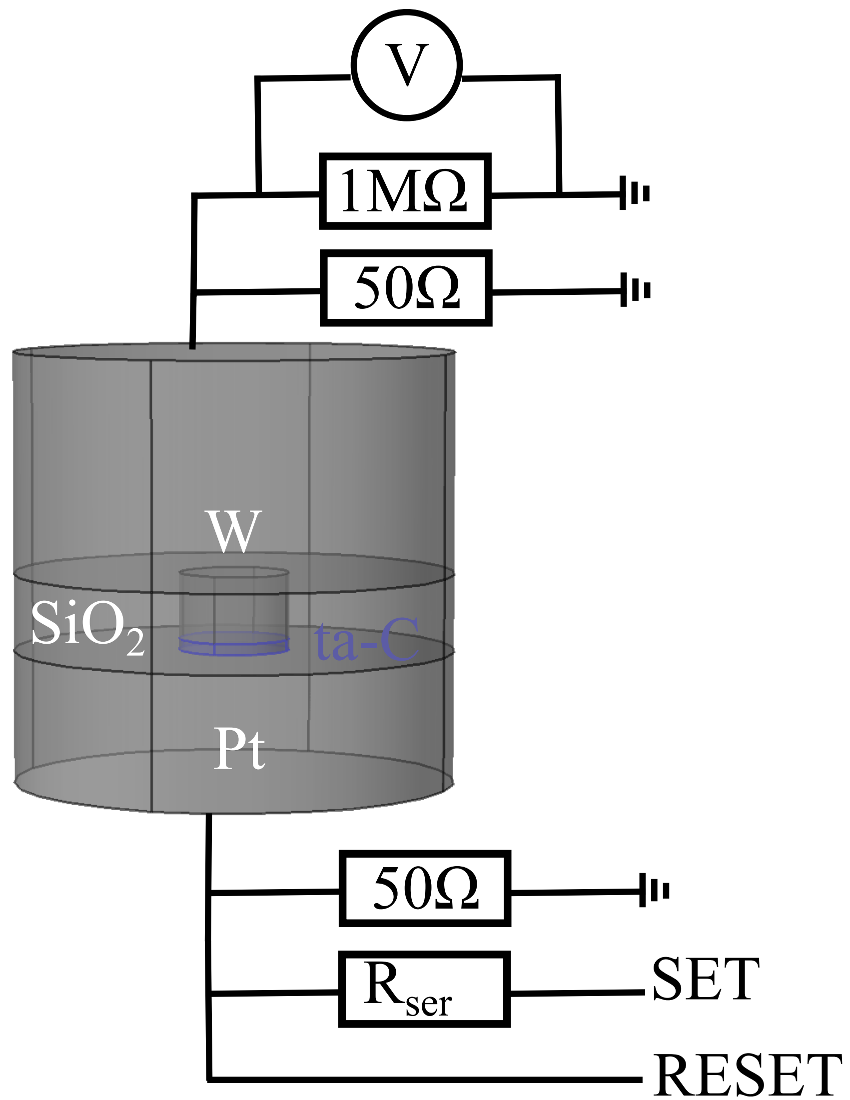


Figure 3.5: Schematic of a device (*here* ta-C) with the electrical connections used for testing. SET and RESET pulses are applied to the bottom electrode. A load resistor limits the current during the set process [modified from [8]].

Capacitance Evaluation The capacitances of the circuitry that are in parallel to the DUT have great impact on the switching characteristics [43]. In addition, the capacitances strongly influence the endurance of the carbon-based memory devices due to the capacitive current that is discharged once dielectric breakdown has occurred and the DUT is switched from the HRS into the LRS [43]. The fast dielectric breakdown speed ≈1 ns can lead to large capacitive currents [46]. Further, low capacitances are desired in order to capture the current response of the DUT accurately, when SET or RESET pulses are applied. The capacitance of the electric circuit including the DUT was determined to be ≈40 fF. This low capacitance together with a resistance of the DUT of around 50 kΩ at the onset of the dielectric breakdown event (cf. Figure 3.9) allowed the capture of switching events on the order of ≈2 ns (see equation 3.1).

Cryogenic Probing Station[9] To study the temperature dependence of the ta-C conductivity, the conductivity of pristine devices (HRS) was measured for temperatures between 85 K to 300 K at low voltages (<1 V) using a cryogenic probing station (JANIS ST-500-2-UHT). The temperature stability of the probing station is <50 mK [123].

A schematic of the vacuum chamber including the most important components is shown in Figure 3.6. The samples were fixed with clamps on top of the top chuck at A. The temperature was set using a temperature controller (Lakeshore 336) and measured using a silicon diode (DT-670B-CU-HT). The set temperature was adjusted using liquid nitrogen and a heater (50 W), indicated at A3 in Figure 3.6. The electrical measurements were carried out using high frequency Dual-Z probes (CascadeMicrotech®) that were connected to an SMU (Keithley 2636B).

[9] A more detailed description of the cryogenic probing station can be found in [123].

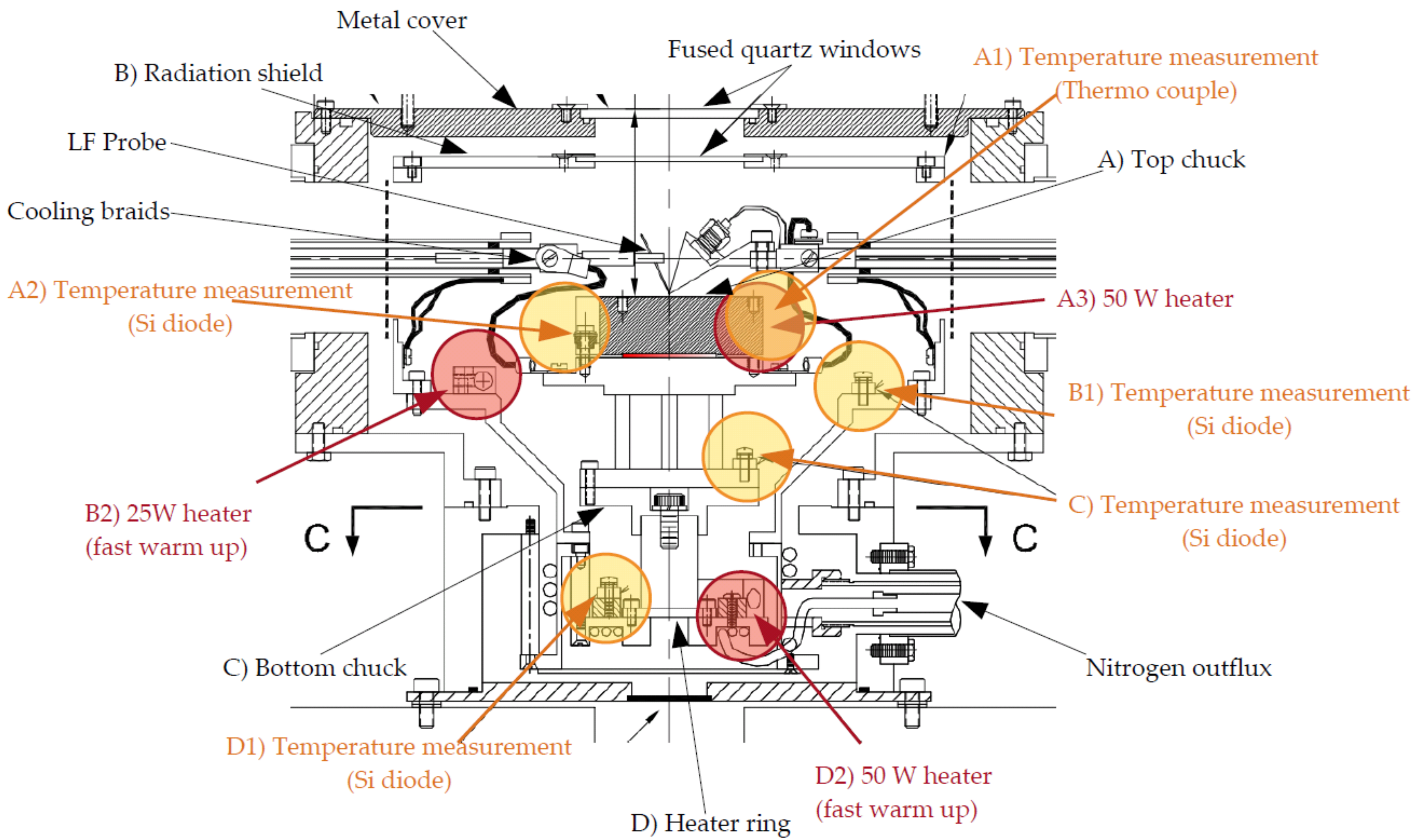


Figure 3.6: The samples were mounted on a copper sample mount A and connected with Dual-Z probes (CascadeMicrotech®). The temperature was sensed at four points: top chuck (A1,A2), radiation shield B1, bottom chuck C1 and heater ring D1. The temperature was adjusted with a heater (50 W) A3 and liquid nitrogen. The heaters at the radiation shield B2, and at the heater ring D2 were used for fast heating [taken from [123]].

3.2 Finite Element (FE) Simulations

The first part of this section describes the model that was used (in Sections 5.3, 5.5 and 5.6) to investigate Joule heating and the resulting temperature distributions within pristine ta-C confined-cell memory devices at the onset of memory switching. This is essential to gain further insights into the switching mechanism and to address the key challenge of cycling endurance (see Section 2.5.1). The model that is introduced in this section was developed in the work of this thesis and accounts for both electric field and temperature dependence of the electrical conductivity in ta-C thin films. It also considers local distributions of sp^2 and sp^3-rich clusters (see Sections 2.4.1 and 2.5.1). To obtain the temperature distribution in the device when a voltage is applied, a finite element software package (COMSOL®) was used to solve the coupled heat and Laplace equations. The simulations were validated with experimental data (see Section 5.3).

The second part of this section describes the model that was used (in Section 6.6) to investigate Joule heating and the resulting temperature distributions within a-CO_x confined-cell memory devices during the read out of the LRS and during the consecutive application of RESET pulses. The consecutive application of partial RESET pulses was carried out in Sections 6.4 and 6.5 to investigate the accumulation properties of a-CO_x based memory devices. The investigation of the temperature distribution during the read out of the LRS is important to verify that the read out does not affect the resistance state of the device (cf. Section 6.2). To achieve this, the maximum temperature obtained from the simulation of the read out of the LRS was compared with the temperatures used in an annealing experiment (see Section 6.6). The investigation of the temperature distribution during the application of partial RESET pulses (described in Sections 6.4 and 6.5) was carried out to shine light on the role that temperature plays during a series of input pulses. An estimate

of the local temperature distribution (and its change) during partial RESET pulses aids, for example, in assessing the basis to which arithmetic operations can be carried out using a previously defined set voltage pulse (see Section 6.5).

3.2.1 Electro-Thermal Model

To obtain the temperature distribution in the ta-C and a-CO_x devices when a voltage is applied, a finite element software package (COMSOL®) was utilised to simulate the electro-thermal properties. The *AC/DC* and *Heat Transfer* modules were used to solve the coupled heat and Laplace equations [124]. The heat equation is given in equation 3.2 and describes the time and space dependent heat flow within the device/material [124]. The material properties within each simulation cell were treated as isotropic due to the amorphous character of the films (though note that this does not mean the overall distribution of sp^2 and sp^3 clusters is isotropic — see Section 3.2.2). The specific heat capacity is denoted as C_p, $\partial T/\partial t$ is the time derivative of the temperature, k is the thermal conductivity and Q is the heat source term. The Laplace equation is given in equation 3.3 and describes the steady-state current flow in the presence of an electric field [124]. The density is denoted as ρ, the conductivity is σ, the electrostatic potential is V and ∇ is the nabla operator (differential operator in x, y, z).

$$\rho C_p \frac{\partial T}{\partial t} - k\nabla^2 T = Q \tag{3.2}$$

$$\nabla \cdot (\sigma \cdot \nabla V) = 0 \tag{3.3}$$

The coupling of equations 3.2 and 3.3 is given through the Joule heating effect. The Joule heating effect describes the resistive heating process that occurs when current flows through a device with a non-zero resistance. The power dissipation is described by equa-

tion 3.4, where P is the power, V the electric potential and I the current [124]. The coupling given in equation 3.5 describes the differential dissipated power dP per differential unit volume $dVol$ [124].

$$P = I \cdot V \tag{3.4}$$

$$Q = \frac{dP}{dVol} = \nabla V \cdot (\sigma \cdot \nabla V) \tag{3.5}$$

3.2.2 ta-C Device Modelling

Cluster Distribution To reflect local sp^2 variations in the models for ta-C films and devices, randomly distributed clusters of different sp^2-rich concentrations were used within the simulation cells. The sp^2 content was randomly assigned to each simulation cell using the probability density function (PDF) of the beta distribution [125]. The PDF of the beta distribution is defined between 0 and 1, which reflects the range of the possible sp^2 content in any particular simulation cell. Thus, the sp^2 content can be assigned randomly to each simulation cell by generating random values from the beta distribution. The random assignment of the sp^2 content is done by using Matlab® and invoking the in-built *betarnd* function. The shape of the PDF is described by the two parameters $\alpha > 0$ and $\beta > 0$ [125]. The PDF of the beta function is provided in equation 3.6 and the mean in equation 3.7 [125]. The gamma function is denoted by Γ.

$$PDF(r, \alpha, \beta) = \frac{\Gamma(\alpha + \beta)}{\Gamma(\alpha)\Gamma(\beta)} r^{\alpha - 1}(1 - r)^{\beta - 1} \tag{3.6}$$

$$mean = \frac{\alpha}{\alpha + \beta} \tag{3.7}$$

The variable r is the sp^2 content and is defined between 0 and 1 in each simulation cell. The PDF was chosen to be symmetric and reflects a mean sp^2 content of 0.5, and α =

$\beta = 2.65$. An sp^2 content of 0.5 was chosen to model the ta-C confined-cell devices that showed the best performance in terms of switching voltage, endurance and switching speed (see Sections 4.4 and 4.6). The values of α and β were chosen arbitrarily. The PDF used is thus as shown in Figure 3.7 for an sp^2 content of $r = 0.5$ and $\alpha = \beta = 2.65$. The threshold for sp^2-like conduction was set to 92 % within each simulation cell. Smaller values (than 2.65) for α and β result in a broader PDF, whereas larger values result in a narrower PDF around the mean. As long as the chosen values of α and β where high enough to account for the presence of sp^2 conductive clusters within the insulating sp^3 matrix, and small enough to prohibit the instantaneous formation of a conductive percolation path, no large variations were found for the simulated conductivities.

The simulated initial conductivity for a ta-C cell (of 50 nm diameter) with randomly distributed sp^2 clusters (as described above) is shown in Figure 3.8. The film thickness in this example was 5 nm reflecting the properties of the experimentally tested ta-C confined-cell

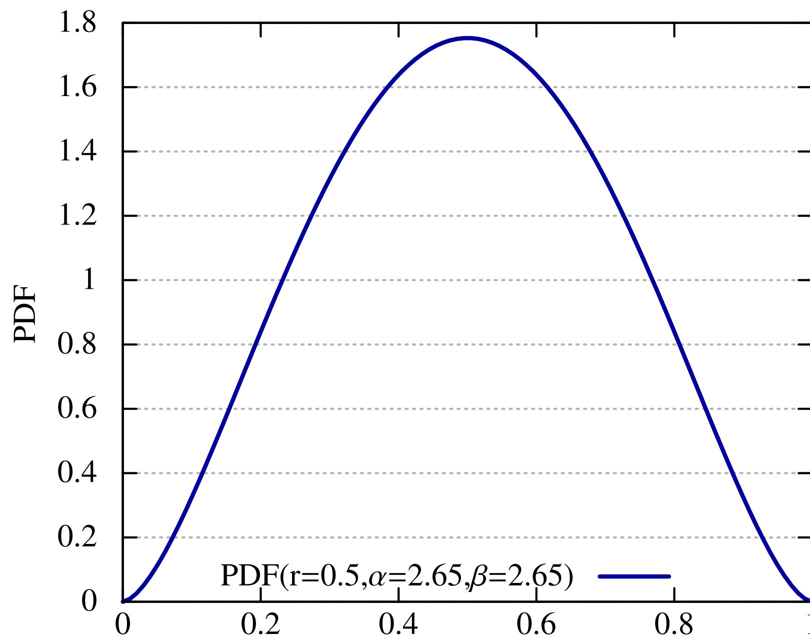


Figure 3.7: PDF of the beta distribution function (used to model the distribution of sp^2 concentration).

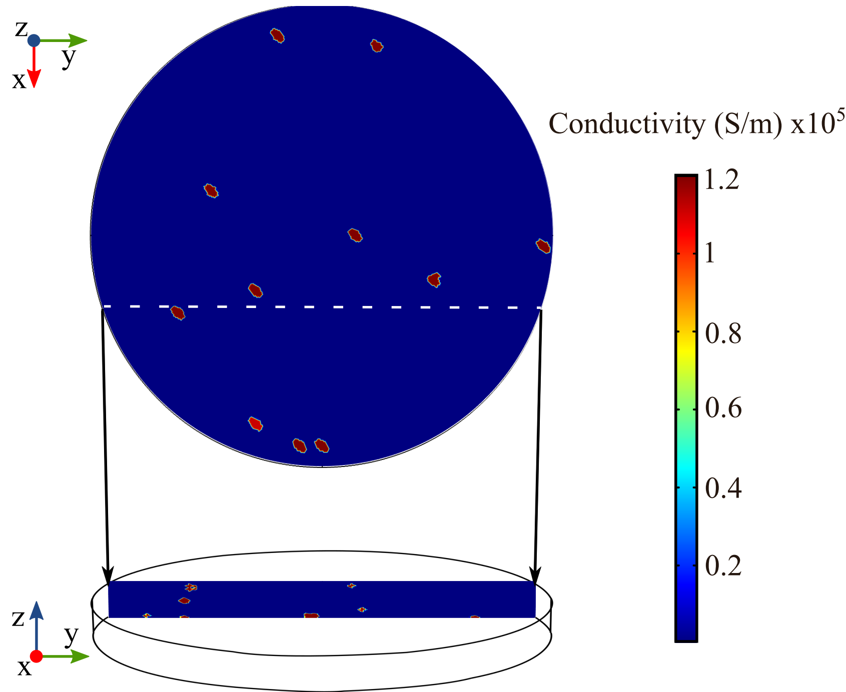


Figure 3.8: Initial conductivity, as calculated via the FE model, for randomly distributed sp^2-like conductive clusters in an sp^3 matrix (red); top shows conductivity in the x,y-plane (at z = 3.3 nm); bottom shows conductivity in the y,z-cross-section (indicated by the dotted line) [taken from [47]].

devices (see Table 3.2). The choice of the mesh size that was used to solve the coupled heat and Laplace equation within COMSOL® was found to influence the choice of conductivity values (cf. Table 3.2.4) that were used to reproduce the experimentally determined conductivity (see Figure 5.6). However, as long as the experimentally determined conductivity was reproduced, the obtained temperature distributions (see Figures 5.8 and 5.9) were similar.

The cross-section in Figure 3.8 shows the conductivity in the x,y-plane at z = 3.3 nm (i.e. 3.3 nm from the bottom electrode-ta-C interface). The vertical distribution of the sp^2-like conductive clusters in the y,z-plane is shown at the bottom of Figure 3.8. The most important material properties used in the simulation of the ta-C devices are summarised in Table 3.4 in Section 3.2.4.

Electrical Switching Pulse Different experimental switching curves were compared to examine the time response of the current on the application of a SET voltage in pristine ta-C devices. This evaluation was carried out to ensure that the implemented model would produce realistic temperature profiles, and that any 'undesirable' transient effects that would occur in experimental switching curves for very short pulses, could be excluded.

Experimental device I-V characteristics for a (typical) trapezoidal voltage pulse with a 15 ns leading edge (LE) followed by a 45 ns plateau and a 15 ns trailing edge (TE) [46] were applied to a pristine ta-C device and compared with a quasi-static triangular pulse with 5 µs LE and TE that was applied to a different pristine device (on the same chip). The voltages applied across the device are plotted (blue) in Figure 3.9, together with the voltage drop across a typical ta-C cell (red) and the corresponding currents. For noise reduction a 200 MHz software filter is applied to the current and voltage signals during post-processing with the exception of during the actual switching event.

It can be seen that the voltage pulse in Figure 3.9a reached the plateau of the trapezoidal pulse after 15 ns, during which little or no increase in current, see Figure 3.9b, was noted (1). The current then began to increase (2) and a dielectric breakdown set in after 30 ns (3). From then on the current followed the voltage pulse (4). This indicated that the electric field alone, in the absence of sufficiently large currents, did not trigger memory switching (cf. Section 2.5).

No such time lag (between voltage and current) could be observed for the slow, quasi-static pulse. There, the current (see Figure 3.9c) always followed the voltage pulse (Figure 3.9d) until dielectric breakdown occurred after 4.8 µs ((5) in Figure 3.9d) and the device was switched from its HRS into the LRS. As a consequence of the absence of any 'undesirable' transient effects in the slow, quasi-static pulse, the simulations were validated using the same SET pulse characteristics as in this experiment (see Figure 3.9d).

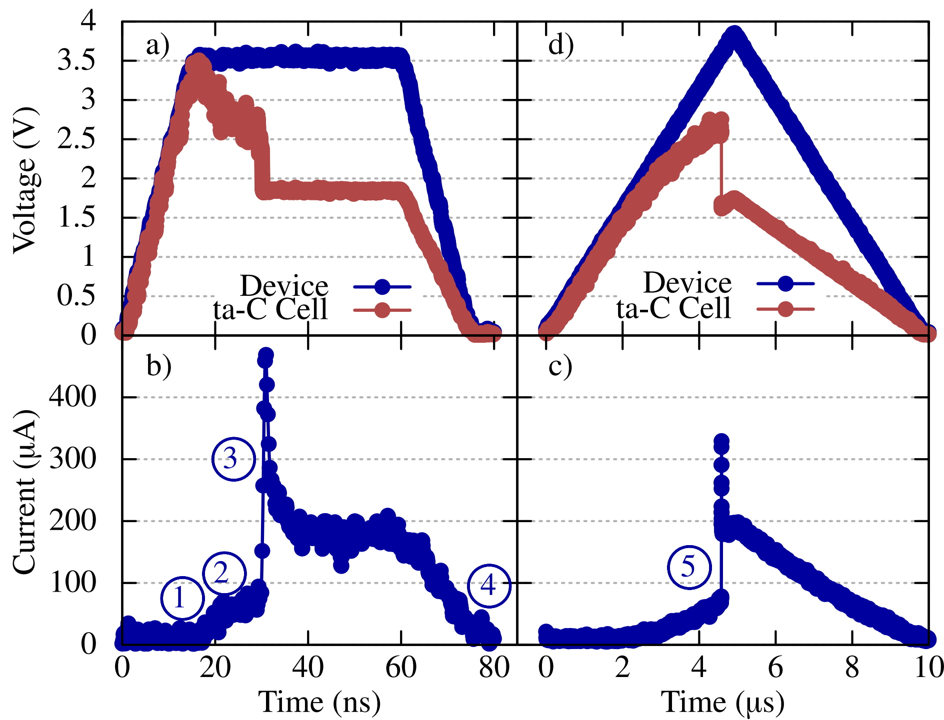


Figure 3.9: Applied voltage over devices (blue) and cells (red) together with the corresponding current response for **a)**, **b)** fast (80 ns) and **c)**, **d)** slow (10 μs) pulses [taken from [47]].

This, in turn, allowed the obtaining of a realistic temperature profile of the memory device at the onset of memory switching using FE simulations (presented in Section 5.3).

3.2.3 a-CO$_x$ Device Modelling

a-CO$_x$ Cell Properties A model of an a-CO$_x$ device in the LRS was developed in the work of this thesis to investigate the temperature distribution during the read out of the LRS of a-CO$_x$ devices, as well as during the application of consecutive (partial) RESET pulses (described in Section 6.5). These studies were carried out to ensure that the read out does not affect the resistance state of the device (cf. Section 6.2) and to highlight the role that temperature plays in achieving different resistance levels (see Section 6.3). The

conductivity of a-CO$_x$ devices in the LRS was assumed to be almost entirely dominated by a conductive filament consisting of highly reduced a-CO$_x$ in an otherwise insulating sp^3-rich a-CO$_x$ matrix. Such a conductive filament is established during the SET process, similar to memory devices based on ta-C (see Section 2.5 and [63]). The sp^2 content of the conductive filament was (arbitrarily) set to 0.55 in the simulation. The choice of the sp^2 content of the conductive filament filament was found to affect the maximum temperature reached in the centre of the simulated cell, whereby a higher sp^2 content resulted in a higher maximum temperature due to the lower heat conductivity of sp^2 bonded carbon (see Table 3.4). However, for sp^2 contents higher than 0.55, the temperature in proximity to the W electrode where the oxygen species are located after the SET process [63] remained at low temperatures (<200 °C) during the simulation of the resistance read out. The film thickness of the simulated a-CO$_x$ cell was 18 nm and the diameter was 100 nm. These dimensions reflect the device dimensions used in the experiments and simulations in Chapter 6. The conductivity was simulated on an a-CO$_x$ device that was experimentally SET into the LRS via an I-V sweep (see Section 6.5). In this case the SET process led to a resistance of ≈2.5 kΩ. Therefore, the diameter of the conductive filament in the simulation was set to 8.8 nm, so as to generate similar resistances to the measured device resistances. This value (8.8 nm) is also in close agreement with a reported carbon filament diameter of 10 nm as a consequence of a high amplitude quasi-static set pulse [43].

The diameter of the conductive filament was kept constant throughout the simulations, but in order to account for the experimentally observed resistance increase during the application of consecutive partial RESET pulses (see Figure 6.5), the conductivity of the filament was adjusted such that the simulated read out of the resistance of the device was equal to the experimentally obtained resistance of the device (cf. Figure 6.5a and Figure 6.8). A schematic of the conductive filament embedded in the a-CO$_x$ matrix is shown in Figure 3.10. The conductive filament is highlighted in blue. Other aspects of

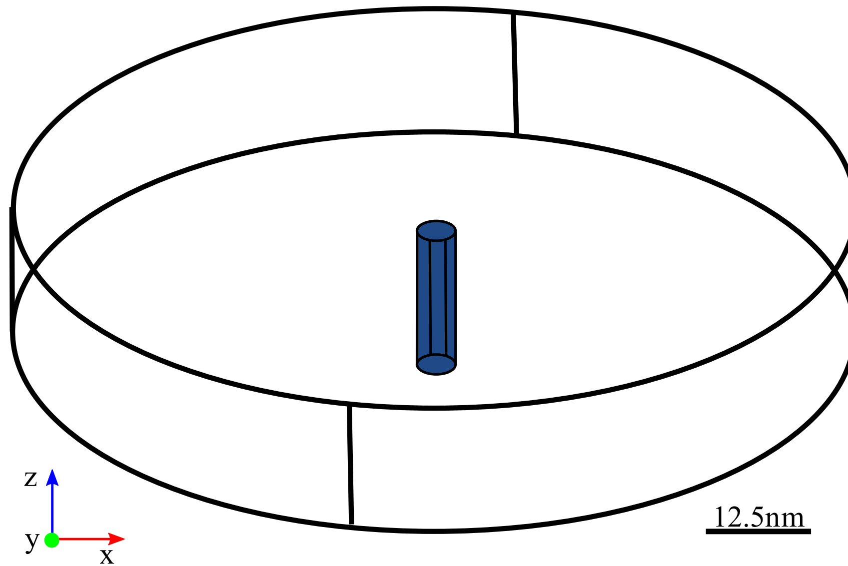


Figure 3.10: Schematic of a conductive filament (blue) bridging top and bottom electrode (electrodes are omitted for clarity) in an a-CO$_x$ device.

the computational model are equivalent to the model used to investigate the temperature distribution in the ta-C devices (see Figure 3.5). The most important material properties used in the simulation of the a-CO$_x$ devices (with the exception of the conductivity of the conductive filament) are summarised in Table 3.4 in Section 3.2.4.

Electrical Switching Pulse The temperature distribution during the read out of the LRS was simulated using a quasi-static trapezoidal pulse with an amplitude of 0.2 V and a duration of 100 ms and a leading and trailing edge of 10 ms each. A slow quasi-static pulse was chosen to account for the slow experimental read out using an SMU.

The temperature distribution that occurs during the application of a series of consecutive (partial) RESET pulses was simulated using short (8 ns), low voltage (−0.9 V) pulses, equivalent to the pulses used in the experiment (see Figure 6.5). The voltage applied across the device is thus as plotted in Figure 3.11.

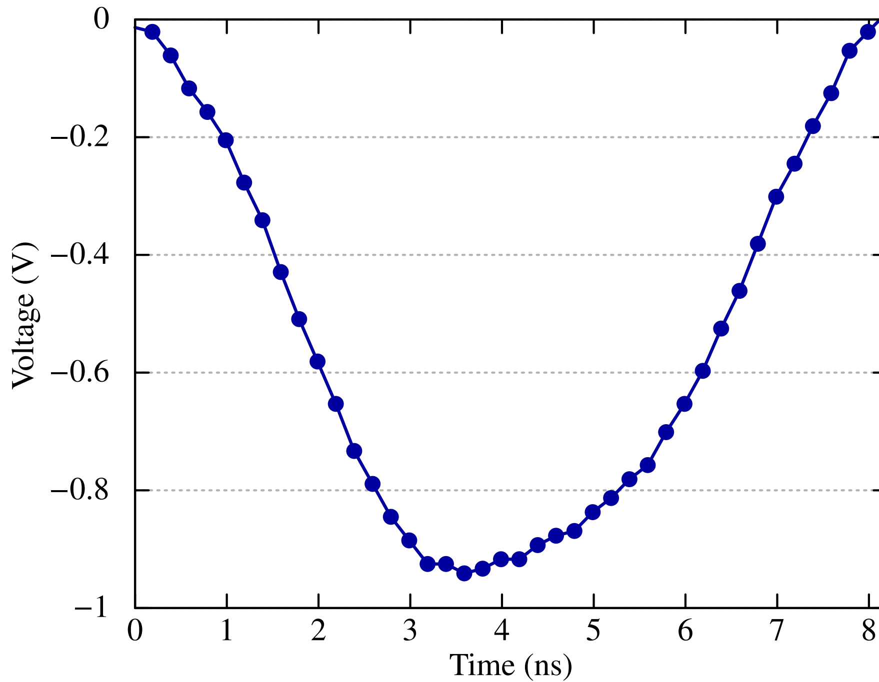


Figure 3.11: A partial RESET pulse (out of a series of consecutive (partial) RESET pulses) applied across an a-CO_x device in the LRS.

3.2.4 Simulation Parameters

The density of amorphous carbon is known to depend linearly on the sp^3 content [70]. Within the framework of the simulation, literature data was fitted to provide the density as function of the sp^3 content of the simulation cell [70]. The specific heat capacity was determined by Dr. Federico Zipoli at IBM Research Zurich (under the auspices of the CareRAMM project) using MD dynamic simulations with a ta-C cell containing an sp^3 content of 0.5. The thermal conductivity is linked linearly to the density [126], and so can be extracted from it. The electrical conductivity of ta-C was determined in Chapter 5 and was found to be field- and temperature-dependent. The most important material properties used in the simulation are given in Table 3.4. The same parameters were used for ta-C and a-CO_x cases, with the exception in the latter case of the electric conductivity of the conductive filament, which was adjusted for each simulation such that the simulated

device resistance was equal to the experimentally obtained device resistance.

Table 3.4: Material parameters of the ta-C and a-CO$_x$ FE model [taken from [47]].

Parameter	Value
sp^3-content (%)[10]	50
Beta (α, β)[11]	$2.65, 2.65$
σ_{sp^2} (S m^{-1}) (cf. [113])	1.2×10^5
$\sigma_{\mathrm{sp}^3,\mathrm{Ohmic}}$ @ 300 K (S m^{-1})	0.0115
σ_{00} (S m^{-1})	$0.345 \cdot \exp\left(-\frac{220\,\mathrm{K}^{1/4}}{T^{1/4}}\right)$
σ_{sp^3} (S m^{-1})	$\sigma_{00} \cdot \sinh\left(\frac{E}{9.5 \cdot 10^9 \left[\frac{\mathrm{V}}{\mathrm{m}}\right]}\right) + \sigma_{\mathrm{sp}^3,\mathrm{Ohmic}}$
Threshold σ_{sp^2} (%)	92
ρ (kg m^{-3}) [70]	$3460 - 1880 \times sp^2$
λ $\left(\mathrm{W\,K^{-1}\,m^{-1}}\right)$ [126]	$1.77 \cdot \rho - 2.82$
$C_{p,avg}$ $\left(\mathrm{J\,kg^{-1}\,K^{-1}}\right)$[12]	2050

[10] Determined using multi-wavelength Raman spectroscopy
[11] Beta distribution with parameters α and β
[12] Average heat capacity of a memory cell computed from molecular dynamic simulations

3.2.5 Summary

In this chapter the deposition methods and material properties of the ta-C and a-CO_x devices that were used in the framework of this thesis were presented. Further, the design of the ta-C and a-CO_x memory devices was provided, together with descriptions of the experimental device test setups that were used to investigate the switching and retention properties of the ta-C and a-CO_x memory devices, and the low temperature conduction properties of the ta-C memory devices. Additionally, the material parameters and electric pulses used within the framework of the computational modelling are provided. It was emphasised that the computational model that was developed to simulate the electrical conductivity of pristine ta-C confined-cell devices accounts for local sp^2 and sp^3 variations, which in turn affect the local electrical conductivity, density and heat conductivity.

Chapter 4

Tetrahedral Amorphous Carbon (ta-C) Devices

Partial results of the presented work in this chapter have been published in:

- ”Carbon-Based Resistive Memories,” in 2016 *IEEE 8th International Memory Workshop (IMW)*, pp. 1–4, IEEE, 2016. *DOI: 10.1109/IMW.2016.7493569*
- ”Temperature Evolution in Nanoscale Carbon-Based Memory Devices due to Local Joule Heating,” in 2017 *IEEE Transactions on Nanotechnology.* IEEE, 2017. *DOI: 10.1109/TNANO.2017.2674303*

Electrical experiments on ta-C devices were done in two parts. A first basic electrical characterisation was done on cross-bar devices with a carbon area coverage of 1 μm^2, 4 μm^2 and 16 μm^2. The cross-bar devices had ta-C film thicknesses of 5 ± 1 nm, 10 ± 1 nm, 15 ± 1 nm and 20 ± 1 nm. The on-chip series load resistors were 3 kΩ to 14 kΩ. An optical image of a cross-bar device is shown in Figure 4.1.

Reversible switching experiments were carried out using confined-cells, due to their low capacitances and smaller cross-sectional area (see Section 3.1.1). The best switching results were obtained on confined-cell devices with a film thickness of 5 ± 1 nm.

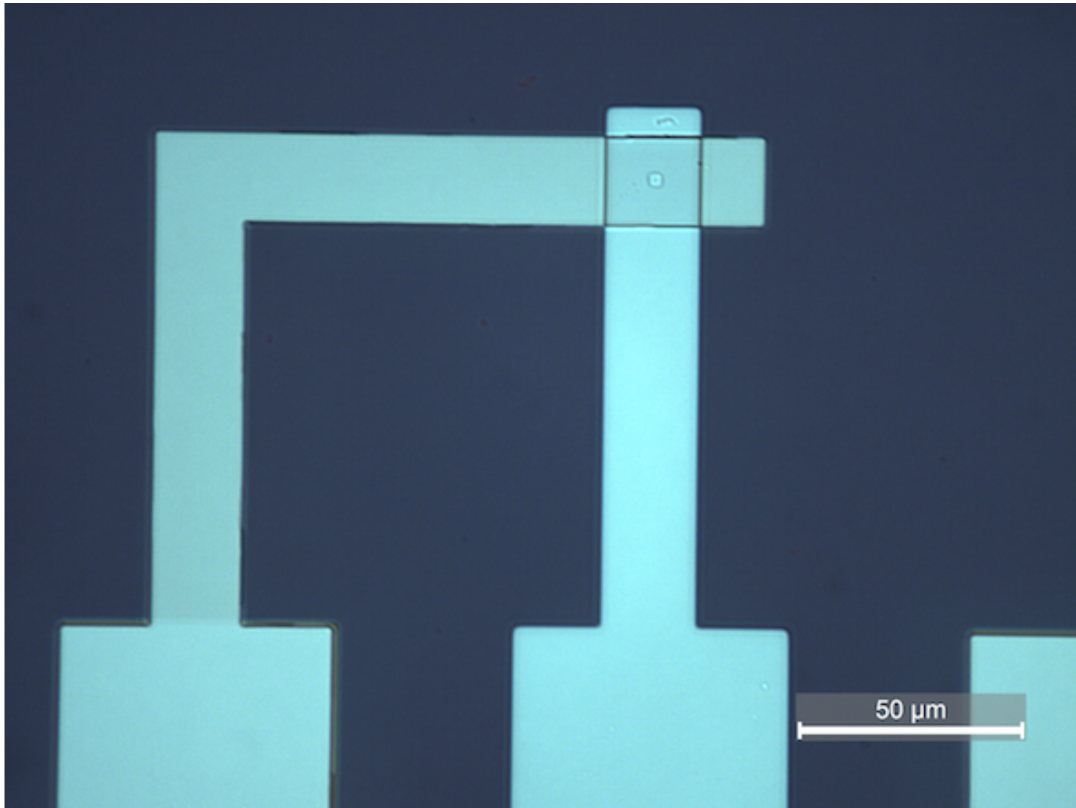


Figure 4.1: Optical image of a cross-bar device, as used for basic electrical characterisation of ta-C devices.

Additional experiments were also performed on confined-cells with film thicknesses of 10 ± 1 nm, 15 ± 1 nm and 20 ± 1 nm.

For the remainder of this thesis the uncertainty in the film thickness of ± 1 nm will be omitted for better readability and the given film thicknesses refer to the nominal film thicknesses.

An overview of the tested confined-cell and cross-bar devices is provided in Tables B.1 and B.2 in Appendices B.2 and B.3. Details about the fabrication of the confined-cell devices and the material properties of the confined-cell with a 5 nm thick ta-C film are provided in Sections 3.1.1, 3.1.3 and 3.1.4.

4.1 Initial Characterisation

4.1.1 Area Dependence

To investigate the current dependence of ta-C-based devices for different cell areas, more than 90 cross-bar devices were switched from the pristine state into the LRS using quasi-static IV measurements. To protect the device in the LRS from excessive current, the current compliance was set to 25 mA. The current is shown as a function of the applied voltage for three exemplar selected cross-bar devices in Figure 4.2, here for devices with 5 nm ta-C layers and contact areas of 1 μm^2, 4 μm^2 and 16 μm^2.

The current increased strongly as the applied voltage is increased, and all devices switched

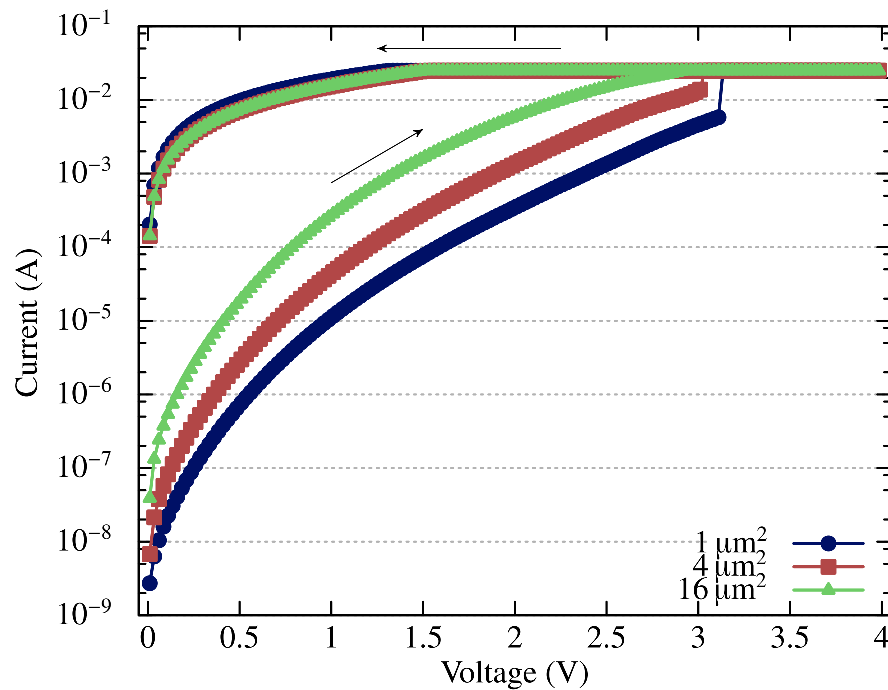


Figure 4.2: IV curves of pristine cross-bar devices with 5 nm ta-C layers and contact areas of 1 μm^2, 4 μm^2 and 16 μm^2. The current compliance was set to 25 mA to protect the device in the LRS.

from the HRS to the LRS. The conductivity of all devices in the LRS is high enough that the current compliance 'kicks-in' at 25 mA. Further, the current required to induce dielectric breakdown showed a correlation with the lateral dimensions of the ta-C devices. This result suggests that a viable way to reduce the energy and power consumption of ta-C-based memory devices is to reduce the lateral dimensions (i.e. smaller area). This correlation between smaller lateral dimensions and a reduced switching current was also confirmed by finite element simulations that were undertaken as part of this work (see Section 5.6). The observation that the SET process occurs at higher currents and lower voltages for devices with larger lateral dimensions, but same thicknesses, provides evidence that the switching mechanism in ta-C cannot just depend on the applied electric field (cf. Section 2.5.1). The lower switching voltages for devices with larger areas is likely a consequence of their lower resistance and hence, higher power dissipation (see equation 3.4).

The link between the lateral dimensions of the ta-C devices and the switching current required to induce the SET process becomes clear from Figure 4.3, where the data shown in Figure 4.2 is plotted as current density against applied voltage. The devices with larger lateral dimensions (i.e. larger area) showed a lower current density at the onset of the SET process for the same applied voltage. This shows that the threshold voltage (to switch the devices from the HRS into the LRS) in ta-C-based memory devices does not — or only indirectly — scale with the area.

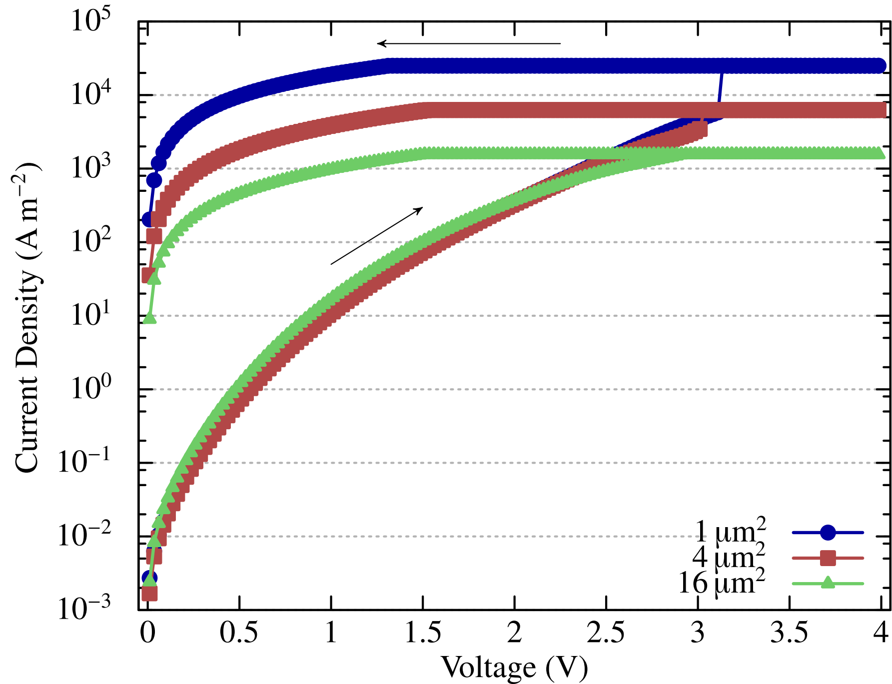


Figure 4.3: Current density of the pristine cross-bar devices presented in Figure 4.2.

4.1.2 Electric Field Dependence

To relate the current density to the electric field, more than 60 cross-bar devices with different thicknesses and areas of the ta-C layer were studied. The DUTs had film thicknesses of 5 nm and 10 nm. The current density is plotted as a function of the electric field in Figure 4.4 for two exemplar cross-bar devices with contact areas of 4 μm^2. The current compliance was set to 25 mA for the device with a 5 nm ta-C and to 10 mA for the more resistive device with a 10 nm ta-C layer.

It can be seen in Figure 4.4 that at low electric fields, the current density was higher for the devices with a 5 nm ta-C layer in comparison to the devices with a 10 nm layer. At high electric fields, the current density increased more strongly for the devices with the 10 nm ta-C layer. Additionally, the electric field required to induce the dielectric breakdown was lower for the 10 nm case. The increased low field current density of the devices with the

5 nm thick ta-C layers can be explained with their higher sp^2 content (0.5 vs. 0.4). As discussed in Section 2.4.2, the low-field conductivity is reported to be governed by VRH. A higher sp^2 content leads to a higher density of states within the mobility gap, which in turn leads to a reduced hopping distance. Assuming VRH transport at low electric fields, the reduced hopping distance then leads to a higher conductivity in the devices with 5 nm thick ta-C layers [99, 114].

The non-linear dependence of the current density on the electric field indicates that the (electric) conductivity σ, which is linked to the electric field E and current density j via equation 4.1, is field dependent [127]. The possibility of Schottky barriers (at the electrode-carbon interfaces) dominating the obtained electrical conductivities was addressed and ruled out in Sections 4.5 and 5.2.

$$j = \sigma \cdot E \tag{4.1}$$

Further, the dielectric breakdown voltage in the tested devices is close to double the value for the device with a film thickness of 10 nm, in comparison to the device with a film thickness of 5 nm (as expected from equation 4.1). The field (and temperature) dependence of the ta-C conductivity was studied in more detail on confined-cell devices in Sections 5.1 and 5.2.

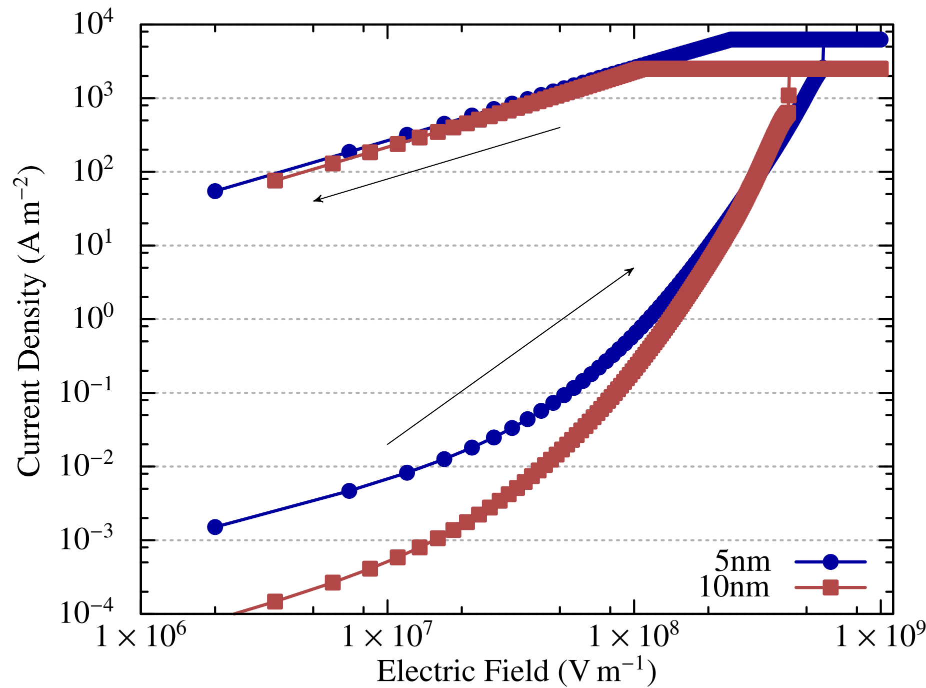


Figure 4.4: The current density is plotted as function of the electric field across pristine crossbar devices with ta-C layer thicknesses of 5 nm and 10 nm and contact areas of 4 µm^2.

4.2 Unipolar Switching

To explore the unipolar (cf. Section 1.4) switching capabilities of ta-C devices, confined-cell structures were switched from their HRS to their LRS and then back again using single polarity voltage pulses. An exemplar set of results is shown in Figure 4.5. Here, a 100 nm diameter, 5 nm thick ta-C confined-cell device was SET from the HRS (not pristine state) into the LRS using a SET pulse with an amplitude of 3.5 V and a duration of 80 ns. The subsequent RESET pulse used to switch the device back into the HRS had an amplitude of 3.3 V and a duration of ≈7 ns. The voltage drop is plotted across the device (including the 13.4 kΩ load resistor) as well as across the ta-C confined-cell alone, to highlight the load shift at the switching event. No load resistor was present during the reverse switching from the LRS into the HRS. The timelines of the current signals are

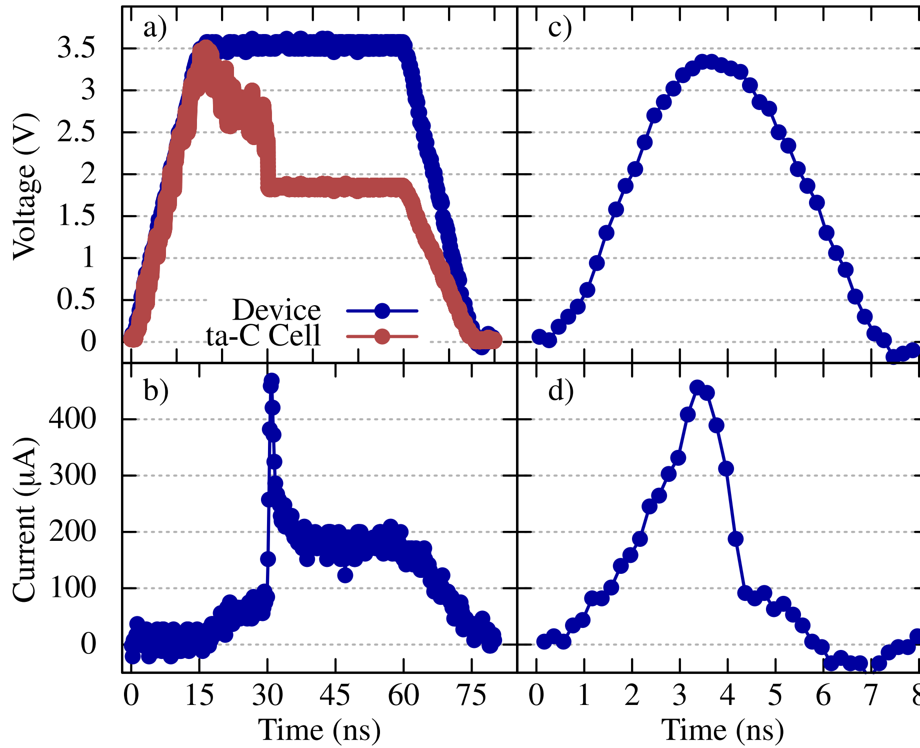


Figure 4.5: **a)** Applied voltage over a confined-cell device (100 nm diameter, 5 nm ta-C layer thickness) including the 13.4 kΩ R_{ser} (blue) and the voltage drop across the ta-C cell itself (red) for a typical SET pulse. **b)** Current response of the device during the switching process. **c)** RESET pulse and corresponding **d)** current during the reverse switching (RESET) process [modified from [47]].

adjusted to the voltage output timelines, which allows the direct comparison of the current response to the applied voltage.

The voltage in Figure 4.5a reached the plateau of the trapezoidal pulse after 15 ns, during which little or no increase in current occurred (Figure 4.5b). Then, the current increased to ≈80 μA before the dielectric breakdown set in after ≈30 ns. The dielectric breakdown was accompanied by a current spike (Figure 4.5b), after which the current stabilised and followed the voltage signal. This time lag between the voltage reaching its maximum and the onset of the dielectric breakdown indicates that the electric field alone, in the absence of sufficiently large currents, cannot initiate memory switching. The excess current at the

dielectric breakdown event is caused by a capacitive discharge.

The current in Figure 4.5d increased with increasing voltage (Figure 4.5c) until the RESET process 'kicks-in' after ≈3.6 ns, after which the current dropped significantly and eventually became too small to be sensed due to the high resistance of the device in the HRS (5.3 MΩ after reset).

These results show that the SET and RESET speeds of ta-C confined-cell devices fulfil the speed requirements for SCMs as depicted in Table 1.1 and are comparable to (or indeed better than) the switching speeds of other emerging storage technologies (see Section 1.5).

4.3 Data Retention

To explore the data retention capabilities of ta-C devices, confined-cell structures were switched from their HRS to their LRS and annealed at 85 °C for 10^4 s. To investigate the data retention capabilities of the HRS, ta-C confined-cell devices were switched into the LRS and back again into the HRS and annealed at 85 °C for 10^4 s. An exemplar set of results is shown in Figure 4.6. Here, a 100 nm diameter, 5 nm thick ta-C confined-cell device was SET from the HRS into the LRS using a SET pulse with an amplitude of 4.4 V and a duration of 60 ns. The series on-chip load resistor value was 13.4 kΩ. To investigate the HRS data retention capabilities, a RESET pulse with an amplitude of 4.1 V and a duration of ≈7 ns was applied to the (same) device to switch it back to its HRS. The resistance values of both states (LRS and HRS) fluctuated around their initial values of ≈10 kΩ (LRS) and 2 MΩ (HRS), thus maintaining an HRS/LRS ratio greater than two orders of magnitude. This good resistance contrast allows the distinction between the two stored logic states ('0' and '1') in ta-C confined-cell memory devices. The typical

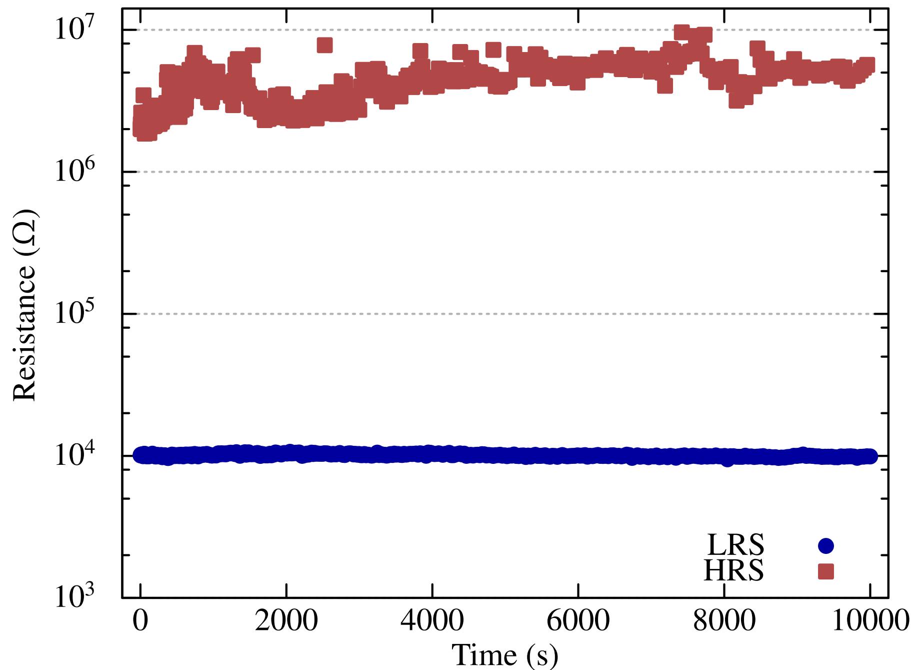


Figure 4.6: Data retention of LRS and HRS of a ta-C confined-cell, measured for 10^4 s at 85 °C [taken from [46]].

requirement for data retention in non-volatile memories, however, is 10 years at 85 °C (see Table 1.1). To take this into account a confined-cell device with a ta-C layer thickness of 5 nm was exemplarily RESET into the HRS (4.6 MΩ) at room temperature and then subsequently annealed from 170 °C to 270 °C in 20 °C steps, with the last annealing step carried out at 300 °C. The device was annealed for 1000 s at each temperature step before the temperature was increased. The resistance evolution is shown as a function of the annealing time in Figure 4.7. For better visualisation only the annealing steps carried out at temperatures of 170 °C, 230 °C and 300 °C are shown. The resistance of the confined-cell device decreased from room temperature (4.6 MΩ) to around 1 MΩ at 300 °C.

After the annealing experiments were carried out, the resistance of the confined-cell device was measured again at room temperature (≈18 MΩ). This obtained high resistance value of ≈18 MΩ indicates that the lower resistance values measured during the anneal-

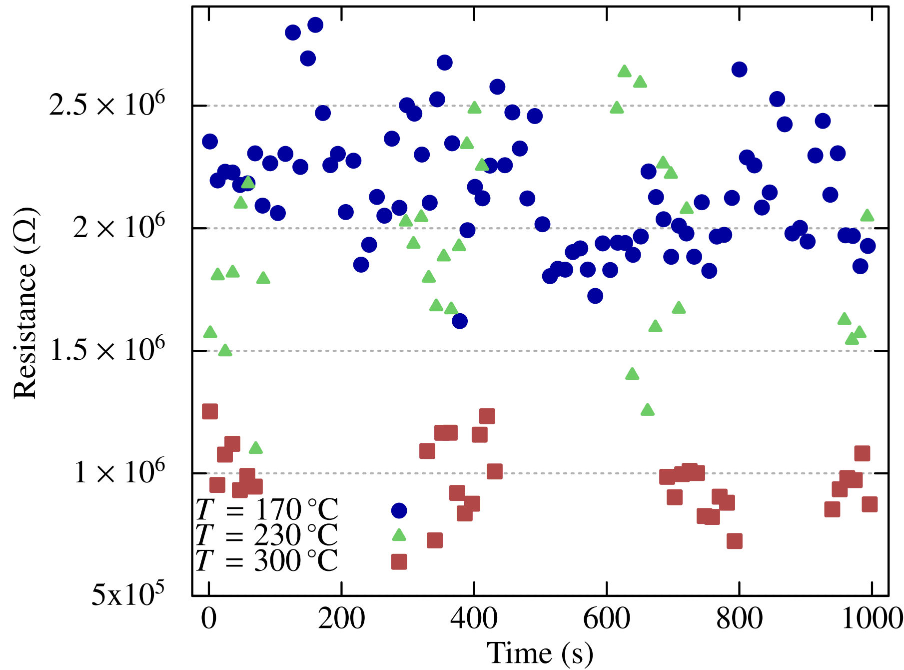


Figure 4.7: Data retention of a ta-C confined-cell, initially in the RESET state and annealed for 1000 s at 170 °C, 190 °C, 210 °C, 230 °C, 250 °C, 270 °C and 300 °C.

ing experiments can be attributed to the temperature dependence of ta-C conductivity (see Section 2.4.2) and not to an sp^3 to sp^2 conversion or to the formation/growth of sp^2 clusters (cf. [114]). In spite of the changes in resistance noted in Figure 4.7, the measured resistances remained well above typical resistances of the LRS (typically below 100 kΩ) during the entire annealing cycles, which makes devices based on ta-C potential candidates for high temperature re-writable memory applications.

ta-C devices might also be suited to write-once-read-many (WORM) applications, and so it is interesting to examine their high-temperature stability from a WORM context also. In a WORM application it is likely that the device would be SET from its pristine state to provide the two required memory states, so it is the temperature stability of the pristine state that is of most interest in this case (since the LRS configuration formed after a SET is the thermodynamically stable state). Thus, the resistance of a randomly

selected pristine confined-cell device with a 5 nm thick ta-C layer was measured at room temperature (17 MΩ), and then subsequently annealed in air at 200 °C, 300 °C, 350 °C, 450 °C, 500 °C, 550 °C and 600 °C. Each annealing step was carried out for 5 min. The resistance was measured at room temperature in all cases and is plotted as the ratio of R/R_0, with R_0 being the initial resistance of the confined-cell device, against the annealing temperature in Figure 4.8. The data is shown up to 550 °C, which is the highest annealing temperature at which the device remained functional. The resistance fluctuated around its initial value and dropped to around 1/10$^{\text{th}}$ of the initial value after annealing at 500 °C, and to 1/100$^{\text{th}}$ after annealing at 550 °C, which is the highest temperature at which the device remained functional. The observed resistance drops for annealing temperatures above 450 °C are in agreement with reports in [114]. Furthermore, this finding suggests that devices based on ta-C as the active material can be employed as WORM data storage devices in a high temperature environment. It has to be noted that it is not necessary to examine the evolution of the LRS at elevated temperatures as it is the thermodynamically stable state (see [114]).

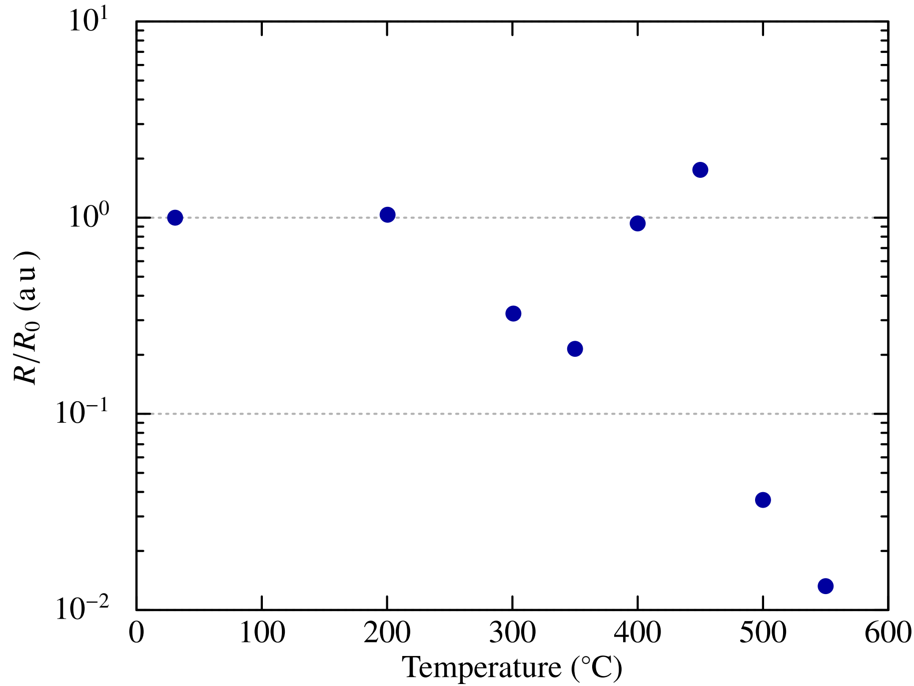


Figure 4.8: Variations of the ratio R/R_0 during annealing of a ta-C confined-cell device in air, with R_0 being the initial resistance of a pristine device.

4.4 Switching Endurance

Besides the already demonstrated high switching speeds, the very good scalability and data retention properties, a high switching endurance is required to use ta-C-based devices for non-volatile re-writable memory applications (see Section 1.1). To evaluate the potential of ta-C-based devices for resistive memory applications that require a high switching endurance, a slow quasi-static triangular pulse with 5 µs LE and TE edges was applied to switch confined-cell structures with a 5 nm thick ta-C layer from the pristine state into the LRS. Subsequently, the devices were cycled between the LRS and HRS using short electric pulses. This alternated switching between HRS and LRS is exemplarily shown in Figure 4.9, where a device was cycled more than 100 times between the LRS and HRS using 55 ns SET pulses and 8 ns RESET pulses [46]. It can be seen that the HRS and

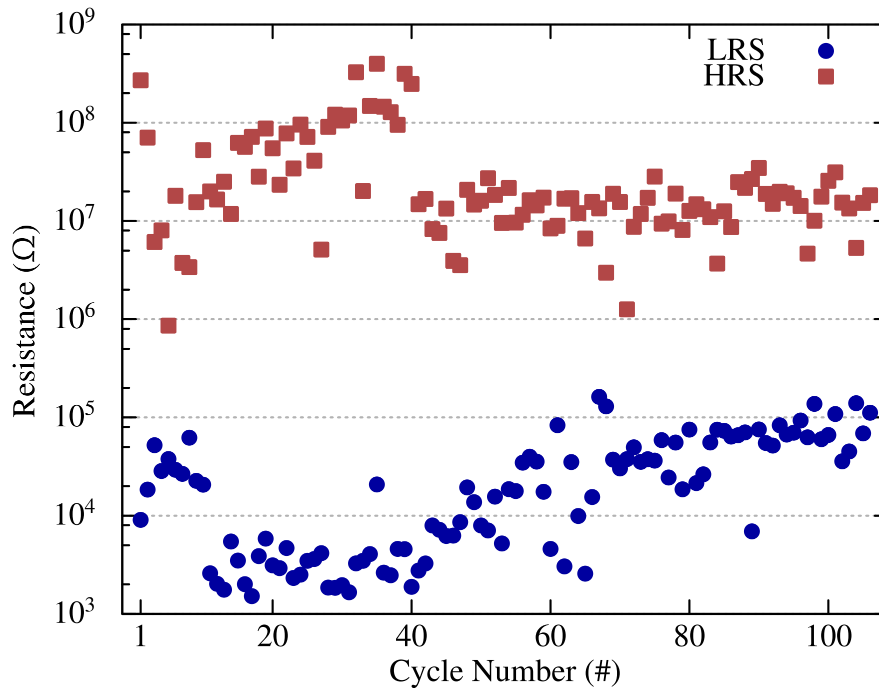


Figure 4.9: SET and RESET switching cycles in a confined-cell device with a 5 nm thick ta-C layer [taken from [46]].

LRS remained separated by at least an order of magnitude throughout the testing process. However, the resistance levels of the LRS drifted to higher values with increasing cycles, despite the fact that the set amplitudes (3.5 V) and pulse durations were not changed. To get more insights of the resistance evolution in the LRS, it is important to obtain a better understanding of the SET process and the LRS state, an aspect that is examined in more detail below.

4.5 LRS Characteristics

Field Dependence To explore the field dependence of the LRS, confined-cell structures were switched from their HRS to their LRS. The field dependence of the LRS was then determined by taking IV curves from 0 V to 0.35 V at temperatures of 85 K, 105 K,

120 K, 135 K, 160 K, 180 K, 200 K, 220 K, 240 K, 280 K, 300 K, 325 K and 350 K. An exemplar set of results is shown in Figure 4.10. Here, a 100 nm diameter, 5 nm thick ta-C confined-cell device was SET from the pristine state into the LRS using a quasi-static triangular SET pulse with an amplitude of 3.25 V and 5 µs LE and TE edges. The resistance in the LRS was measured to 27 kΩ (read out at 0.2 V). For better visualisation only the IV curves taken at temperatures of 85 K and 350 K are shown. It can be seen that the current increased non-linearly with the applied voltage, which indicates that the electronic transport in the LRS is not governed by a metal filament bridging the two electrodes, but is likely a consequence of the formation of one or several conductive carbon filaments as discussed in Sections 1.4 and 2.5. The symmetric current-voltage dependency suggests that the observed non-linear IV characteristic is not a contact limited conduction behaviour (cf. Section 5.2).

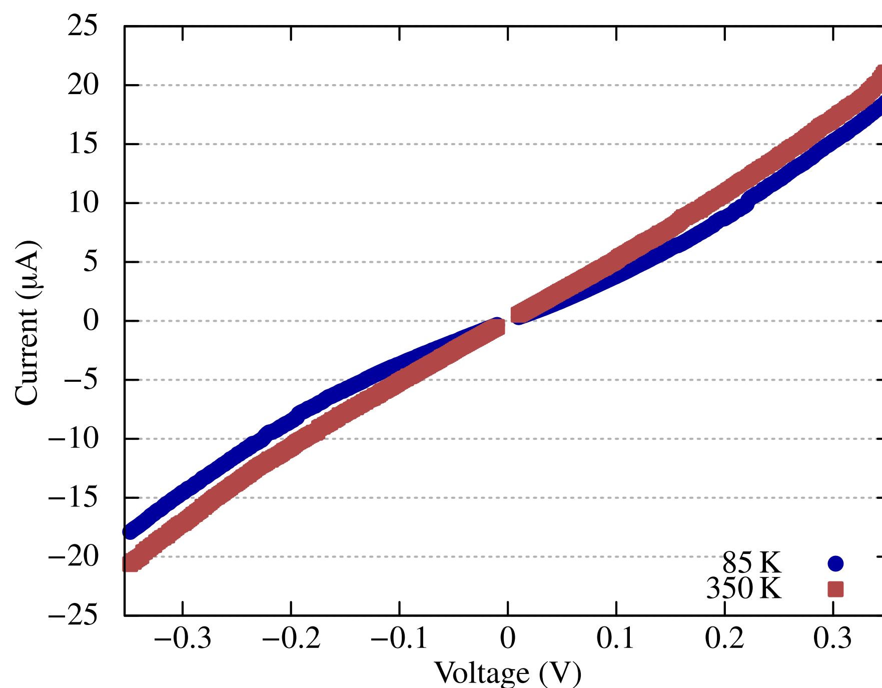


Figure 4.10: Current of the LRS of a confined-cell with 5 nm thick ta-C layer as function of the applied voltage for IV curves taken at 85 K and 350 K.

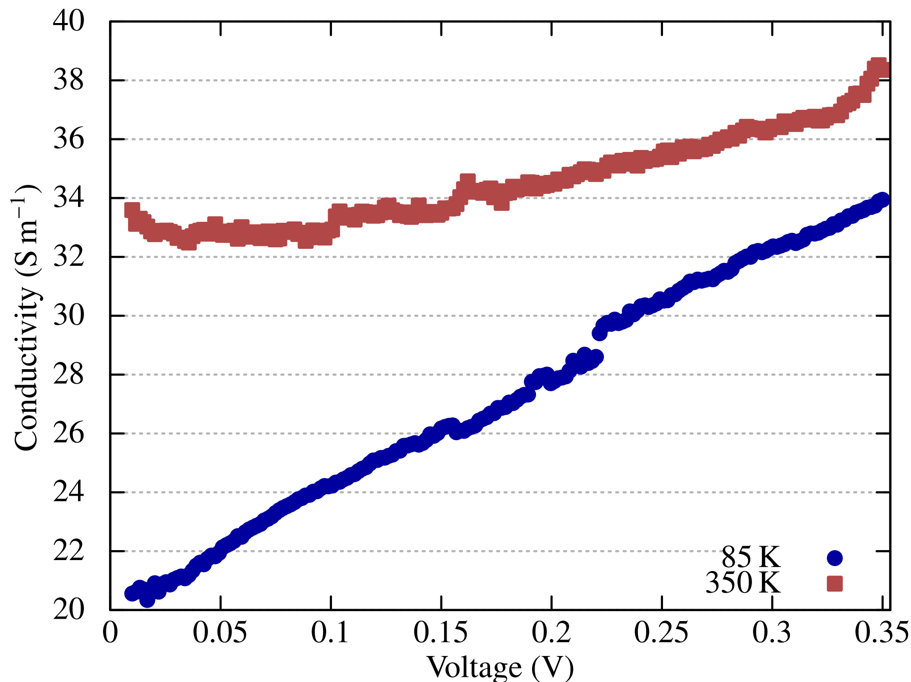


Figure 4.11: Conductivity of the LRS, calculated from the data of Figure 4.10, as function of the applied voltage for IV curves taken at 85 K and 350 K.

The non-linear dependence of the current on the applied voltage is also illustrated in Figure 4.11, where the conductivity is plotted as a function of the applied voltage. From Figure 4.11 it is clear that the conductivity increased as a function of the applied voltage. The increase is more pronounced at 85 K than 350 K, which is an indication for a temperature activated conduction behaviour (see equations 2.9 and 2.8). The observed non-linear increase of the conductivity with the applied voltage is important with respect to the reverse switching process, where large temperatures and temperature gradients are expected to play an important role in reverse switching (RESET) as discussed in Section 2.5.2.

Temperature Dependence To evaluate the temperature dependence of the LRS in more detail, low field data from the Ohmic regime of the IV measurements (cf. Figure 4.10) was examined. The conductivity is plotted in Figure 4.12 as a function of the temperatures at which the IV measurements were carried out.

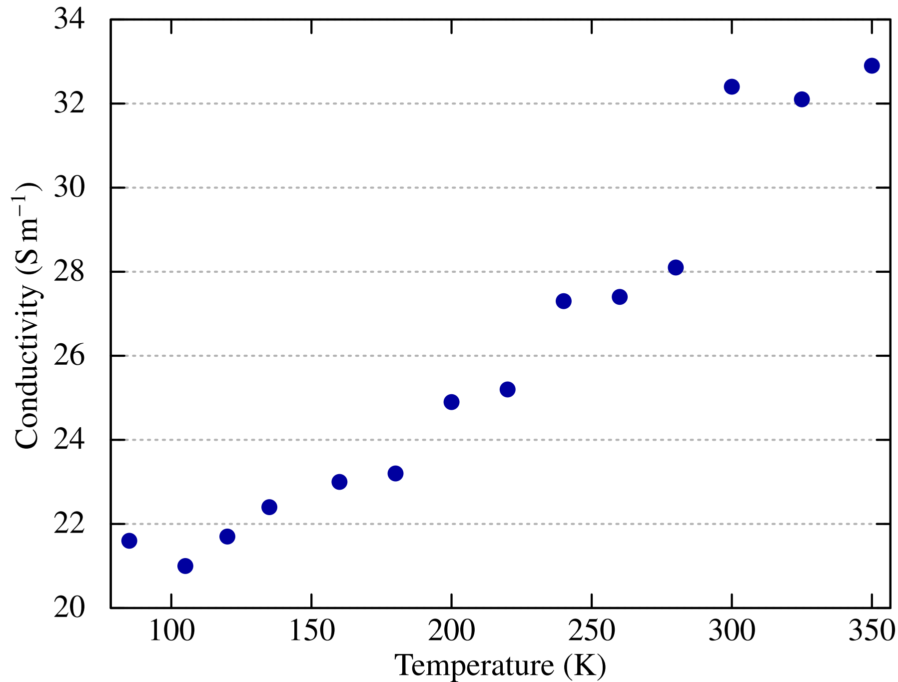


Figure 4.12: Conductivity of the LRS of a confined-cell device with a 5 nm thick ta-C layer. The measurement was taken in the Ohmic regime for temperature ranging from 85 K to 350 K (cf. Figure 4.10).

Generally, the conductivity increased with increasing temperature. This provides further evidence against a metal filament formation during the SET process, since the temperature coefficient of conductivity is typically negative in metals [128]. This result is important as it not only helps to rule out metal filamentation as a possible source of switching, but the occurrence of a positive temperature coefficient of resistance may contribute to large temperature gradients during the reverse switching process, and hence may play an important role in the reversible switching process in ta-C-based memory devices.

4.6 Elemental Analysis and Bonding Ratio

To investigate the influence of the switching process on the sp^2/sp^3 ratio two randomly selected confined-cell devices with 20 nm thick ta-C layers were switched from the pristine state into the LRS and the elemental distributions within the two ta-C cells (in the LRS) were analysed using energy-dispersive X-ray spectroscopy (EDX) and EELS (cf. Section 2.3) and then compared to the elemental distributions within a randomly selected pristine confined-cell device with the same ta-C layer thickness.

The first device (100 nm ta-C cell diameter) was SET into the LRS during an IV sweep up to 8 V, labelled as HARDSET in the following description. The on-chip current limiting load resistor during the SET process was 13.6 kΩ. The IV curve is shown in Figure 4.13, with the current plotted as function of the applied voltage (blue) and voltage drop across the ta-C cell (red).

Initially, most of the voltage in Figure 4.13 is dropped across the ta-C cell indicated by the overlap of the red and blue curve. At around 2 V the conductivity of the ta-C cell increased significantly and consequently, the voltage drop across the load resistor increased. At around 3.7 V (across the ta-C cell) the switching process 'kicked-in' and the device switched from the pristine state into the LRS, which was accompanied by a voltage snap back (red) due to the sudden increase of the ta-C conductivity.

The second device (50 nm ta-C cell diameter) was SET using a quasi-static triangular pulse with 5 µs LE and TE edges and an amplitude of 6.25 V, labelled as SET in the following. The on-chip current limiting load resistor during the SET process was 7.7 kΩ. The voltage applied across the device is plotted (blue) in Figure 4.14a together with the

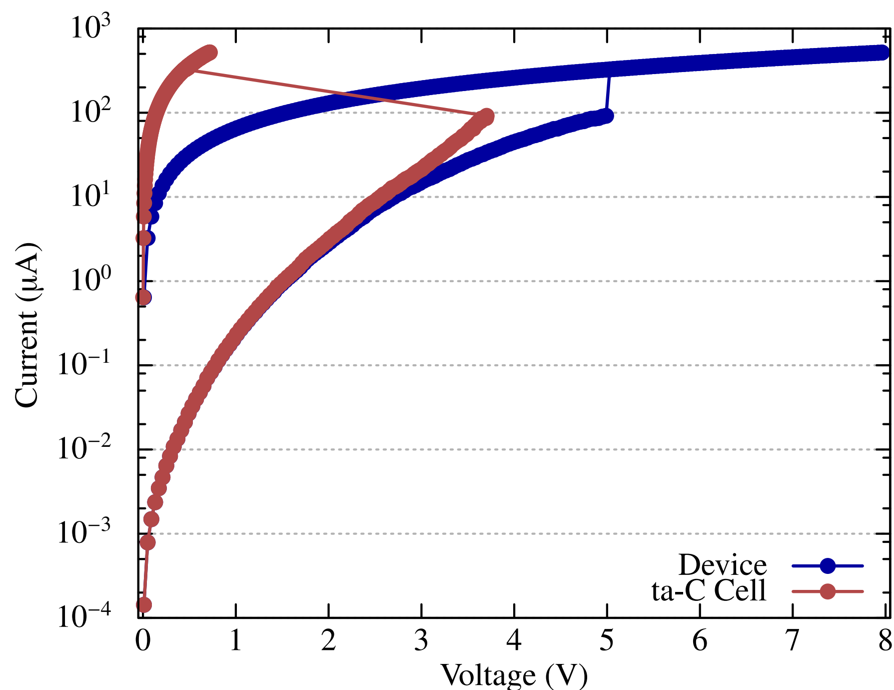


Figure 4.13: IV curve on a confined-cell device with a 20 nm thick ta-C layer.

voltage drop across the ta-C cell (red) and the corresponding current in Figure 4.14b. Similar as in the case of the HARDSET state, most of the voltage is dropped initially across the ta-C cell as indicated by the overlap between the red and blue curve in Figure 4.14a. At around 2.5 V the conductivity of the ta-C cell increased significantly and hence, the voltage drop across the load resistor increased. At around 4.2 V (across the ta-C cell) the switching process 'kicked-in' and the device switched from the pristine state into the LRS, which was accompanied by a voltage snap back (red) due to the sudden increase of the ta-C conductivity.

The above three devices in the HARDSET, SET and PRISTINE states were subsequently cross-sectioned and elemental analysis was performed. The analysis of the HARDSET and SET states was carried out using scanning transmission electron microscope (STEM), EDX and EELS. Since no switching was performed on the PRISTINE state only EELS was carried out to determine the sp^2/sp^3 ratio. The TEM related measurements were

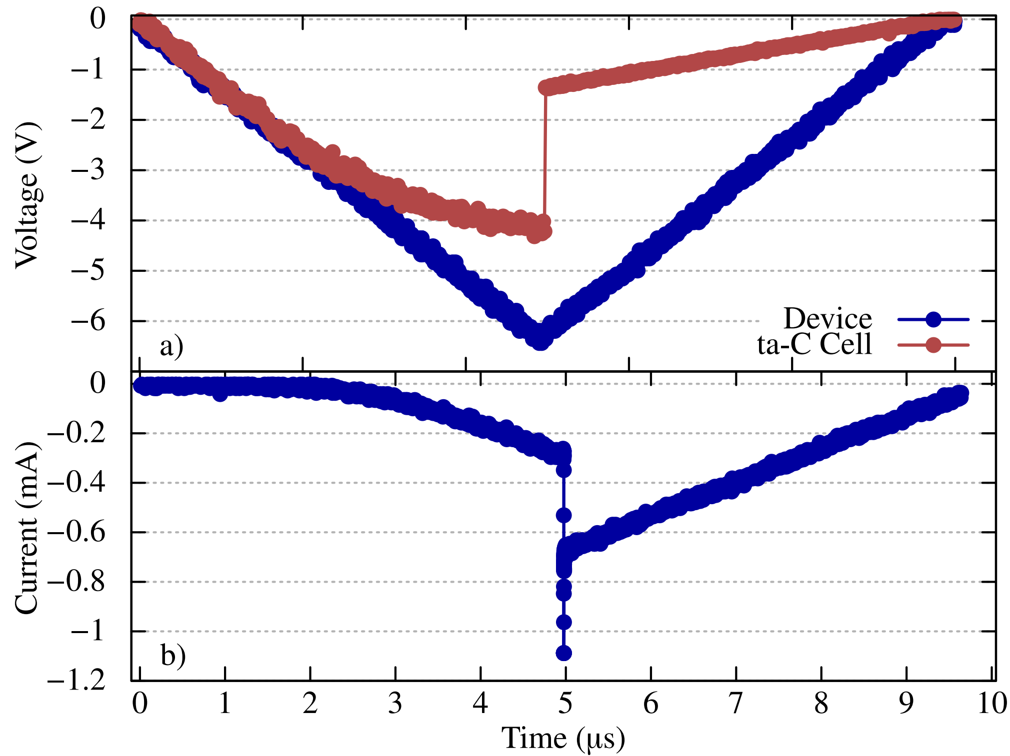


Figure 4.14: **a)** Slow forming pulse on a confined-cell device with a 20 nm ta-C layer using a voltage pulse with an amplitude of 6.25 V and a duration of 10 µs. **b)** Current response of the device including dielectric breakdown switching the device into the LRS.

carried out by Dr. O. Cojocaru-Mirédin at RWTH Aachen within the framework of the CareRAMM project. To get insights into the elemental distribution of the SET and HARDSET states and to rule out metal filamentation as a possible source of switching, TEM lamellae were prepared and inspected using high-angle annular dark field (HAADF) imaging. The elemental distribution was investigated using EDX. The HAADF image and the EDX image of the SET state is depicted in Figure 4.15a and of the HARDSET state in Figure 4.15b, respectively. The HAADF image shows the SiO_2 encapsulation was, during the sample preparation process, etched away together with parts of the Pt top electrode. The EDX chemical analysis showed a clear separation of Si, Pt and C in both cases (SET and HARDSET). This provides further evidence that no metal filament was formed during the SET processes.

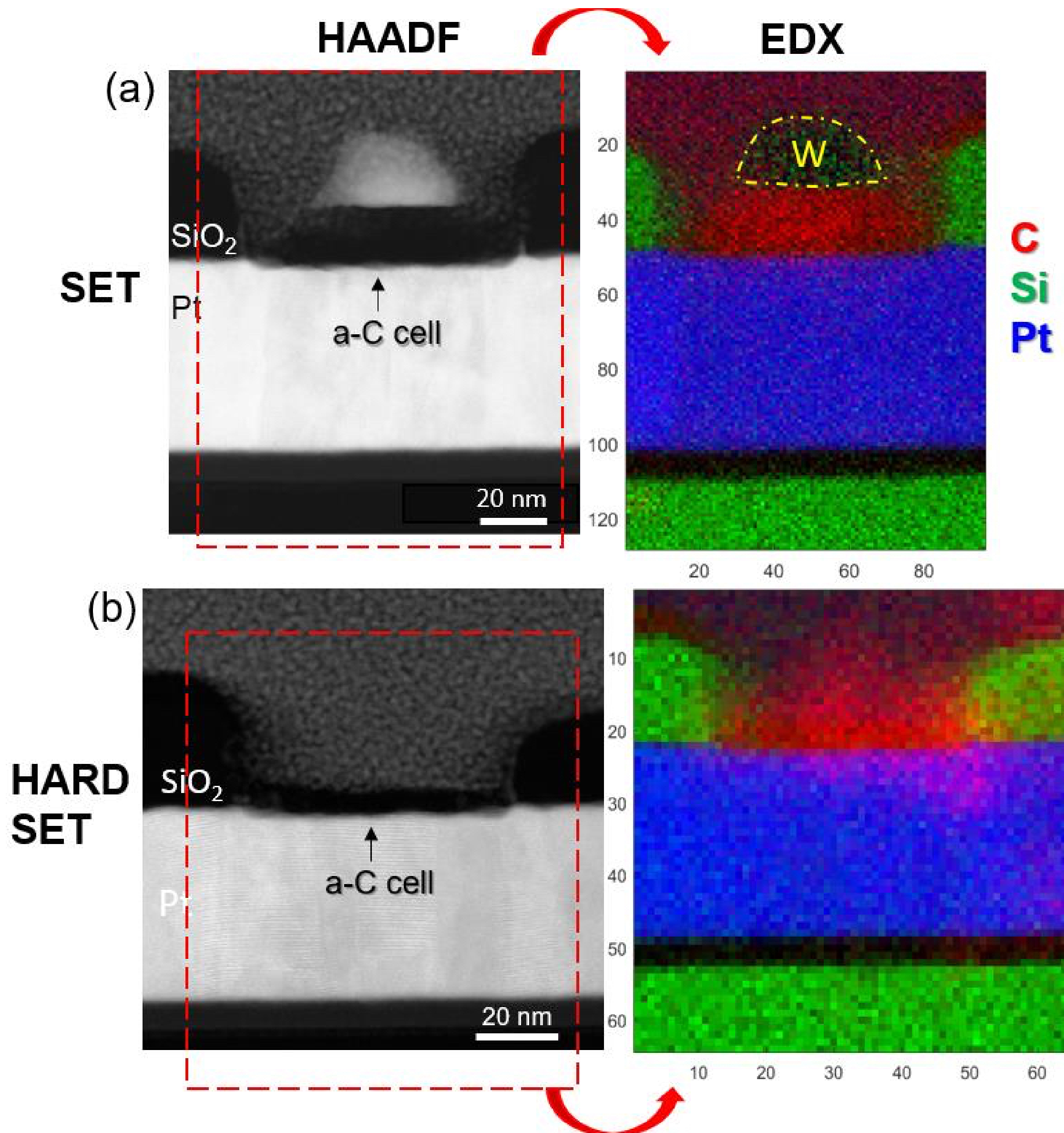


Figure 4.15: HAADF STEM images of cross-sections of confined-cells with 20 nm ta-C layers, and the corresponding EDX spectrum images from the same cells in **a)** SET state and **b)** HARDSET state showing the distribution of C, Si, and Pt elements.

To investigate the sp^2/sp^3 ratio, EELS analysis was performed to evaluate the π^*/σ^* ratio for the three devices PRISTINE, SET and HARDSET. The π^* orbitals are linked to sp^2 bonded carbon and the σ^* orbitals are linked to sp^2 and sp^3 bonded carbon (see Section 2.3). The intensity is plotted as function of the energy loss in Figure 4.16, for energies between 260 eV to 320 eV. The energies related to π^* could be located at 285 eV and the energies corresponding to σ^* can be located at 300 eV. Although the change of the π^*/σ^* ratio is not pronounced, it can be seen from Figure 4.16 that the π^*/σ^* ratio is highest for the HARDSET device, followed by the SET device and the PRISTINE device.

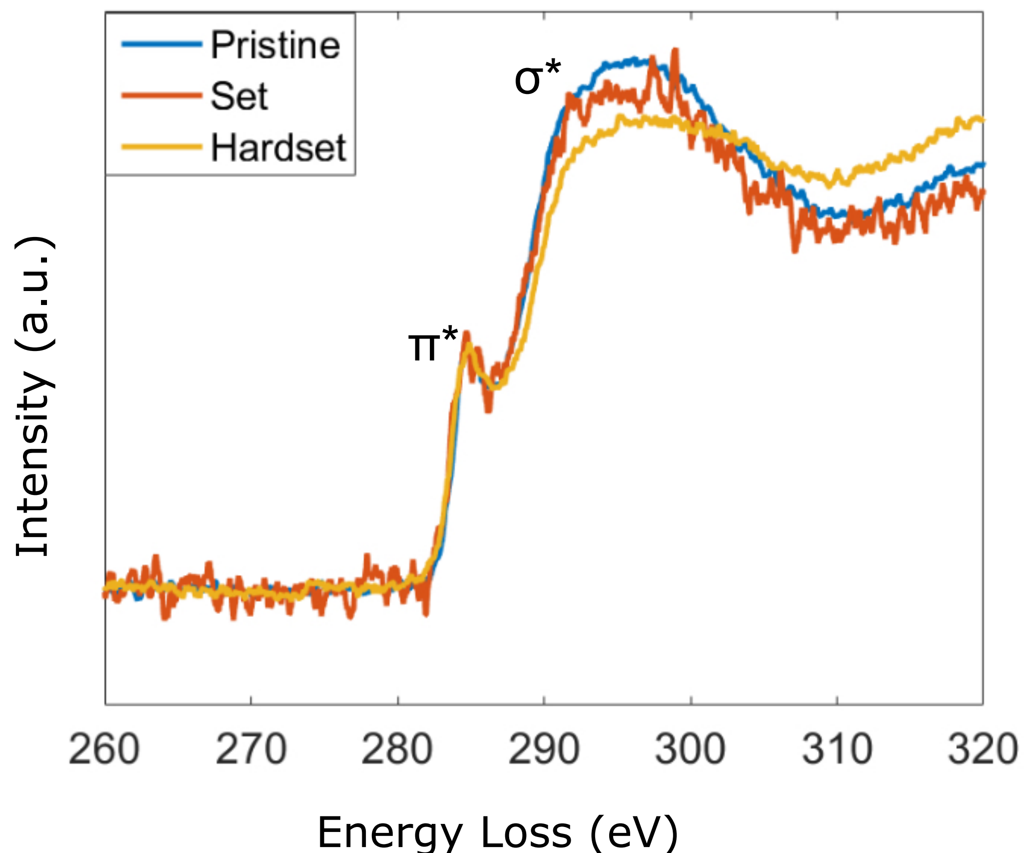


Figure 4.16: EELS spectra from 260 eV to 320 eV of PRISTINE, SET and HARDSET confined-cell devices with 20 nm thick ta-C layers.

Time Lag To investigate the stochasticity of the time lag between the applied voltage reaching its maximum and the onset of the dielectric breakdown (see Figure 3.9), randomly selected pristine confined-cell devices with ta-C layer thicknesses of 5 nm were initially SET into the LRS using quasi-static triangular pulses with 5 µs LE and TE edges. A (exemplarily selected) device was subsequently RESET and cycled using SET pulses with amplitudes of 3.5 V and pulse durations of 75 ns. Four SET voltages across the ta-C confined-cell device are exemplarily plotted in Figure 4.17a. The corresponding current responses are plotted in Figure 4.17b. The LRS resistances were 3.7 kΩ, 15 kΩ, 12 kΩ and 16 kΩ.

It can be seen from Figure 4.17 that the dielectric breakdown events occur at different times, and that there is no obvious correlation between SET pulses and observed time lag. This is expected since the electric field alone does not suffice to induce switching (see Sections 2.5, 4.1.1 and 4.2) and the local temperature distribution in the ta-C cell — at the onset of the dielectric breakdown — is caused by Joule heating (see Sections 2.5.1), which depends on the local current density (see equations 3.4 and 3.5). The local current density depends on the local atomic configuration of the HRS which is intrinsically stochastic [129]. These findings also suggest that in order to reduce the time lag and benefit from the fast switching speed of ta-C-based memory devices, higher voltages are required. Also it is noted that the stochasticity of the dielectric breakdown event could potentially be used as a hardware random number generator.

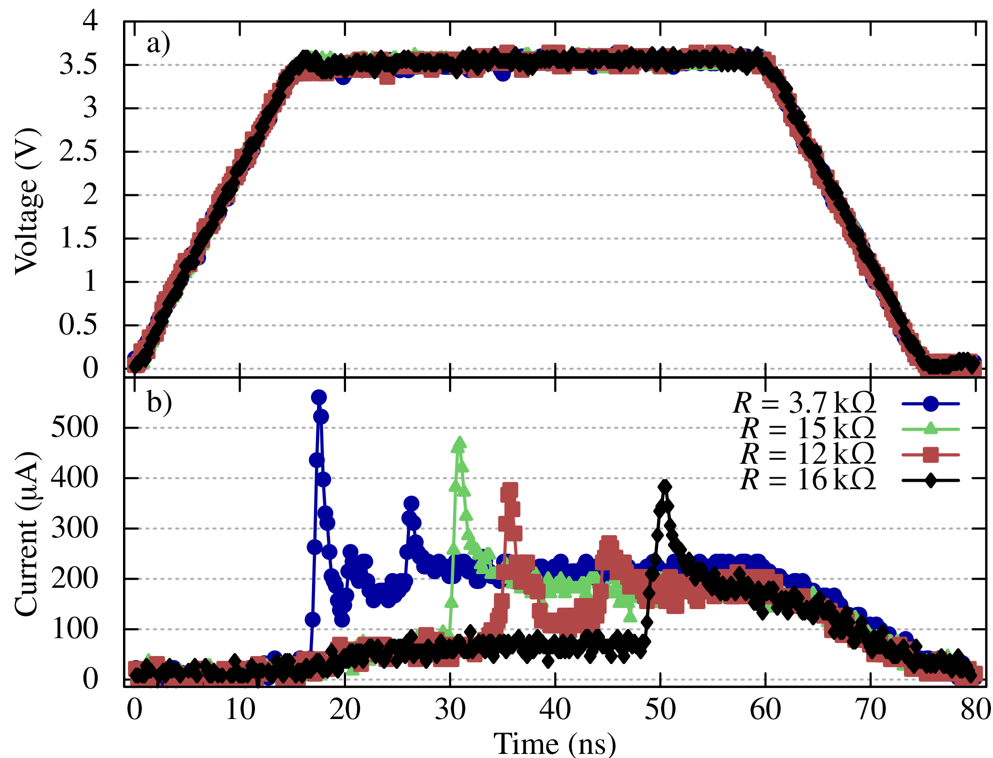


Figure 4.17: **a)** Four SET pulses with amplitudes of 3.5 V and durations of 75 ns used to switch a ta-C confined-cell device. **b)** Current responses of the device including the switching from the HRS into the LRS.

4.7 Switching Characteristics

Fast Switching Pulse To explore the switching speeds that might be achievable with ta-C devices, an exemplar pristine device (68 MΩ) with a 5 nm thick ta-C layer was switched into the LRS (1.3 kΩ) using a SET pulse with an amplitude of −4.1 V and a duration of 7 ns. The applied voltage across the device (blue) is plotted together with the voltage drop across the ta-C (red) cell in Figure 4.18a. The corresponding current response is plotted in Figure 4.18b.

The dielectric breakdown occurred after ≈5.0 ns, which is around 1.5 ns after the voltage pulse reached the maximum amplitude and represents a significant reduction of the time

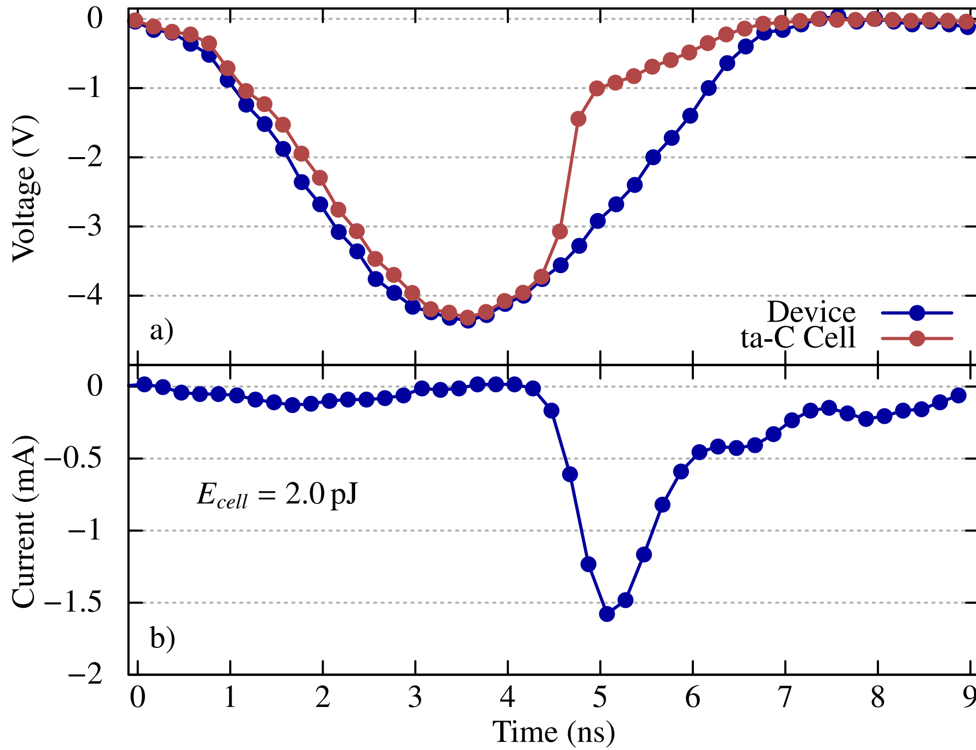


Figure 4.18: a) Fast forming pulse using a voltage pulse with an amplitude of −4.1 V and a duration of ≈7 ns. **b)** Current response of the ta-C confined-cell device including dielectric breakdown switching the device into the LRS.

lag in comparison to the SET pulses shown in Figure 4.17. The peak current was around −1.5 mA, which is high and is a consequence of the high voltage amplitude and the fact that no voltage drop occurred across the load resistor prior to the switching event. This is expected as the device was switched from the pristine state where no pre-formed conductive percolation path is present. The energy consumption E_{cell} was determined to be 2.0 pJ using equation 4.2 [122], where E is the energy, I the current, V the voltage and t is the time. The energy calculation is based on the voltage drop across the ta-C cell. This is significantly faster than the previously reported switching speeds of ta-C-based memory devices (see Table 2.2) and is around 50 times lower in energy than NAND flash cells and is comparable to (or better than) other emerging technologies (see Tables 1.1 and 1.2). Thus, the obtained switching speed and writing energy consumption of ta-C confined-cell

devices fulfil the requirements for SCM as denoted in Table 1.1. Further, as depicted in Figure 4.18, the device switched from the pristine state into the LRS in less than 1 ns, thus indicating that ta-C confined-cell devices have the potential to carry out sub-ns memory operations. This is in agreement with reports from MD simulations (see Section 2.5.1).

$$E = \int I \cdot V \, dt \tag{4.2}$$

Quasi-Static Switching Pulse Such high switching speeds (as demonstrated in Figure 4.18) come, however, at the cost of large currents and power requirements which may be acceptable for WORM applications, but limit the switching endurance in re-writable ta-C memories due to the formation of a large extended sp^2 network that is difficult to RESET [43, 46]. To reduce the switching current (and power), the time lag (see Figures 4.5a and 4.18) between the SET voltage pulse reaching its maximum amplitude and the onset of the dielectric breakdown should be minimal. To investigate the effects of a reduced time lag on the switching current, long quasi-static SET pulses were used to switch pristine devices into the LRS. Typical results are shown in Figure 4.19, for a randomly selected confined-cell device with a 5 nm thick ta-C layer. The device was switched from the pristine state into the LRS using a quasi-static triangular SET pulse with an amplitude of 3.5 V and a duration of 10 µs. The current limiting on-chip load resistor was 13.5 kΩ. For noise reduction a 200 MHz software filter is applied to the current and voltage signals during post-processing with the exception of the actual switching event.

Figure 4.19 shows that the current increased steadily until the dielectric breakdown 'kicked-in' after 4969 ns, which is before the voltage pulse reached the maximum amplitude. Further, the maximum current flow was ≈296 µA, which is a significant reduction in comparison to Figure 4.18. This decrease in current can be attributed to a lower parasitic capacitive discharge. The lower capacitive discharge can be attributed to the lower

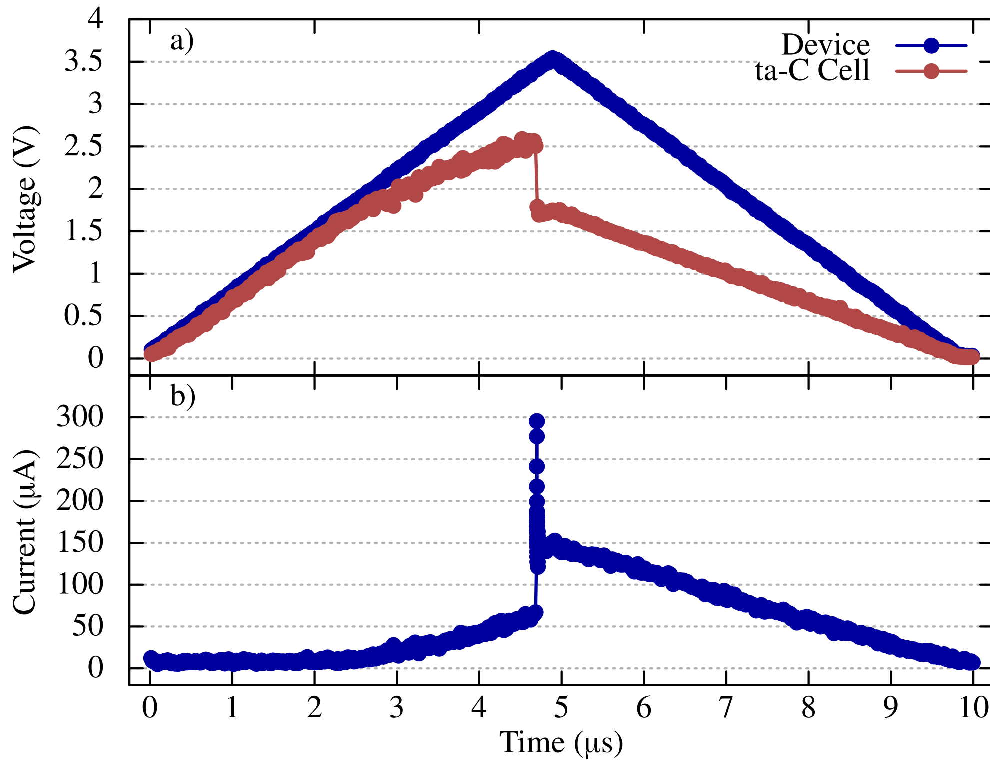


Figure 4.19: **a)** Slow forming pulse using a voltage pulse with an amplitude of 3.5 V and a duration of 10 µs. **b)** Current response of the device including the switching from the HRS into the LRS.

switching voltage that was required to SET the device (cf. Figure 4.18) and to the fact that some voltage dropped across the load resistor prior to the switching event. The observed increase in conductivity could be explained by a temperature dependence of the conductivity (see Section 2.4.2), which in turn increased the conductivity in a runaway process, ultimately triggering a temperature activated process leading to material modifications during the switching event. Such a thermal runaway process is studied in more detail in Sections 5.2, 5.3 and 5.4. To optimise cyclic endurance (see Figure 4.9) it was found essential during the work of this thesis to use long, quasi-static SET pulses to switch pristine confined-cell devices into the LRS (see Figure 3.9).

4.8 Summary & Conclusion

In this chapter, it has been demonstrated that ta-C confined-cell devices can be operated in unipolar (and bipolar) operational mode and switched from the HRS into the LRS (and vice versa) below 10 ns, which represents an improvement of the SET speed by a factor of 5 in comparison to previous studies (see Table 2.2). Reversible switching was shown on a ta-C confined-cell device with a 5 nm thick ta-C layer for more than 100 cycles. This is — to the best of knowledge — the thinnest ta-C layer reported to show memory switching, where solely ta-C was used as the active memory material. The reverse switching speed from the LRS into the HRS was observed to be well below 8 ns, which is significantly faster than in previous reports (cf. Table 2.2). In agreement with the literature it was shown that the actual switching process from the pristine state into the LRS (i.e. the dielectric breakdown event) takes place on a sub-ns time scale.

The tested ta-C confined-cell devices kept their initial resistance value up to a temperature of 450 °C for 5 min and remained fully functional, i.e. read out of the resistance state was possible, after an annealing step at 550 °C for 5 min. This is — to the best of knowledge — the highest reported temperature for any ta-C-based memory device and shows that ta-C confined-cell devices are suitable candidates for high temperature WORM applications.

For the application as re-writable SCM type formats, cyclic endurance has to be improved. In agreement with literature it was found that a reduction of the current which is required to switch the ta-C devices from the pristine state into the LRS, is paramount to achieve a high cyclic endurance. In agreement with literature it was found on ta-C cross-bar structures that the switching current is reduced for ta-C devices with higher sp^3 contents. It was shown that the switching voltages (and currents) can be reduced by using long, quasi-static SET pulses to switch ta-C confined cell devices from the pristine state into the LRS.

Further, it was shown that the switching voltages (and currents) to SET pristine devices into the LRS are lower for confined-cell devices with a thinner ta-C layer. It was found that the reduction of the lateral dimensions (i.e. area) of ta-C cross-bar structures helped to increase the switching performance in terms of reduced energy and power consumptions.

Evidence was also shown that the switching from the HRS into the LRS is likely caused by the formation of a conductive sp^2-rich carbon filament. The absence of scaling between switching voltage (and current) with the ta-C area in ta-C cross-bar structures ruled out interfacial switching as cause for the resistance contrast between HRS and LRS. Further, no electrode metal oxide layer was found in pristine devices using HAADF, EDX and EELS analysis techniques. Further, it was shown for the first time — to the best of knowledge — on ta-C memory devices that not only the HRS, but also the LRS is field- and temperature-dependent. The positive temperature coefficient of resistance of the LRS allowed the exclusion of metal filamentation (originating from the metal electrodes) as a possible source of switching from the HRS into the LRS. Additionally, no evidence of the presence of metal atoms was found in the LRS using HAADF, EDX and EELS analysis techniques.

Additionally, it was shown that the time lag between the voltage reaching its maximum and the onset of the dielectric breakdown indicates that the electric field alone, in the absence of sufficiently large currents, cannot initiate switching from the HRS into the LRS in ta-C memory devices.

Chapter 5

Joule Heating Effects in ta-C Devices

Partial results of the presented work in this chapter have been published in:

- ”Joule Heating Effects in Nanoscale Carbon-based Memory Devices,” in 2016 *IEEE Nanotechnology Materials and Devices Conference (NMDC).*, pp. 1–2, IEEE, 2016. *DOI: 10.1109/NMDC.2016.7777081*

- ”Temperature Evolution in Nanoscale Carbon-Based Memory Devices due to Local Joule Heating,” in 2017 *IEEE Transactions on Nanotechnology.* IEEE, 2017. *DOI: 10.1109/TNANO.2017.2674303*

A key challenge for amorphous carbon-based memory is cyclic endurance, as discussed in Sections 2.5 and 4.4. To improve the cyclic endurance it is necessary to get a better understanding of the conditions at the onset of the dielectric breakdown. A computational model was therefore developed to help shine light on the conditions at dielectric breakdown, especially the temperature distribution due to the Joule heating effect. In the first part of this chapter, the role of Joule heating and the resulting temperature distributions at the onset of memory switching are investigated on the basis of the experimental data presented in Chapter 4. The experimental data is then compared with computational modelling results. The second part of this chapter has the aim to provide a guideline

for the optimisation of ta-C confined-cell devices with respect to achieving higher cyclic endurances.

5.1 Temperature-Dependent Conductivity

To get insights into the conditions at the onset of dielectric breakdown, it is necessary to study both the field- and the temperature dependence of the electrical conductivity separately. The temperature dependence of pristine confined-cell devices with 5 nm thick ta-C layers was determined by measuring IV curves for temperatures from 85 K to 300 K at low electrical fields. At low electrical fields, electronic transport in amorphous carbon is reported to be mainly governed by variable-range-hopping in localised states (see Sections 2.4.2 and 2.4.3) [92–95]. The conductivity in localised states typically follows a power law and is, here, plotted against $T^{-1/4}$ in Figure 5.1 for the Ohmic regime (identified using the measured IV curves for temperatures from 85 K to 300 K). Each data point was obtained from a fit of the Ohmic region at the corresponding temperature (cf. Figure 5.2 for 300 K).

This type of conductivity behaviour describes VRH as introduced by Mott (see equation 5.1) [96].

$$\sigma_{00} = \sigma_0 \cdot \exp\left(-\left[\frac{T_0}{T}\right]^{1/4}\right) \tag{5.1}$$

The conductivity is denoted as σ_{00} and σ_0 and T_0 were fitted to the data shown in Figure 5.1 and have the values 0.345 S m^{-1} and 220 K. The linear dependence over the whole temperature range confirms that electrical transport in the ta-C confined cell devices examined here is governed by hopping between localised states [88, 89, 96].

It has however to be noted that the range of applicability of the Mott law is still a matter of

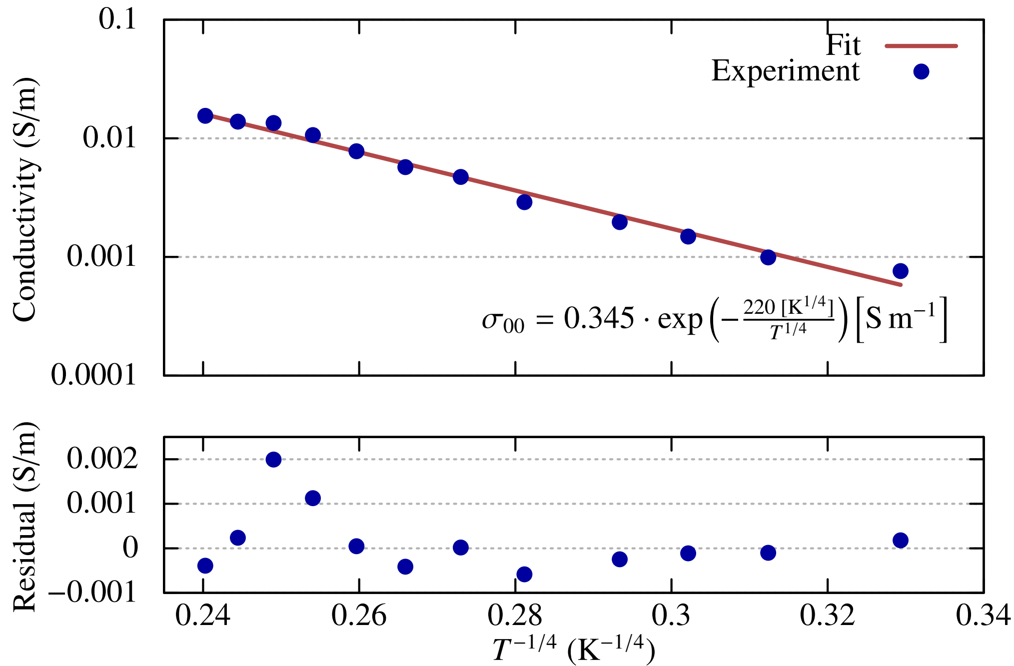


Figure 5.1: Conductivity of a pristine carbon memory device measured at low voltages from 85 K to 300 K [taken from [8]].

debate [98, 99, 130]. The main criticism, as pointed out by Marshall et al. [99], originates from the fact that equation 5.1 was derived by setting the dominant hopping distance of localised charge carriers equal to the maximum hopping distance within a spherical volume that contains one (localised) charge carrier at its centre. This assumes that defects are equally distributed and ignores spatially closer empty jumping sites and hence, does not take different jumping probabilities for different jumping distances into account [99]. However, in the work of this thesis equation 5.1 is only used — together with the field-dependent part of the conductivity — with the aim to reproduce the experimentally determined conductivity prior to dielectric breakdown. A more in-depth discussion of VRH can be found in [86, 95, 98, 99, 101, 102, 131].

5.2 Electric Field-Dependent Conductivity

The field-dependent part of the conductivity was determined at room temperature with the aim of developing a computational model that is capable of describing the experimentally obtained conductivity in ta-C confined-cell memory devices (see Chapter 4 and Section 5.3) over the range from Ohmic conduction until the onset of the dielectric breakdown. To determine the field-dependent part of the conductivity of ta-C confined-cell devices, and to distinguish it from the Ohmic conduction, IV curves were taken up to a maximum of 0.8 V. In Figure 5.1 the Ohmic part of the conductivity of a randomly selected ta-C confined-cell device is shown, and the field-dependent part of the conductivity of the same device is shown in Figure 5.2 for the whole IV curve taken at room temperature.

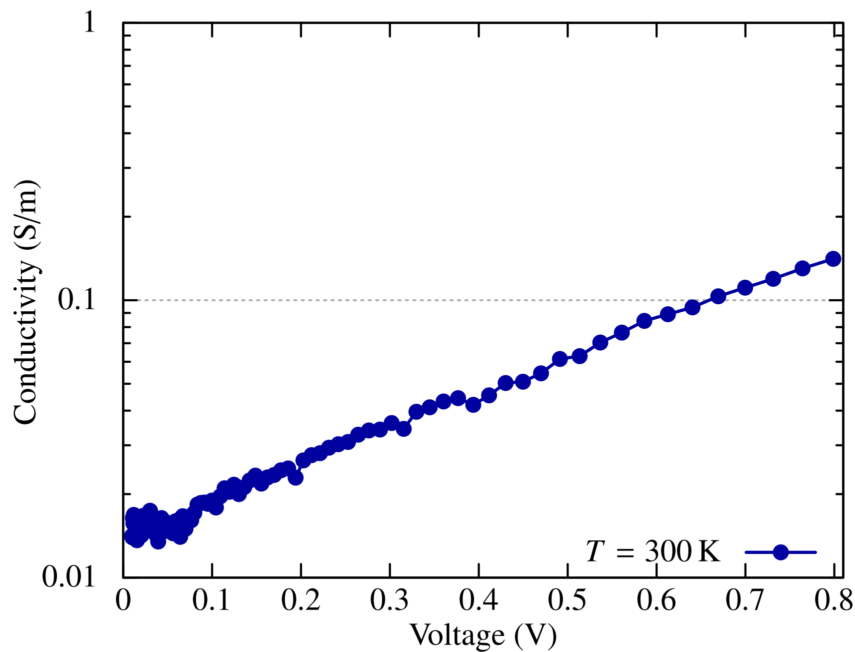


Figure 5.2: Field-dependence of the conductivity of a carbon memory device measured at 300 K.

From Figure 5.2 it can be seen that initially, the conductivity remained constant until ≈0.1 V, where the transition from Ohmic to field-dependent conduction took place. To exclude noise as the origin for the observed constant conductivity at low electrical fields, the same experimental data is plotted in Figure 5.3 and shows that the data is well above the system noise floor even for low applied voltages.

From then on, the conductivity increased exponentially with the applied voltage, which is in agreement with a Poole-type conduction behaviour [106]. A Poole-type conduction behaviour is also in agreement with reports of a high defect density in ta-C [65].

With the assumption of a Poole-type conduction, the transition from Ohmic conduction to the field-dependent conduction can be described using equation 5.2 [21, 104, 132].

$$I = A \cdot \sinh\left(\frac{eV_a s}{2k_B T t}\right) \tag{5.2}$$

The current is denoted as I, A is a fitting constant, e is the elementary charge, k_B the Boltzmann constant, T the temperature (*here* 300 K), t the thickness (*here* 5 nm) and s is a fitting constant that describes the dominating distance between Coulomb (i.e. trap) centres as defined in [21].

The applied voltages, during taking of the IV curve used to generate Figure 5.2, were low enough (<0.8 V) to keep the Joule heating small (below 1 K). Thus the temperature was set constant to 300 K (note that the temperature evolution in the ta-C cell as function of the applied voltage was verified a posteriori with simulation results presented in Section 5.4) and the experimental IV curve fitted to the Poole model for the range of voltages from 0.1 V to 0.8 V, as shown in Figure 5.3. The fit can be seen to be good.

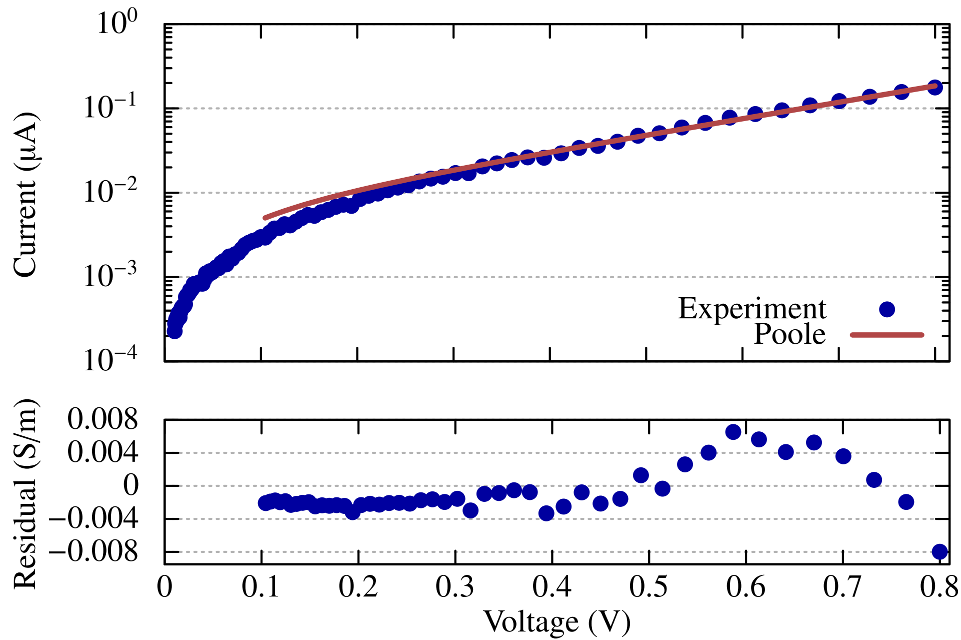


Figure 5.3: Fit of the field-dependent part of the conductivity of a ta-C confined-cell device using equation 5.2.

For applied voltages below 0.1 V, VRH was chosen to describe the low-field conduction of the tested ta-C confined- cell devices, as shown in Figure 5.1 and discussed in Sections 2.4.2 and 5.1.

Accordingly, the low field conduction of ta-C confined-cell devices was implemented in the computational model using VRH, and the field-dependent part of the conductivity was implemented using a Poole-type conduction model. The most important parameters used in the simulation of ta-C (and a-CO_x) confined-cell devices are provided in Table 3.4.

To exclude a metal-insulator junction as a possible alternative to explain the obtained IV data, the Schottky emission process is briefly reviewed in the following.

Schottky-Barrier The Schottky emission process is based on an energy barrier at a metal-insulator interface [133, 134]. In the case of an insulator, the energy barrier ϕ_B is much larger than the thermal energy $k_B T$. This allows a description of the energy barrier ϕ_{B0} and the observed lowering due to the electric field F as [128]:

$$\phi_B = \phi_{B0} - \sqrt{\frac{eF}{4\pi\epsilon\epsilon_0}} \tag{5.3}$$

The elementary charge is denoted as e, with ϵ and ϵ_0 being the relative permittivity and vacuum permittivity, respectively. Furthermore, since the mean free path of electrons in amorphous solids is typically short [135], the diffusion theory of metal-semiconductor rectification is typically used to describe the Schottky emission [21, 136]. The current density is thus given in equation 5.4, using the Einstein relation $D_n = k_B T \mu_n / e$ [128]:

$$j_n \approx e\mu n N_C F \exp\left(-\frac{e\phi_B}{k_B T}\right)\left[\exp\left(\frac{eV_a}{k_B T}\right) - 1\right] \tag{5.4}$$

where the DOS close to the interface is N_C, the free carrier mobility μ_n and the applied voltage V.

As a consequence of the use of two different electrode materials in the ta-C confined-cell devices (W and Pt) and their different potential barriers, equation 5.4 predicts a strong increase in current density when the ta-C devices are biased in a forward direction and a significantly smaller increase in reverse direction. However, this behaviour was never observed for the ta-C devices examined here, as they can be operated in a unipolar manner in both directions, as discussed in Section 2.5. For example, the current is plotted as function of the applied voltage for a randomly selected pristine confined-cell device with a 5 nm thick ta-C layer in Figure 5.4 for an IV curve taken from −0.3 V to 0.3 V. It can be seen that the current increase was symmetric, polarity independent, and solely a function of the amplitude of the applied voltage. In addition, as shown in Figure 4.17, the ta-C

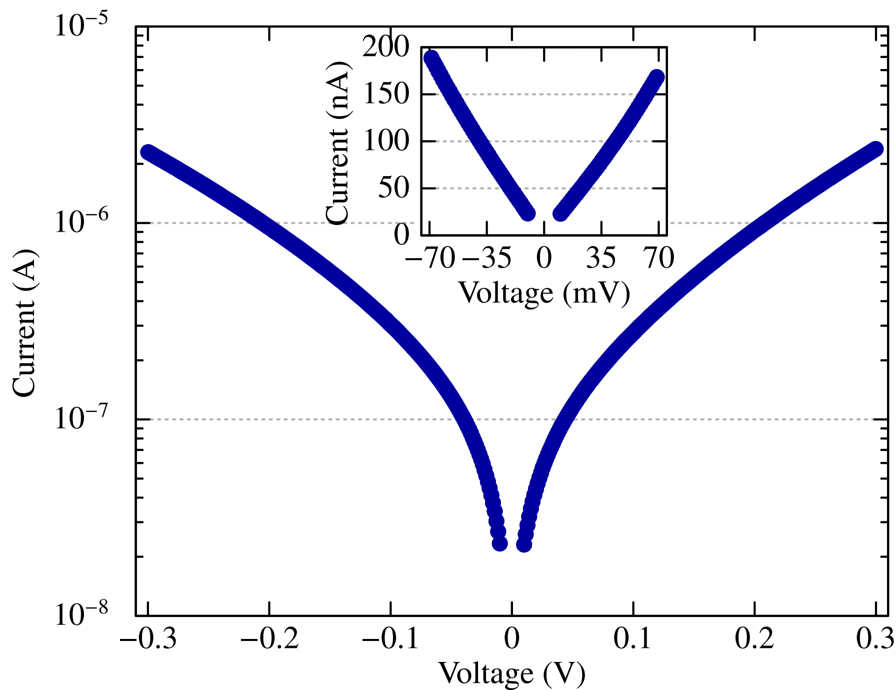


Figure 5.4: Current as function of the applied voltage for a randomly selected pristine confined-cell device with a 5 nm thick ta-C layer (inset shows the IV curve on linear scales).

devices have an almost linear current-voltage dependence after switching, indicating an Ohmic contact at the electrode-(t)a-C interface. Thus, Schottky emission can be ruled out as a significant contributor to the electrical transport properties of the ta-C devices examined here.

5.3 Model Validation

Isothermal Field-Dependent Conductivity To validate the computational model introduced in Section 3.2.2, the simulated conductivity of confined-cell devices with 5 nm thick ta-C layers was matched to the experimental results for low- and intermediate electric fields, prior to the onset of Joule heating. This was done with the aim to obtain a realistic conductivity of confined-cell devices with 5 nm thick ta-C layers, which were

extensively investigated in the work of this thesis. It is important to reproduce the experimentally obtained conductivity using the computational model in order to gain insights into the temperature distribution at the onset of the dielectric breakdown, where Joule heating is expected to play an important role (see Sections 2.5.1 and 4.6). The most important material properties used in the simulation of the confined-cell devices with 5 nm ta-C layers are provided in Table 3.4. To obtain the temperature distribution in the ta-C cell, a finite element software package (COMSOL®) was used to solve the coupled heat and Laplace equations (see equations 3.2 and 3.3). More details regarding the electro-thermal model are provided in Section 3.2.1.

To justify the isothermal approach that was used to determine the conductivity for the computational model at low- and intermediate electric fields (see Figures 5.2 and 5.3) a posteriori, the simulated maximum temperature within the ta-C cell is plotted as a function of the applied voltage in Figure 5.5. The temperature increase remained <1 K within the fitted voltage range of Figure 5.3, thus justifying the assumption of a constant temperature at low voltages.

The simulated conductivity is compared with experimental data in Figure 5.6. The simulation (red) described the isothermal part of the conductivity (blue) very well up to electric fields of around 2×10^8 V m^{-1} ($|V| = 1$ V).

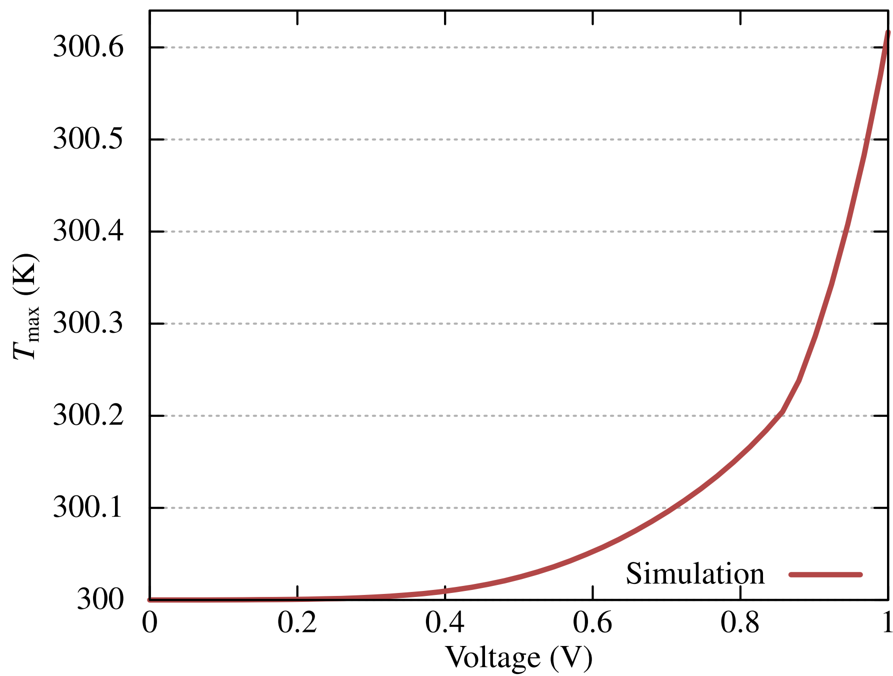


Figure 5.5: Local temperature evolution in a ta-C confined-cell device as function of the applied voltage [adapted from [47]].

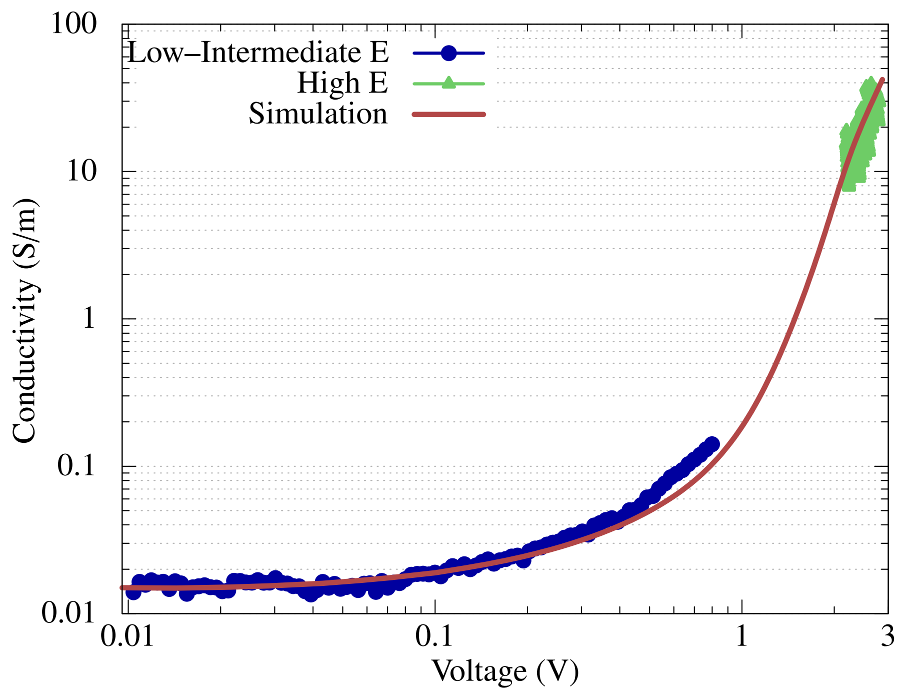


Figure 5.6: Measured and simulated conductivity of a ta-C confined-cell device as function of the absolute value of the applied voltage [taken from [47]].

Joule Heating Effects at Dielectric Breakdown To validate the computational model (see Section 3.2.2) at high electric fields and to investigate Joule heating effects at the onset of dielectric breakdown, a randomly selected confined-cell device with a 5 nm thick ta-C layer was experimentally switched from the pristine state into the LRS using a quasi-static triangular switching pulse with an amplitude of −3.5 V and 5 µs leading and trailing edges. To increase the computational speed, a device with the smallest available ta-C confined-cell diameter of 50 nm (see Section 3.1.1) was used in both experiment and simulation. A quasi-static pulse was chosen to exclude any time lag between the applied voltage and the onset of the dielectric breakdown (cf. Figure 4.19). For both experiment and simulation a 13.3 kΩ load resistor was used. The applied voltage across the device (blue) is plotted together with the voltage drop across the ta-C (red) cell in Figure 5.7a. For noise reduction a 200 MHz software filter was applied to the current and voltage signals of the quasi-static SET pulse in Figure 5.7 during post-processing. The corresponding current response is plotted in Figure 5.7b. The current always followed the voltage pulse until dielectric breakdown occurred after 4.4 µs and hence, no time lag was observed.

Note that the oscilloscope was programmed to ensure to proper capture of the currents present at dielectric breakdown and, as a consequence, was insensitive to low currents at low voltages. Therefore, the experimental data originating from the quasi-static pulse in Figure 5.7a is shown in Figure 5.6 only for voltages from $|V| = 2.2$ V until the onset of the dielectric breakdown (i.e. $|V| = 2.7$ V). There, the simulated conductivity (using COMSOL®) is compared with experimental data for the entire conductivity range prior to dielectric breakdown. The simulation (red) reproduced the isothermal part of the conductivity (blue) and the field-dependent part (green) very well.

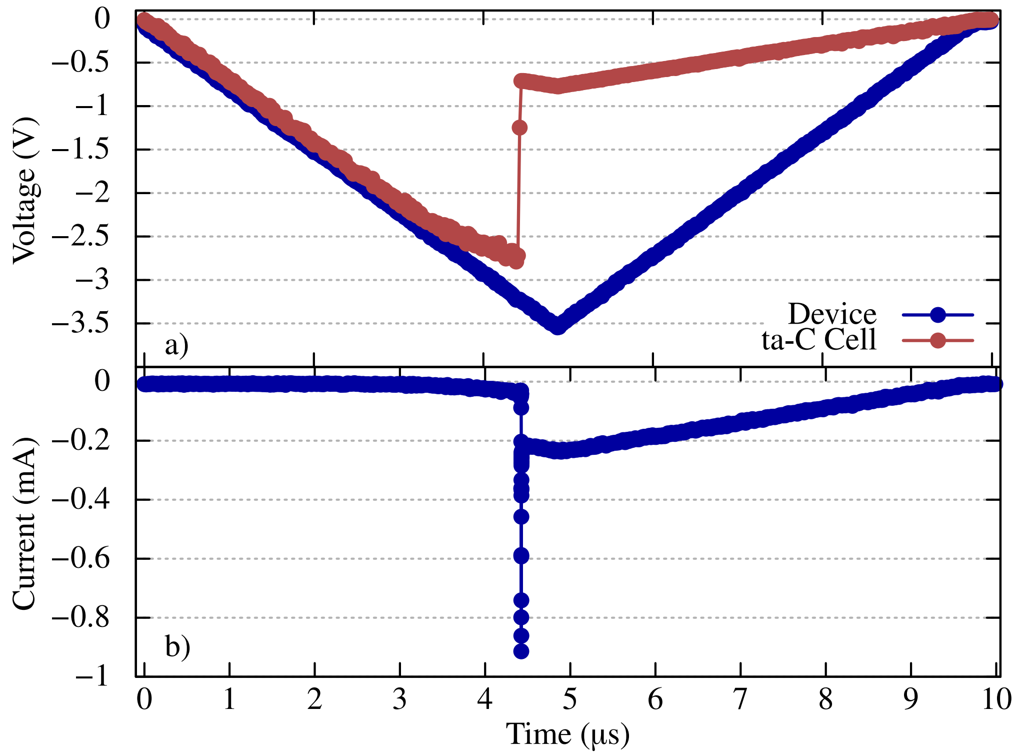


Figure 5.7: a) Quasi-static SET pulse on a confined-cell device with a 5 nm ta-C layer using a voltage pulse with an amplitude of −3.5 V and a duration of 10 µs. **b)** Current response of the device including dielectric breakdown switching the device into the LRS.

5.4 Temperature Distribution at Dielectric Breakdown

The very good agreement between simulated and experimentally determined conductivity, as shown in Figure 5.6, indicates that the computational model can be used with confidence to investigate the local temperature distribution on the device-scale using realistic switching pulses. The temperature increase due to Joule heating is calculated by solving the coupled heat and Laplace equations (see equation 3.5) using (COMSOL®). The temperature distribution within the ta-C confined-cell using the quasi-static SET pulse shown in Figure 5.7 is thus as presented in Figure 5.8 (for 4.4 µs into the SET pulse). The applied voltage (blue) at the onset of the dielectric breakdown was 3.15 V and the voltage drop

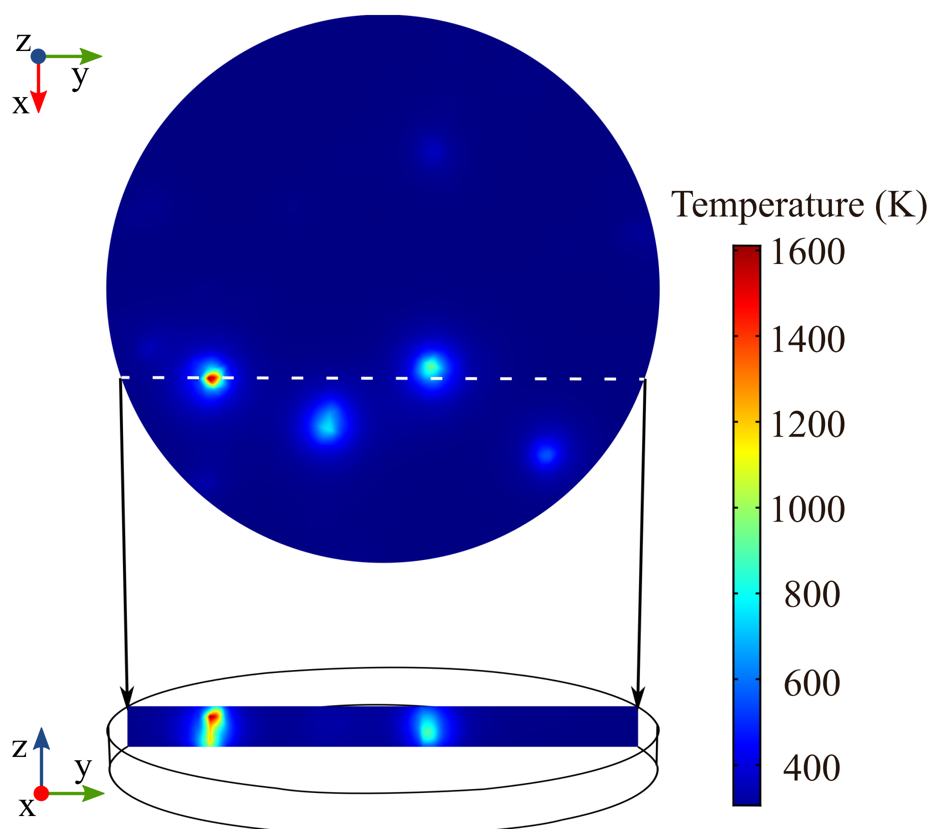


Figure 5.8: Simulated temperature distribution in a confined ta-C cell with a 5 nm thick ta-C layer and 50 nm cell diameter at dielectric breakdown after 4.4 μs into the SET pulse (see Figure 5.7); top shows distribution in the x,y-plane (at $z = 3.3$ nm), bottom shows distribution in the y,z-cross-section (indicated by the dotted line) with the hottest area at $z = 3.3$ nm (bottom to top); applied voltage is −3.15 V and voltage drop across the ta-C cell is −2.7 V [taken from [47]].

across the ta-C confined-cell (black) in Figure 5.7 was $|V| = 2.7$ V, and so these values were also used for the simulations.

In Figure 5.8 it can be seen that the highest temperatures were obtained at $z = 3.3$ nm, close to the mid-plane of the 5 nm thick ta-C layer. The temperature of the electrodes remained close to room temperature, 311 K at the Pt/ta-C interface and 337 K at the W/ta-C interface, which is expected as the metal electrodes acted as heat sinks [46]. The observed high temperatures close to the mid-plane of up to 1615 K are in agreement with reports from molecular dynamic (MD) simulations that were carried out by Dr. F. Zipoli under

the auspices of the EU FP7 project CareRAMM [46]. The obtained hot spots are likely to indicate the origin of sp^2 filament formation(s) after dielectric breakdown take(s) place.

The above findings emphasise the relevance of taking local variations in conductivity into account and underline the importance of numerical modelling to obtain a detailed temperature profile of the ta-C memory cell, which is not accessible otherwise. To illustrate this, a comparison between the average temperature in the memory cell and the maximum temperature is plotted in Figure 5.9 as a function of the absolute value of the voltage drop across the memory cell.

The average temperature of the cell remained at moderate temperatures and reaches a maximum value of 320 K, which agrees well with values reported in [67]. However, the localised temperature can obviously be much higher, high enough to lead to the formation of sp^2 filaments and so induce resistive switching. This finding is important as it emphasises that localised Joule-heating does not significantly affect the average temperature within the memory cell as long as the size of the hot spot is negligible in comparison to the lateral dimensions. Also, the highly localised hot spots prior to a filament formation provide evidence that memory switching in carbon-based devices is a temperature activated process, which is in agreement with reports from MD simulations [46, 111, 112]. Note that an increase of the sp^2 content would lead to a reduced distance between the sp^2 conducting clusters in the insulating sp^3 matrix. This in turn would result in larger currents and higher temperatures due to Joule heating being more effective. Once the lateral dimensions of the device approach the filament dimensions, it is suggested that the whole device can be re-amorphised using a standard reset pulse, which is expected to increase the cycling endurance significantly [43].

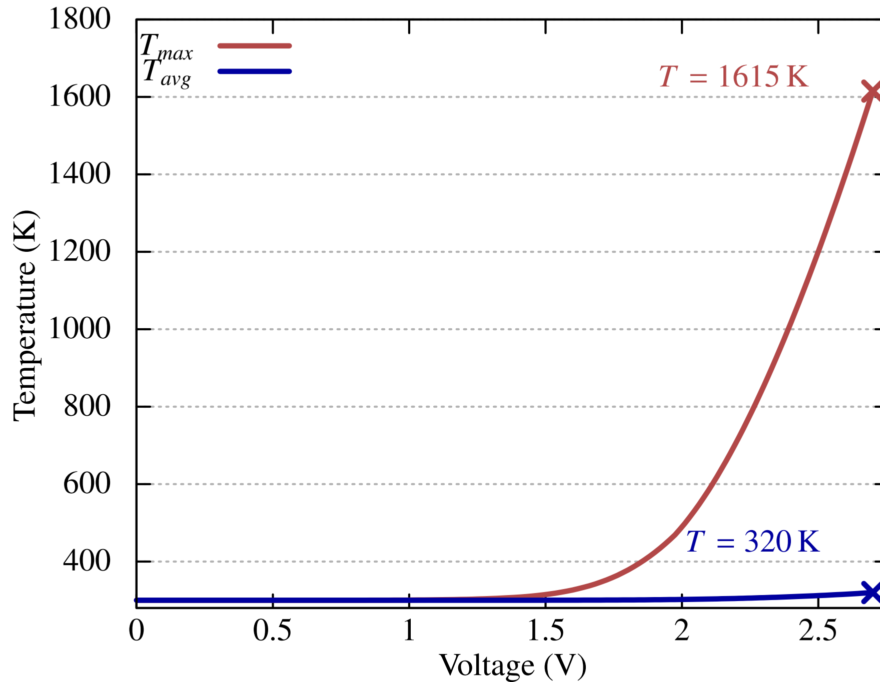


Figure 5.9: The maximum temperature inside the simulated ta-C confined-cell (cf. Figure 5.8) is plotted together with the average temperature as function of the absolute value of the voltage drop across the ta-C confined-cell [taken from [47]].

5.5 Influence of Load Resistor

To achieve a high cycling endurance in ta-C devices, a current limiting load resistor is required that has a resistance small enough to allow for efficient Joule-heating, but large enough to limit the current after memory switching has occurred. This is to ensure that the device can be reversibly switched from the thermodynamically stable LRS into the HRS.

To visualise the influence of the current limiting on-chip load resistor on the voltages necessary to achieve dielectric breakdown in ta-C confined-cell devices, the load resistor is varied from 2.5 kΩ to 50 kΩ, using the computational model introduced in Section 5.3. The conductivity of the ta-C cell is plotted as a function of the applied voltage for the

different load resistor values in Figure 5.10. The maximum temperature ($T = 1615\,\mathrm{K}$) within the ta-C cell at the onset of the dielectric breakdown (cf. Figure 5.9) is indicated by the red dashed line. The simulation results from Figure 5.10 show that the voltage that has to be applied to the device (including the load resistor) to induce the dielectric breakdown increases with increasing load resistor values from 2.70 V for $Rser = 2.5\,\mathrm{k\Omega}$, 2.85 V for $Rser = 7.5\,\mathrm{k\Omega}$, 3.15 V for $Rser = 13.3\,\mathrm{k\Omega}$, 3.37 V for $Rser = 25\,\mathrm{k\Omega}$, to 4.11 V for $Rser = 50\,\mathrm{k\Omega}$.

The strong increase of the applied voltage that was required to induce the dielectric breakdown in the device with $Rser = 50\,\mathrm{k\Omega}$, in comparison to the devices with lower load resistor values, suggests that localised Joule heating becomes less effective for higher load resistor values due to the increased voltage drop across the resistor.

This finding suggests that the load resistor used in the experimental switching of ta-C confined-cell devices with sp^3 contents of 0.5 (as in the work of this thesis) should be below 50 kΩ. Further, it has to be noted that lower switching voltages are also preferable to minimise the excess current that flows through the ta-C device as a consequence of the dielectric breakdown (see Section 4.2) [43, 45].

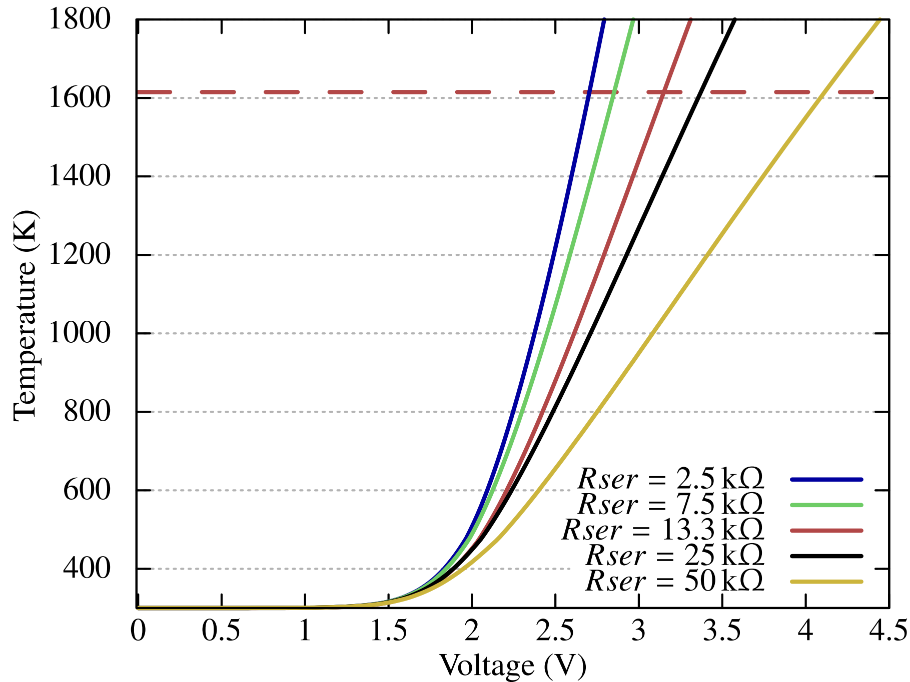


Figure 5.10: Maximum temperature in the ta-C confined-cell as function of the applied voltage across the device (including $Rser$). The maximum temperature at the onset of the dielectric breakdown event (see Figure 5.7) at $T = 1615\,\mathrm{K}$ is indicated by a red dashed line.

5.6 Influence of Confined-Cell Lateral Dimension

To evaluate the device performance for smaller lateral confined-cell dimensions, the maximum temperature within the ta-C cell of devices with ta-C cell radii of 15 nm and 10 nm are compared to the maximum temperature obtained from the simulation of a ta-C confined-cell with a cell radius of 25 nm, which was used in the experiments (see Figure 5.6).

To assess the performance, the current which was required to reach the maximum temperature of 1615 K present at the dielectric breakdown event (see Figure 5.9), is compared for ta-C cell radii of 25 nm, 15 nm and 10 nm in Figure 5.11.

The current required to reach the temperature present at the onset of the dielectric breakdown decreased from 34 µA for a cell with a radius of 25 nm, to 20 µA for a cell with

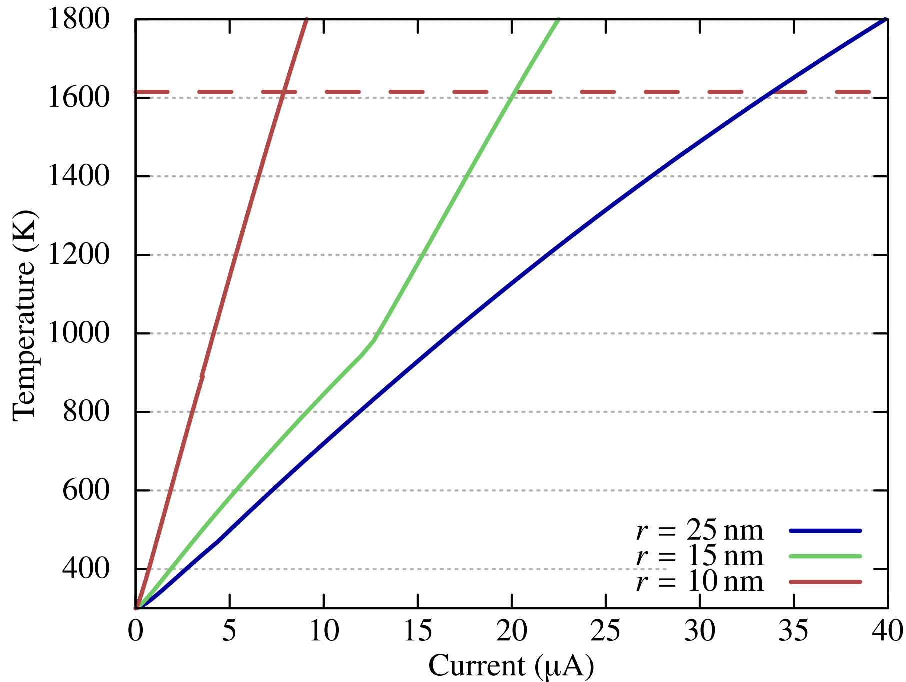


Figure 5.11: The maximum temperature inside the ta-C memory cell is plotted as function of the current flow for different ta-C confined-cell dimensions (radii). The maximum temperature at the dielectric breakdown event is indicated by a red dashed line.

a radius of 15 nm and to 8 μA for a cell with a radius of 10 nm. This corresponds to a four times lower power consumption at the onset of the dielectric breakdown event.[13] Therefore, a viable way to reduce the power and energy consumption in ta-C confined-cell devices for cyclic switching is to reduce the lateral dimensions of the ta-C cell.

5.7 Summary & Conclusion

In this chapter, it has been shown that the developed electro-thermal simulation model (which consisted of randomly distributed sp^2-rich clusters in an sp^3-rich insulating matrix to constitute the material composition of ta-C confined-cell memory devices, sp^2 content

[13]The applied voltage is used to calculate the power reduction.

dependent heat conductivities, and field- and temperature-dependent conductivities of the sp^3-rich clusters see Table 3.4), could successfully reproduce the experimentally obtained conductivity ranging over ≈4 orders of magnitude, all the way from Ohmic conduction until dielectric breakdown.

This very good agreement between experiment and simulation allowed for the first time — to the best of knowledge — to show, on the device-scale and using realistic electrical switching pulses, that local variations in conductivity between sp^2-rich and sp^3-rich clusters in ta-C confined-cells cause localised Joule heating, which in turn, leads to locally very high temperatures (*here* 1615 K) at the onset of the dielectric breakdown. The presence of one or several hot spots as a consequence of localised Joule heating via randomly distributed conductive sp^2-rich clusters in an otherwise insulating sp^3 matrix, is likely the origin of the formation of one (or several) conductive filament(s) that is/are established during electrical switching from the HRS into the LRS. This finding is in agreement with reports from MD simulations that suggest that the switching event from the HRS into the LRS is triggered by a temperature activated process.

Further, it has been shown that the choice of the series load resistor has a great impact on the required applied voltage that is necessary to achieve these high temperatures. It has been shown for ta-C confined-cell devices with an sp^2 content of 0.5 that Joule heating becomes inefficient for load resistors with resistance values of 50 kΩ due to the increased voltage drop across the series load resistor.

It has also been shown, for confined-cell devices with 5 nm thick ta-C layers, that a decrease of the lateral dimensions (area) from 50 nm diameters to 10 nm diameters led to a significant reduction of the current and power that is required to achieve the high temperatures present in the ta-C cell at the onset of the dielectric breakdown. This finding

is likely to have important consequences in terms of addressing the issue of limited cycling endurance in ta-C memory devices (i.e endurance should be improved by the scaling down of cell size).

Chapter 6

Oxygenated Amorphous Carbon (a-CO_x) Devices

As discussed in the previous chapters, a key challenge for amorphous carbon-based memory is cyclic endurance primarily due to the thermodynamical stability of the LRS. Besides, if fast and reliable SCM systems were to be successfully developed, a more fundamental problem limits the performance of current computer systems, namely the need for the constant transfer of data between the central processor (CPU) and the memory in order to carry out logic and arithmetic operations. This physical separation between storage and memory, the so-called von Neumann bottleneck, leads to limitations in computational speed and significant 'wasted' power (see Section 1.6). The limitations caused by the von Neumann bottleneck can be overcome or alleviated by carrying out certain logic and arithmetic operations directly in the memory and hence, overcoming the physical separation between logic and memory (see Section 1.6). This so-called memcomputing approach can be carried out using memristive devices.

To investigate the memristive capabilities of amorphous carbon based devices and to overcome the poor cyclic endurance of ta-C, confined-cell devices based on oxygenated amorphous carbon were employed due to their superior cyclic endurance in comparison to ta-C [63]. Details about the device fabrication are provided in Section 3.1.2 and [63], testing

methods are provided in Section 3.1.3 and an overview of the electro-thermal model used to model the temperature distribution during reverse switching from the LRS into the HRS is provided in Sections 3.2.1 and 3.2.3.

In the first part of this chapter, the switching energies of confined-cell devices with 18 ± 2 nm thick a-CO_x layers are investigated and their resilience towards high SET energies and powers is demonstrated. Further, the role played by oxygen atoms in the switching process is highlighted. For the remainder of this thesis the uncertainty in the film thickness of ± 2 nm will be omitted for better readability and the given film thicknesses refer to the nominal film thicknesses.

The second part, and main focus of this chapter, is on the examination of the memristive capabilities of a-CO_x confined-cell devices, and in particular their ability to provide the multilevel and accumulation properties that underpin memcomputing type applications. The last part of this chapter aims to shine light on the accumulation properties of a-CO_x confined-cell devices by investigating the role temperature plays during a series of input pulses. The temperature distribution was obtained using computational (FE) modelling of experimentally applied (accumulative) input pulses.

Partial results of the presented work in this chapter have been published in:

- ”Carbon-Based Resistive Memories,” in 2016 *IEEE 8th International Memory Workshop (IMW)*, pp. 1–4, IEEE, 2016. *DOI: 10.1109/IMW.2016.7493569*
- ”Memristive Effects in Oxygenated Amorphous Carbon Nanodevices,” in 2017 *Nanotechnology.*, vol. 29, no. 3, p. 035201, 2017. *DOI: 10.1088/1361-6528/aa9a18*

6.1 Switching Characteristics

To explore the resilience of confined-cell devices with 18 nm thick a-CO_x layers towards high SET energies and powers, a randomly selected confined-cell device with a 100 nm diameter was SET from the pristine state (65 MΩ) into the LRS (23 kΩ) using an SMU IV sweep from 0 V to 7 V. Afterwards, the device was cycled more than ten times to ensure that it was still functional, using RESET pulses with amplitudes of −2.0 V and durations of 7 ns and SET pulses with amplitudes of 3.2 V and durations of 50 ns. It has to be noted that during the work of this thesis reversible switching after an initial SMU SET was only achieved in confined-cell devices based on a-CO_x (and not on ta-C).

Exemplar results for a pair of RESET and SET pulses applied to the a-CO_x confined-cell device are shown in Figure 6.1. The RESET pulse that switched the device back into the HRS (1.4 MΩ) is shown in Figure 6.1a, with the corresponding current response shown in Figure 6.1b. No load resistor was present during the reverse switching from the LRS into the HRS. The timelines of the current signals are adjusted to the voltage output timelines, which allows the direct comparison of the current response to the applied voltage. The energy required to RESET the device was 1.0 pJ. The subsequent SET pulse that switched the device from the HRS into the LRS (29 kΩ) is shown in Figure 6.1c. The voltage drop is plotted across the device (including the 40 kΩ load resistor) as well as across the a-CO_x confined-cell, to highlight the load shift at the switching event. The corresponding current response shown in Figure 6.1d. The energy required to SET the device was 2.3 pJ. The energy calculation is based on the voltage drop across the a-CO_x cell.

The RESET speed shown in Figure 6.1 is significantly faster than previously reported RESET speeds of a-CO_x-based memory devices (see Table 2.2), the cycling between states is more than 40 times lower in energy than NAND flash cells and is comparable

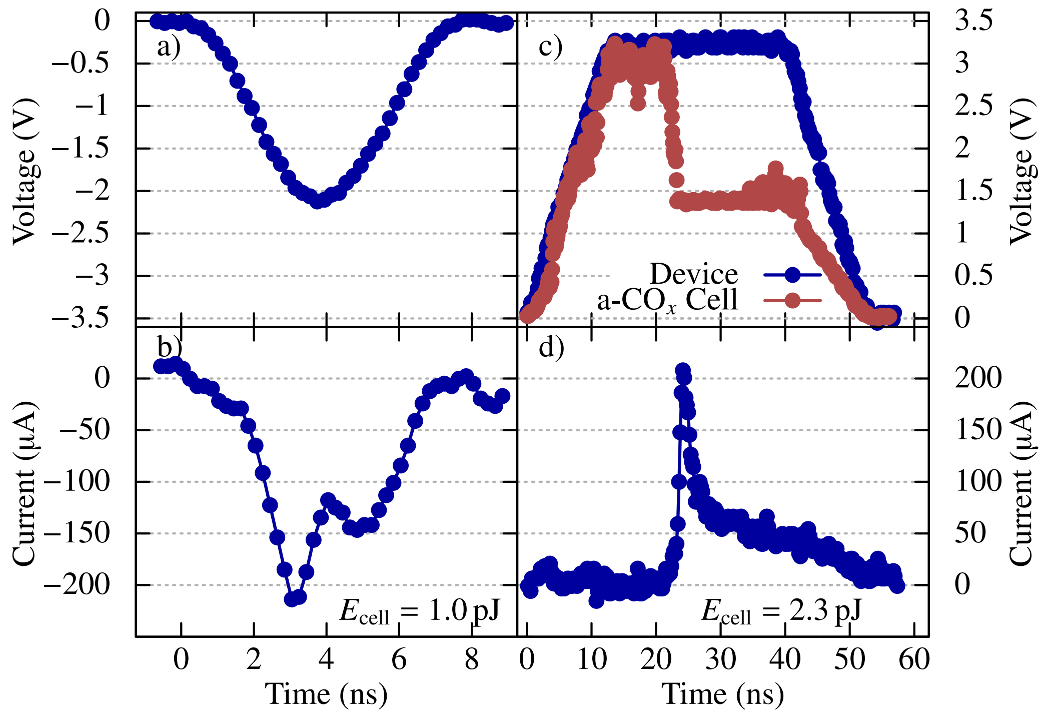


Figure 6.1: a) Applied RESET voltage over a confined-cell device (100 nm diameter) with an 18 nm thick a-CO$_x$ layer. **b)** Current response of the device during the reversible switching from the LRS into the HRS. **c)** SET pulse including the 40 kΩ R_{ser} (blue) and the voltage drop across the a-CO$_x$ cell itself (red). **d)** Current response during the switching (SET) process [taken from [46]].

to (or better than) other emerging technologies (see Tables 1.1 and 1.2). The obtained switching speed and writing energy consumption of a-CO$_x$ confined-cell devices fulfil the requirements for SCM as denoted in Table 1.1. Furthermore, the RESET speed and current is comparable to devices based on ta-C (see Figure 4.5), which indicates that the reverse switching speed — at least for ns-pulses — is not adversely affected by the addition of oxygen.

6.2 Thermal Annealing

As mentioned in Section 6.1, for sub-10 ns RESET pulses the reverse switching currents in a-CO_x are similar to the RESET currents observed in ta-C-based devices (see Figure 4.5). However, the addition of oxygen and a bipolar operation mode was found to greatly enhance the switching endurance [63]. Since the RESET process is the endurance limiting step for reversible cycling of memories based on amorphous carbon, it is likely that a different kind of thermal behaviour, due to the role played by oxygen atoms in the switching process, is responsible for the high switching endurance in a-CO_x-based memory devices.

To confirm (or otherwise disprove) the expectation of a different thermal dependence of the resistance for a-CO_x-based devices than for ta-C films and devices, a randomly selected confined-cell device with a 100 nm diameter and an 18 nm thick a-CO_x layer was SET into the LRS ($R_{LRS} = 3.6\,\mathrm{k\Omega}$) via an I-V sweep to 11 V (see Figure 6.2a), and then the device resistance monitored during various heating and cooling cycles.

The evolution of the resistance is shown in Figure 6.2b during the annealing cycle of this confined-cell device as it was heated from 40 °C to 300 °C (at 2 °C min^{-1}), when it was being held at 300 °C for 5 min, and then during the cooling down cycle (also at 2 °C min^{-1}). Between 40 °C and 236 °C, the resistance decreased with temperature and showed, as previously observed [63]. A thermally-activated behaviour can be well described by a $\log \sigma_R \sim E_a/(k_B T)$ behaviour between RT and 118 °C with E_a being the activation energy for conduction (here $E_a = 36\,\mathrm{meV}$), k_B the Boltzmann constant and T the temperature in Kelvin. Between 236 °C and 300 °C however, the resistance of the a-CO_x confined-cell device increased, with the increase being quite dramatic (three orders of magnitude) between 260 °C and 300 °C. Such increases of resistance with temperature are in stark

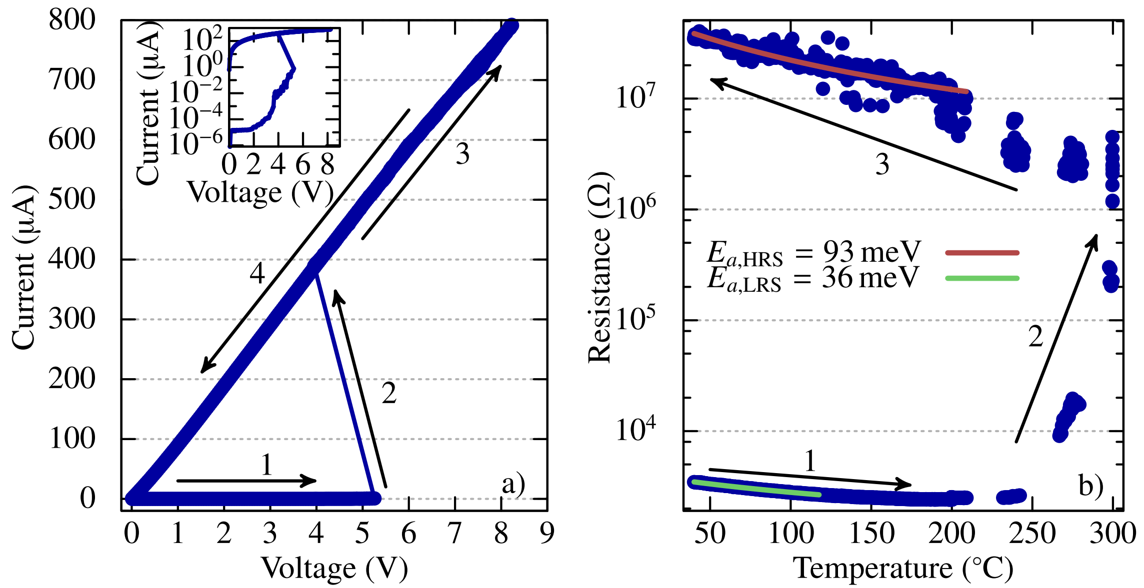


Figure 6.2: a) I-V curve for an a-CO$_x$ confined-cell device (used to SET the device into LRS for the measurements reported in b). The voltage was measured across the device itself (i.e. with the voltage drop across the series resistor subtracted) and the inset shows the I-V curve with the current on a log scale. **b)** The variation of resistance as a function of annealing temperature for the device of a) in the LRS; the fit of the activation energies $E_{a,LRS}$ and $E_{a,HRS}$ is shown in b) [taken from [137]].

contrast to that reported for films and devices based on elemental amorphous carbon, where the resistance decreases continuously with increasing temperatures (cf. Figure 4.8) [65, 92, 114, 116]. The resistance increase with increasing temperature in the a-CO$_x$ case can be linked to a re-distribution of oxygen within the cell during heating, with the oxygen breaking up the low-resistivity C-C sp^2 (graphite-like) rings and inducing high-resistivity C sp^3 (diamond-like) hybridization (see [63]). Upon cooling down to 40 °C, the resistance of the a-CO$_x$ devices followed again a $\log \sigma_R \sim E_a/(k_B T)$ type behaviour, with an activation energy in this case of $E_a = 93\,\mathrm{meV}$. The value of the activation energy, together with the high resistance of the device, suggests that electrical transport was mainly governed by hopping between localised states (see Section 2.4.2). However, without detailed knowledge of the DOS it is not possible to determine the activation energy more

accurately (see discussion in Section 5.1) and hence, the value provided for E_a should be interpreted as an estimation.

The data shown in Figure 6.2b indicate that, in addition to the electrochemical mechanism already identified [63] as the main driving force for the resistive switching process in a-CO_x-based devices, there is most likely also a thermal component involved in the switching, most probably as a result of thermally-driven diffusion of oxygen ions. In any case, the results of Figures 6.2a and 6.2b indicate that, by appropriate control of a-CO_x cell excitation conditions, it should be possible to access intermediate resistance levels, lying between the LRS and the HRS, something that has not been previously reported and so is explored in the next sections.

6.3 Multilevel States

To evaluate the possibility of accessing multilevel resistance states, a-CO_x confined-cell devices were SET from the pristine state into the LRS (via an I-V sweep), input excitations (voltage pulses) of various amplitudes and durations were applied, and the resulting device resistance measured. Typical results are shown in Figure 6.3. Here, the device was first cycled six times between a partial RESET state, with a resistance of roughly (on average) 1 MΩ, and the SET state by a sequence of (partial) RESET pulses having a duration of 7 ns and an amplitude of −2.1 V (top electrode grounded) and SET pulses of 60 ns duration and 3.2 V amplitude. Following this, a sequence of seven 7 ns/−2.5 V RESET pulses was applied, again interleaved with 60 ns/3.2 V SET excitations, and a significantly higher HRS resistance of around (on average) 50 MΩ was achieved. The results of Figure 6.3 show that multilevel states can indeed be accessed in a-CO_x confined-cell devices,

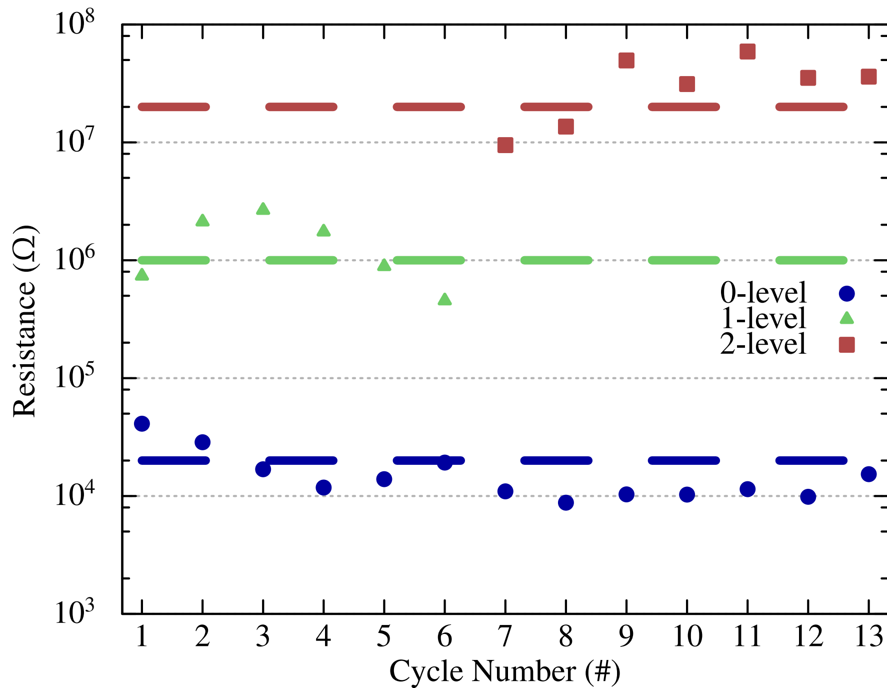


Figure 6.3: Cycling between multilevel resistance states in a-CO$_x$ confined-cell devices. Here three programmed states are shown, one LRS (0-level) state and two HRS (1-level and 2-level) states. The 0-level is accessed (programmed) using 60 ns/3.2 V pulses, while the 1-level and 2-level states are accessed using 7 ns/−2.1 V and 7 ns/−2.5 V pulses respectively. (Note that the dashed lines are simply guides for the eye [taken from [137]].)

although in this case cycle-to-cycle variation in resistance is not insignificant. Nonetheless, three distinct and readily distinguishable resistance levels are observed, equivalent to the storage of 1½ bits per cell (specifically, in this case, the 0-level (SET level) has resistances between 41 kΩ to 88 kΩ, the 1-level (partial RESET level) has resistances between 450 kΩ to 2.7 MΩ and the 2-level (full RESET) lies between 9.5 MΩ to 59 MΩ).

6.4 Memristive Effects

The exploitation of accumulation properties has previously been used successfully in phase-change memory type devices to carry out addition, subtraction, multiplication and

division directly in high-order bases (e.g. base-10), as well as more complex arithmetic processing such as parallel factorisation [19, 62]. Moreover, once such arithmetic computations are completed, the result is automatically stored in the device (which is in itself a non-volatile memory) that carried out the calculation. Thus, processing and memory can be carried out simultaneously by one and the same device, providing a form of computing-in-memory, or memcomputing (see Section 1.6). An alternative view of this kind of processing is as a form of non-von Neumann computing, in which the need (of a conventional von Neumann computer) to constantly transfer data between the processing unit and an external memory is removed, so potentially saving significant amounts of energy and potentially increasing computation speeds.

As a first step to test the memristive capability of a-CO_x confined-cell devices for the potential use in memcomputing applications, the effect of short (nanosecond), low amplitude (partial) RESET pulses on the resistance state of a randomly selected a-CO_x confined-cell with an 18 nm thick a-CO_x layer was investigated. Here, the device was switched from the pristine state into the LRS (1.8 kΩ) during an IV sweep to −14 V. Subsequently, 16 gradual RESET pulses with a duration of 8 ns and an amplitude of −0.5 V were applied. To study the effect of the amplitude on the resistance state, this was followed by 15 partial RESET pulses with the same duration and an amplitude of −0.7 V. The resistance of the device was read out after each RESET pulse and is shown in Figure 6.4 as a function of the pulse number. The resistance increased monotonously with every RESET pulse. The observed resistance increase is likely a consequence of high temperatures due to Joule heating (see Section 6.2), with the potential aid of the electric field helping to re-distribute the oxygen away from the tungsten electrode (this correlation between resistance and temperature evolution in the device is examined in more detail in Section 6.6) [63]. A subsequent increase of the amplitude to −0.7 V causes further increase of the resistance, which is attributed to more efficient Joule-heating accompanied by a larger

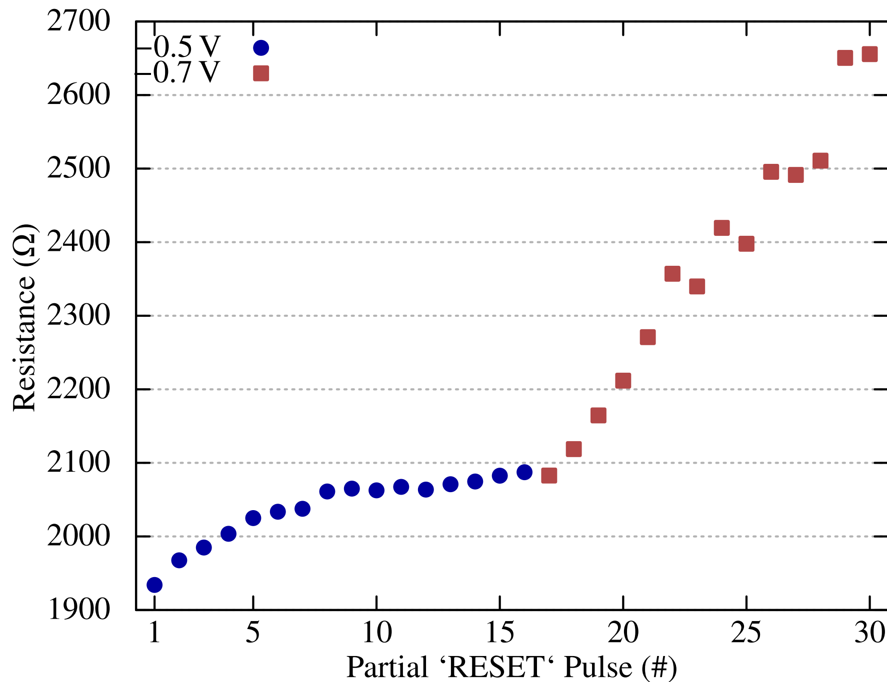


Figure 6.4: Resistance evolution of the LRS in a confined-cell device with an 18 nm thick a-CO_x layer as a function of partial RESET pulses with durations of 8 ns and amplitudes of −0.5 V and −0.7 V, respectively.

electric field affecting the oxygen distribution in the cell. This finding suggests that short RESET pulses of varying amplitude allow for the control of cell resistance when moving from the LRS to the HRS configurations. Hence, the observed accumulation response of a-CO_x confined-cell devices to partial RESET pulses makes a-CO_x-based devices viable candidates for memcomputing type applications. The memcomputing capabilities of a-CO_x confined-cell devices are investigated in the following section in more detail.

6.5 Low Energy Memcomputing

The basic process of accumulation-based computing involves the excitation of a memory-type device by a predetermined number of identical electrical pulses. Note that, unlike in

the case for multilevel storage, accumulation does not require that *all* individual resistance levels are distinguishable, merely that it is possible to (reliably and repeatably) determine that the pre-set resistance threshold has been reached/passed (cf. Section 1.6). This in turn requires that (or at least is easier to do if) the cell resistance changes monotonically as the number of input pulses increases, and that the window between the resistances of the cell after the input of (n-1) and n input pulses is sufficiently large.

To investigate the memcomputing capabilities of a-CO_x confined-cell devices, a randomly selected device with an 18 nm thick a-CO_x layer was SET into the LRS state via an I-V sweep (in this case leading to a SET resistance of $\approx$2.5 kΩ). Then, a series of short (8 ns), low voltage (-0.9 V) input pulses was applied, while the resistance was measured after each applied partial RESET pulse. The results are shown in Figure 6.5a, here for the case of 30 successive input pulses. The variation in resistance with pulse number displays a sigmoidal-like response, which is well-suited to the implementation of an accumulator [62]. Moreover, between pulses 13 and 16 the resistance changes are well separated, allowing the ready placement of a suitable detection threshold. For example we could, as shown in Figure 6.5a, place the decision threshold between state-15 and state-16 (since the resistance window between those states is relatively large) and this would yield a base-16, or hexadecimal, accumulator. Such an accumulator would also have relatively low energy consumption, since the energy consumed per input pulse is around the pJ level or lower (see Figure 6.5b).

The response as obtained in Figure 6.5a could for instance be used for hexadecimal addition. For example, to add 7_{10} and 11_{10} (i.e. 7 + B in hexadecimal notation) one would first input 7 pulses (the augend of the addition that is being carried out) to an a-CO_x confined-cell device having the accumulator response of Figure 6.5a; this would take the cell to state-7 on the *R* vs. *PulseNumber* curve. Then, input pulses equal in number to

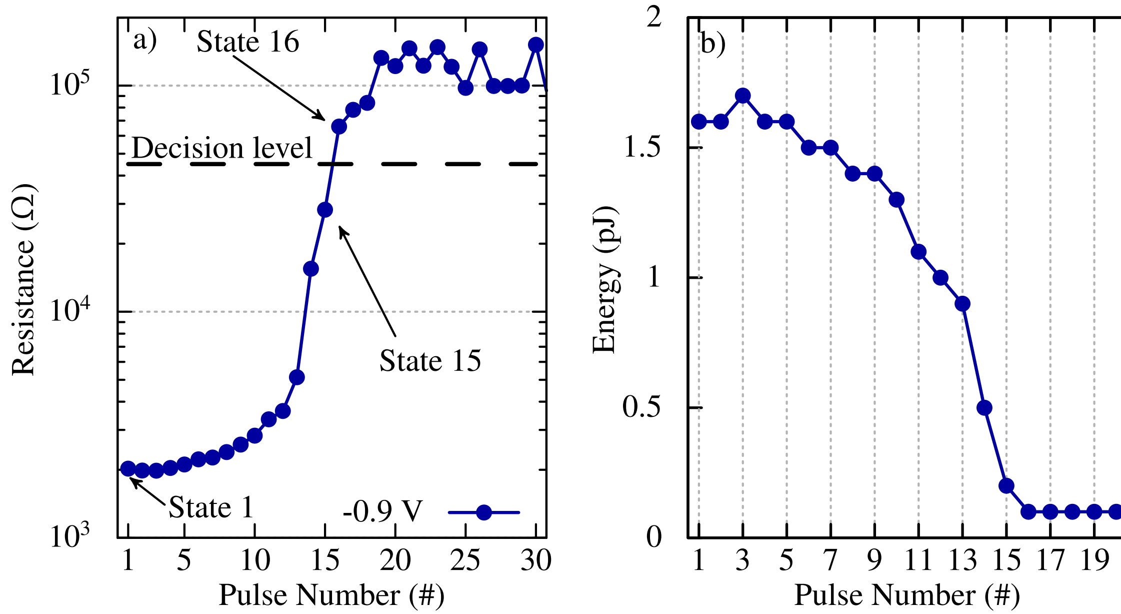


Figure 6.5: **a)** An accumulator-type response in an a-CO_x confined-cell obtained by the input of a series of identical -0.9 V/8 ns pulses. Also shown is position of a (resistance) decision threshold for use as a base-16 accumulator. **b)** The energy consumed per pulse (first 20 pulses only shown) for the accumulator of a) [taken from [137]].

the addend (11_{10}) would be applied to the device. However, in this case after receipt of pulse #9 of this addend sequence of 11 pulses, the cell resistance would cross the pre-set decision threshold (set between state-15 and state-16), this would be detected (by additional circuitry) and the cell would be SET back into the LRS state before the remaining addend pulses (i.e. pulses #10 and #11) were inputted (cf. Section 1.6). After completion of this whole process the a-CO_x cell would be in state-2, and one SET process would have been carried out. By this means the cell has computed the addition 7 + B in hexadecimal and the result is given by the number of times the cell has been SET (due to passing the decision threshold) along with the number stored in the cell itself. To access this stored number, further identical input pulses to the cell are required until it again crosses the decision threshold. Fourteen (14) pulses would be needed in this case, which is the (base-16) complement of the number we require (2). Thus $7_{10} + 11_{10} = 18_{10}$ (or in hexadecimal,

7 + B = 12).

To carry out the accumulator based computation of the hexadecimal addition (7_{16} + B_{16}) as above requires additional circuitry for both the detection of the crossing of the (resistance) decision threshold, the recovery of a number from its complement and the carry-over operation. However, such circuitry is not necessarily complicated; for example crossing of the decision threshold could be achieved by standard circuits used for resistive memory read out, in tandem with a comparator, while the generation of a number from its complement can be achieved by using a complementary accumulator cell (see [62]).

Moreover, it should be noted that the major benefit of using the accumulator approach is that a single nanoscale a-CO_x memory cell has, in the above example, carried out the core part of the task of adding two hexadecimal numbers and, importantly, stored the result in the self-same cell. Furthermore, the process is relatively fast (*here* 8 ns), fairly energy efficient (≈1 pJ per pulse) and easily parallelised (for the provision of multi-integer or fixed-point numbers).

Thus, it would seem that a-CO_x memory-type devices are potentially well-suited to memcomputing type operations. While the above example demonstrated the use of an accumulator arranged for base-16 or hexadecimal operation, other bases can of course be implemented by using different input pulse amplitudes and/or durations. In addition, it should be noted that programming the accumulator response as a form of gradual RESET (i.e. moving from the LRS to the HRS state) not only unlocks the high switching speeds inherent to the RESET process, but leads to a reduction in energy consumption as a computation proceeds. This is due to the decreasing current flow with increasing pulse number, as shown in Figure 6.6. Indeed, after around 20 input pulses the switching current is here comparable to the noise in the measurement circuit.

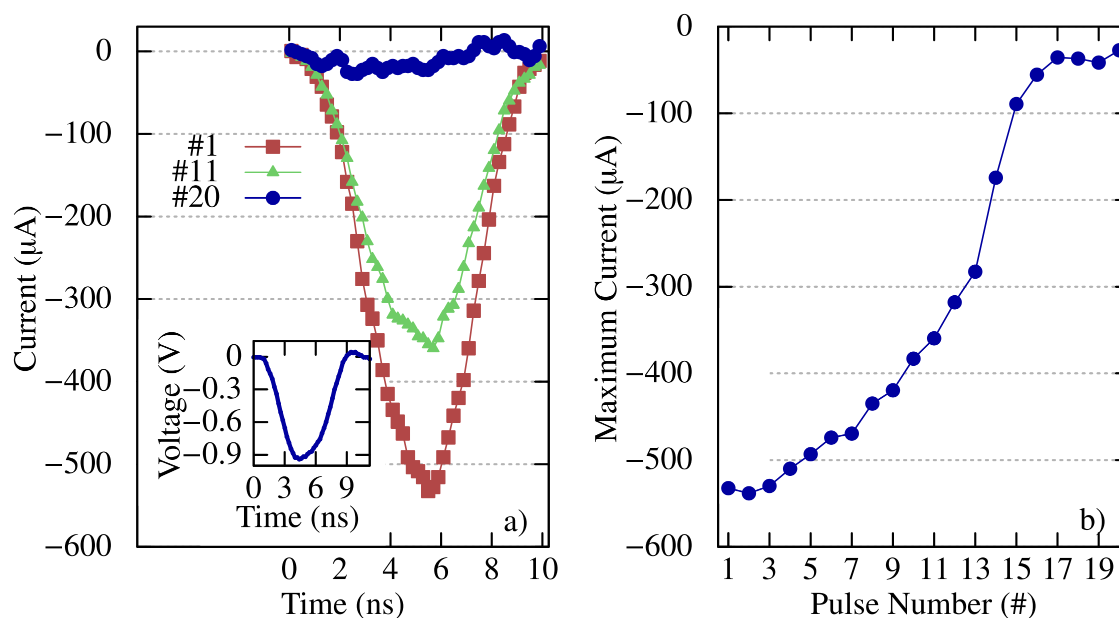


Figure 6.6: **a)** The switching current in the a-CO$_x$ confined-cell accumulator of Figure 6.5a for input pulse #1, #11 and #20 (inset shows the applied voltage pulse). **b)** The variation of (maximum) current during accumulator switching as a function of input pulse number [taken from [137]].

6.6 Thermal Analysis

The last part of this chapter aims to shine light on the role temperature plays in the a-CO$_x$ confined-cell accumulator response of Figure 6.5a, and further aims to validate that the SMU read out at 0.2 V did not affect the resistance state of the DUT during the experiments carried out to obtain the accumulator response of Figure 6.5a.

The computational model introduced in Section 3.2.3 assumed that the conductivity of the a-CO$_x$ confined-cell devices in the LRS (the starting state of the accumulation-based experiments) is almost entirely dominated by a conductive filament consisting of highly reduced a-CO$_x$ in an otherwise insulating sp^3-rich matrix [63].

The conductivity of the conductive, sp^2-rich filament was set equal to the sp^2 carbon conductivity and the diameter of the conductive filament was chosen such that the resistance of the a-CO_x confined-cell matched the experimentally determined resistance of Figure 6.5a. Therefore, the diameter of the conductive filament was set to 8.8 nm for the simulation of the first gradual RESET pulse of Figure 6.5a. This is in good agreement with a reported carbon filament diameter of 10 nm [43]. The sp^2 content of the conductive filament was set to 0.55 in the simulation.The diameter of the conductive filament (in the simulation) was reduced and adjusted to ensure that the simulated resistance corresponded to the experimentally measured resistance state of the preceding gradual RESET pulse in the results of Figure 6.5. More details about the computational model are provided in Section 3.2.3 and the most important material parameters are provided in Table 3.4.

The maximum temperatures that were obtained in the simulation of the first gradual RESET pulse (−0.9 V/8 ns) on the LRS (2.5 kΩ) of Figure 6.5a are shown in Figure 6.7a. The highest temperatures, with $T \approx 2.5 \times 10^3$ °C, were reached in the mid-plane of the filament at $z = 9$ nm after ≈3.6 ns into the gradual RESET pulse. The obtained high temperatures seem reasonable bearing in mind that the resistance of the initial LRS was fairly low (2.5 kΩ). In addition, it was reported that conductive carbon filaments can withstand even higher temperatures [43]. Further, the obtained maximum temperatures are well above the temperatures that were found necessary in Figure 6.2 to induce the transition from the LRS into the HRS, and confirm that despite the presence of high electric fields, temperature is likely to play an important role in the reverse switching process from the LRS into the HRS in a-CO_x devices.

The maximum temperatures that were obtained in the simulation of the read out of the resistance level (0.2 V/100 ms) of the LRS (2.5 kΩ) of Figure 6.5a are shown in Figure 6.7b. The maximum temperature $T = 137$ °C was reached in the mid-plane of the filament at

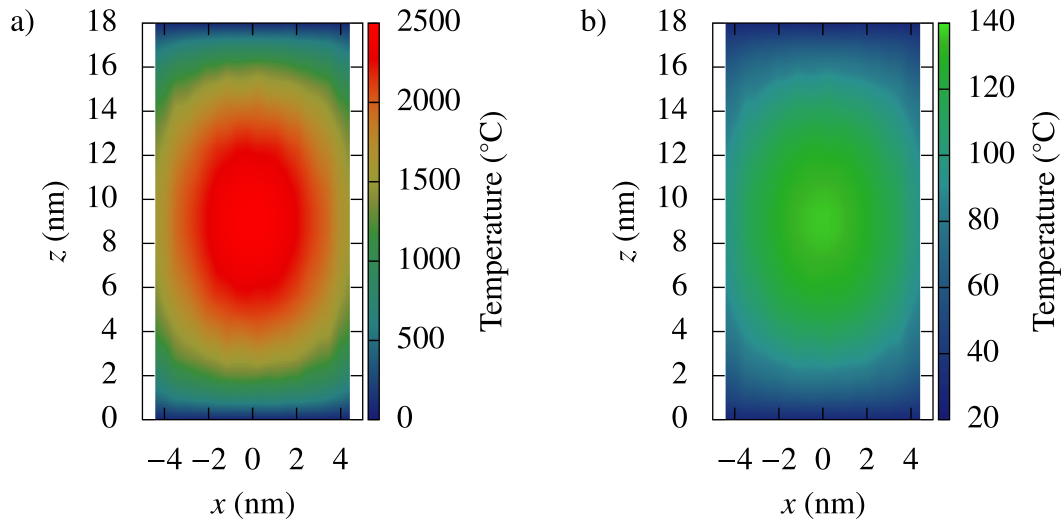


Figure 6.7: a) Simulated maximum temperature distribution in the conductive filament of an a-CO_x confined-cell after ≈3.6 ns into the gradual RESET pulse (−0.9 V/8 ns) on the initial LRS (2.5 kΩ) of Figure 6.5a. **b)** Maximum temperature during read out (0.2 V/100 ms) of the (same) LRS as in a).

z = 9 nm and remained significantly below the temperature threshold of 236 °C that was found necessary in Figure 6.2 to induce the transition from the LRS into the HRS (in the absence of aiding electrical fields), thus confirming that the read out of the resistance state at 0.2 V did indeed not alter the resistance state itself.

To investigate the relation between the different resistance levels (a consequence of the accumulator response) in Figure 6.5a and the temperatures in the conductive filament during the simulation of the gradual RESET pulses, the highest temperatures T_{max} obtained (in the simulation) are compared with the experimentally measured device resistances in Figure 6.8. The maximum temperatures are normalised by the highest temperature $T_{\mathrm{max,initial}}$ that was obtained for the initial LRS (2.5 kΩ) in Figure 6.5a.

The ratio of maximum temperature $T_{\mathrm{max}}/T_{\mathrm{max,initial}}$ decreased strongly with the device resistance increasing, and dropped to ≈10 % (≈250 °C) of its original value at around 30 kΩ.

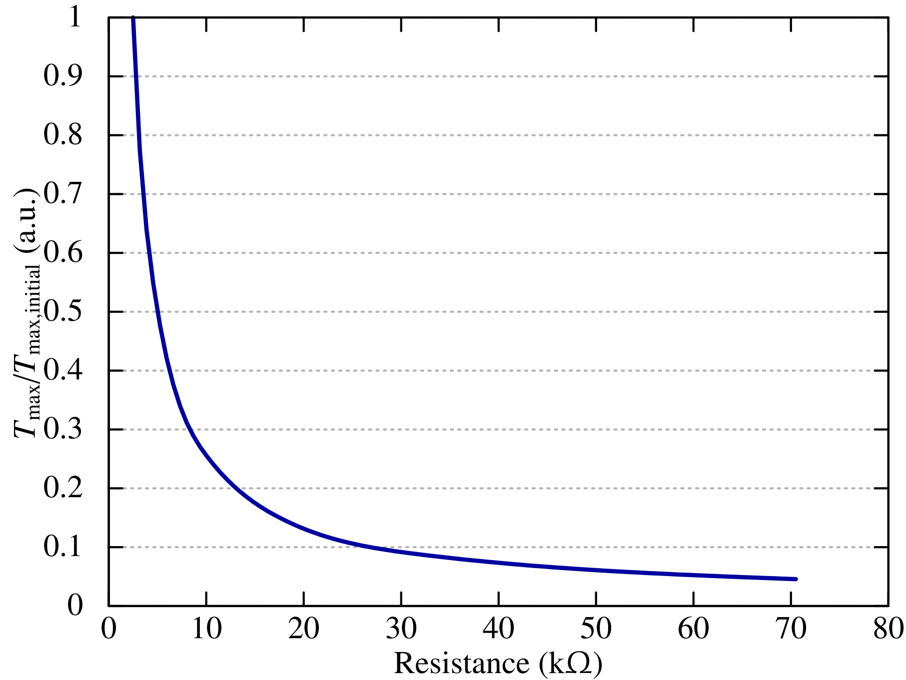


Figure 6.8: Evolution of the normalised maximum temperature in the conductive filament $T_{max}/T_{max,initial}$ of an a-CO_x confined-cell device during the accumulator response shown in Figure 6.5a.

This is close to the temperature threshold of 236 °C that was found necessary in Figure 6.2 to induce the transition from the LRS into the HRS (in the absence of aiding electrical fields) and provides an explanation why the resistance level of the HRS stabilises at ≈100 kΩ in Figure 6.5a and did not increase further, despite the fact that the gradual RESET pulse (−0.9 V/8 ns) was kept constant.

Further, this finding highlights the importance of a current limiter to control the resistance of the LRS during the switching from the HRS into the LRS, which is crucial for amorphous carbon-based memories that do not have a dopant (like oxygen) that facilitates the RESET process.

6.7 Summary & Conclusion

In this chapter, it has been shown that a-CO_x confined-cell devices can be reversibly switched from the LRS into the HRS using sub-10 ns pulses. In addition, the resilience of a-CO_x-based devices (in contrast to ta-C-based devices) was shown by resetting devices after they have been switched from the pristine state into the LRS using long, quasi-static IV sweeps. This capability of devices based on a-CO_x as the active material could be linked to the presence of oxygen by showing that the transition from the LRS into the HRS can solely be induced by high temperatures (>236 °C), in the absence of aiding electric fields. A solely temperature induced transition from the LRS into the HRS is in contrast to devices based on ta-C as the active material.

Additionally, it has been shown that simple two-terminal, nanoscaled, a-CO_x confined-cell devices, in addition to their previously demonstrated non-volatile binary memory functionality, possess memristive type capabilities including the ability to provide the multilevel and accumulation properties that underpin computing type applications. Specifically, the storage of 3-levels (1½ bits) per individual cell was successfully demonstrated, as well as an accumulator-like response suited to the provision of arithmetic processing. Exemplarily, a base-16, or hexadecimal, accumulator was implemented and it was shown how such a device can carry out hexadecimal addition and simultaneously store the resulting sum in a single a-CO_x confined-cell, all using fast (sub-10 ns) and low-energy (sub-pJ) input pulses.

Chapter 7

Conclusions & Future Work

7.1 Conclusions

In **Chapter 1** the performance gap between DRAM and NAND Flash was identified and the performance characteristic of different contenders for so-called storage class memories that lie in this gap were presented. The different contenders were classified according to the International Technology Roadmap for Semiconductors (2015) to either 'Prototypical Storage Technologies' or 'Emerging Storage Technologies'. It was pointed out that insulating amorphous carbon memory devices (e.g. based on ta-C or a-CO_x), whose operating principle is based on the reversible formation of a conductive sp^2 network, in an otherwise amorphous, insulating carbon matrix, have recently gained traction due to their fast switching speeds, good scalability and simple deposition techniques.

It was pointed out in **Chapter 2** that a clear understanding of the resistance switching mechanism in carbon-based resistive-switching memories is still lacking, and that the main challenges to achieve high cycling endurances in memories based on elemental tetrahedral amorphous carbon originate from their current sensitivity during the SET process. This is exacerbated by the fact that fast switching speeds lead to a high parasitic capacitive current, making it difficult to reset the device from the LRS into the HRS. Oxygenated

amorphous carbon was presented as an alternative to ta-C with potentially better cycling (switching endurance) properties, due to oxygen facilitating the RESET process.

The device characteristics and the material properties of ta-C and a-CO_x active layers were presented in **Chapter 3**. The experimental device setups that were used to evaluate the switching performance of (spatially) confined ta-C and a-CO_x devices were introduced, together with the characteristics of the finite-element model that was used to study the Joule heating effects in both, ta-C and a-CO_x confined-cell devices.

In **Chapter 4**, the switching performance of ta-C-based confined-cell devices with a 5 nm thick ta-C layer, which is — to the best of knowledge — the thinnest ta-C layer reported to show switching thus far, was presented. Notably, evidence was provided that the SET process is not governed by the electric field alone. The achieved switching speeds were well below 10 ns, which is – to the best of knowledge – the fastest SET speed reported to date for ta-C-based devices. In agreement with literature it was shown that the actual switching process from the pristine state into the LRS (i.e. the dielectric breakdown event) takes place on a sub-ns time scale. Further, data retention was obtained for >300 s at 450 °C, which is — to the best of knowledge — the highest reported temperature for any ta-C-based memory device thus far, showing the potential suitability of ta-C memories for high temperature applications. The reverse switching speed from the LRS into the HRS was observed to be well below 8 ns, which is significantly faster than in previous reports. Additionally, and in agreement with literature, evidence was shown that the switching from the HRS into the LRS is likely caused by the formation of a conductive sp^2-rich carbon filament. Moving to smaller cells should therefore improve the cyclability (switching endurance) of ta-C devices, since smaller switching currents lead, in general, to the formation of smaller and more easily disrupted sp^2 filaments.

In **Chapter 5**, it was shown that the developed electro-thermal computational model,

which used randomly distributed sp^2 and sp^3-rich clusters, can successfully reproduce experimentally obtained conductivity ranging over ≈4 orders of magnitude, all the way from Ohmic conduction until dielectric breakdown. It was also shown — to the best of knowledge — that as a result of the local variations in conductivity between sp^2 and sp^3-rich clusters, Joule heating caused locally very high temperatures that, in turn, triggered a temperature activated process leading to material modifications (i.e. switching) in tetrahedral amorphous carbon. Further, it was shown that Joule heating becomes inefficient for high load resistor values. Additionally, it was shown that smaller lateral dimensions of the ta-C cell reduce the required switching current and hence, the energy consumption.

In **Chapter 6**, the switching performance, temperature stability and memristive capabilities of spatially confined oxygenated carbon memory devices was investigated. The achieved RESET speeds were also below 10 ns, which is – to the best of knowledge – the fastest switching speeds reported for a-CO_x-based devices. The SET speeds were around 50 ns, which is en par with the fastest SET speeds reported previously. Additionally, the improved resilience of a-CO_x in comparison to ta-C was demonstrated by reversibly switching devices that had been initially set to the LRS using quasi-static IV sweeps up to 12 V. It was shown that the observed resilience towards large currents can be attributed to the presence of oxygen and further, it was shown that the transition from the LRS into the HRS can solely be induced by high temperatures (>236 °C), in the absence of large aiding electrical fields.

Multilevel storage in a-CO_x (3-levels or 1½ bits per individual cell) was also achieved for the first time, paving the way for an increased storage density. Further, the accumulator-like response of a-CO_x confined-cell devices towards partial RESET pulses was investigated. The latter was used to demonstrate the potential suitability of a-CO_x confined-cell devices for arithmetic processing in a non von Neumann computational architecture. For

this purpose it was shown that a base-16, or hexadecimal, accumulator can be successfully implemented. Further, it was shown how hexadecimal addition can be carried out, while the result is simultaneously being stored. It was shown that this arithmetic processing can be carried out in a single a-CO_x confined-cell, using fast (sub-10 ns) and low-energy (sub-pJ) input pulses.

The updated version of Table 2.2, including the results achieved within the framework of this thesis is presented in Table 7.1. The state-of-the-art benchmarks that were achieved in the work of this thesis are highlighted (*). Further, it has was shown that the actual switching event switching a ta-C confined-cell memory device, from the HRS into the LRS, is faster than 1 ns.

In conclusion, the work of this thesis has contributed to the development of new insights and understanding of the switching processes in ta-C and a-CO_x memory devices, it has demonstrated enhanced switching performances in such devices (e.g. in terms of switching speed, switching power/energy, cell size) and it has also successfully demonstrated that a-CO_x devices can offer additional functionalities including multi-level storage and memcomputing (the latter via the accumulation regime).

Table 7.1: Specifications of device performances for ta-C and a-CO_x.

	ta-C	a-CO_x
Maturity	Emerging	Emerging
Film Thickness	5 nm$^{(*)}$	18 nm$^{(*,15)}$
Device Diameter	50 nm$^{(*)}$	50 nm$^{(*,15)}$
SET Speed	7 ns$^{(*)}$	50 ns$^{(*,15)}$
RESET Speed	7 ns$^{(*)}$	7 ns$^{(*)}$
Retention Time	300 s @ 450 °C$^{(*)}$	10^4 s @ 85 °C$^{(15)}$
Endurance Cycles	$10^{3(14)}$	$4 \times 10^{4(15)}$
Write Energy per Bit	<1 pJ$^{(14)}$	≈2 pJ$^{(*)}$

$^{(*)}$ Achieved within the framework of this thesis
$^{(14)}$ Taken from [119]
$^{(15)}$ Taken from [63]

7.2 Future Work

The presented work demonstrated the switching capabilities of memory devices based on ta-C and a-CO_x and shed light on the challenges of cyclic endurance in ta-C based devices. To improve the cycling endurance, precise current control is paramount. Improvements in this direction can include the use of a transistor as current control unit and a reduction of parasitics to lower the excess current. Further, an improved device performance can be achieved by reducing the lateral and vertical dimensions. The latter would additionally increase the temperature gradient during the reset process, which is assumed to aid the reversible switching process. To shine more light onto the switching process in ta-C, the full cycling dynamics including dielectric breakdown and reversible switching could be investigated and potentially be described, in simulations, by implementing a cluster re-organisation that is based on a rate equation approach.

Additional functionalities, like multilevel storage and beyond von Neumann computation seem to be better addressable in filamentary memories based on a bipolar operation mode and hence, a-CO_x appears as a good candidate for potential memcomputing applications due to the low energy consumption of partial RESET series input pulses. Future work in this respect could include further development of the accumulator approach to carrying out arithmetic computations, for example by examining the time-stability of the intermediate resistance states of the accumulator, and by exploring intra- and inter-cell variations in switching properties (i.e. does each cell switch after the same number of pulses on repeated accumulations, is there significant inter-cell variability in the accumulator response). The use of multi-level resistance states and the accumulator response might also be explored for neuromorphic computing approaches, where the inherent stochastic nature of the conductive filament is beneficial in mimicking artificial synapses and neurons.

Appendix A

MD Simulations

The MD simulations were carried out in collaboration with work in this thesis by Dr. Federico Zipoli at IBM Research Zurich (under the auspices of the EU FP7 project CareRAMM). The MD model used a constant volume approach which reflects that the volume of the ta-C cell cannot change due to the spatial confinement between the electrodes and the side walls (see Figure 3.2). The initial sp^3 content was set to 0.5 in all simulations.

Partial results of the presented work in this chapter have been published in:

- ”Carbon-Based Resistive Memories,” in 2016 *IEEE 8th International Memory Workshop (IMW)*, pp. 1–4, IEEE, 2016. *DOI: 10.1109/IMW.2016.7493569*

A.1 Dihedral Angle

The influence of the dihedral angle, discussed in Section 2.4.1, on the conductivity of ta-C is visualised in Figure A.1. The delocalised, bonding π orbitals are approximated by 3D Gaussians and centred between the carbon atoms, whereas the anti-bonding π^* orbitals are approximated by 3D Gaussians centred on the carbon atoms. The conducting π orbitals

are indicated as 'good' bonds (red). The anti-bonding π^* orbitals are indicated as 'bad' bonds (blue).

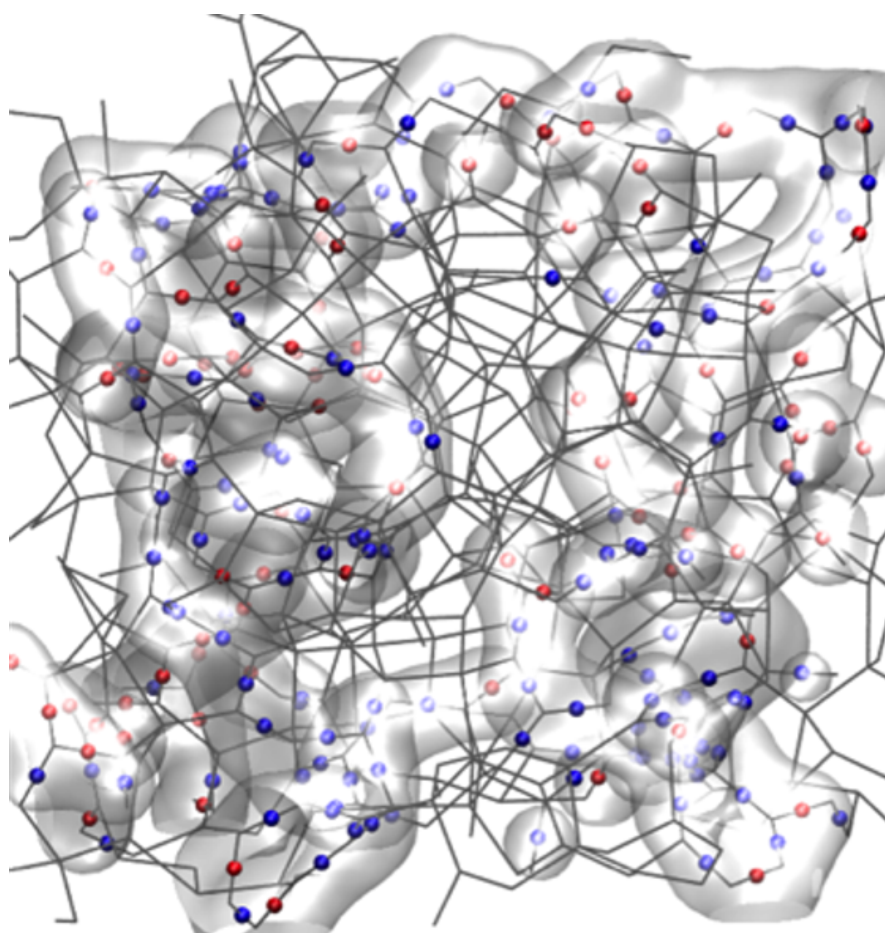


Figure A.1: The delocalised π orbitals ('good' bonds) are shown in red and the anti-bonding π^* orbitals ('bad' bonds) in blue.

A.2 Thermostat

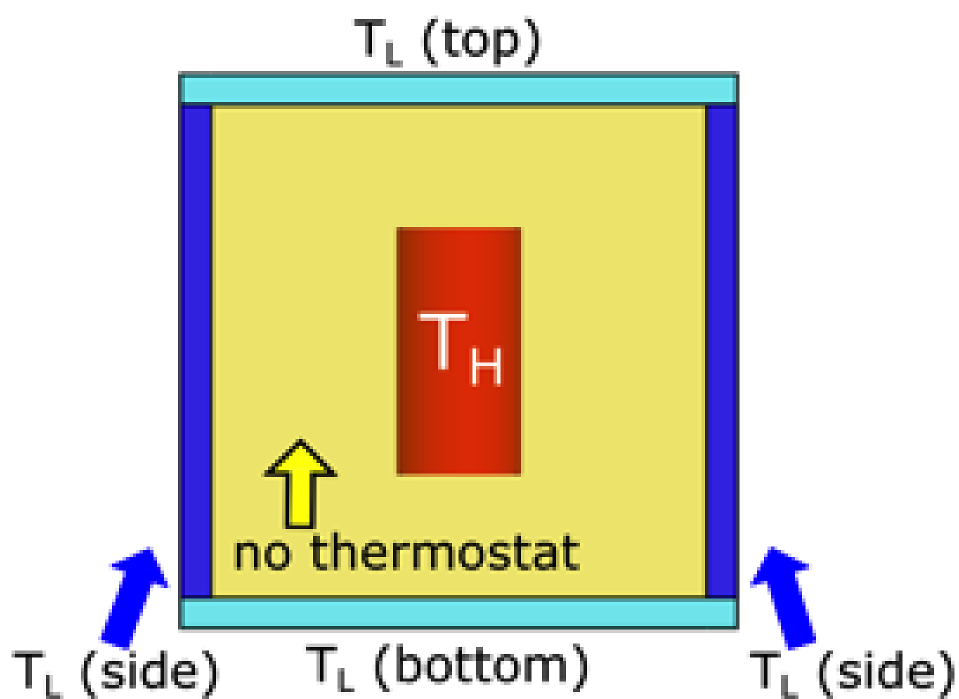


Figure A.2: The electrode temperature T_L (bottom), the side wall temperature T_L (side) and the temperature of the cylindric area around the conductive filament T_H were controlled in the MD model.

A.3 SET Process

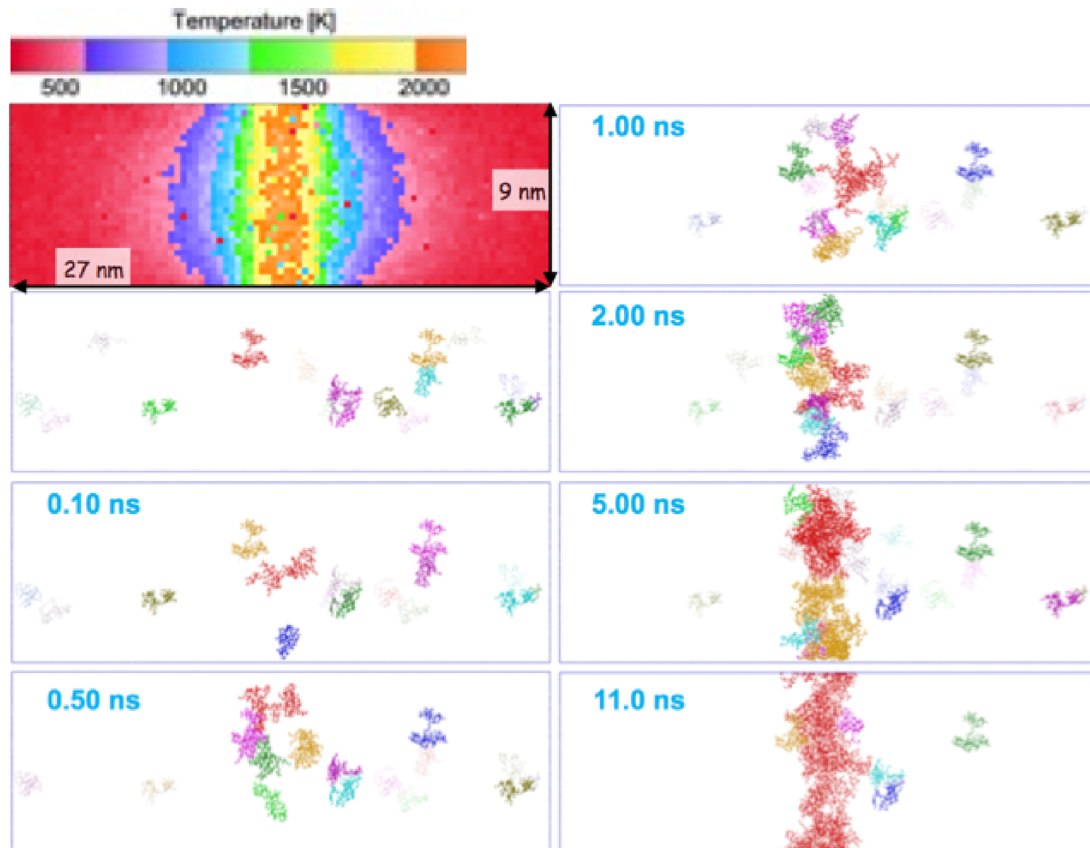


Figure A.3: Formation of a conjugated π-network after T_H was set to $2500\,\mathrm{K}$. A conductive percolation path bridging the two electrodes is established after $11.0\,\mathrm{ns}$ (red).

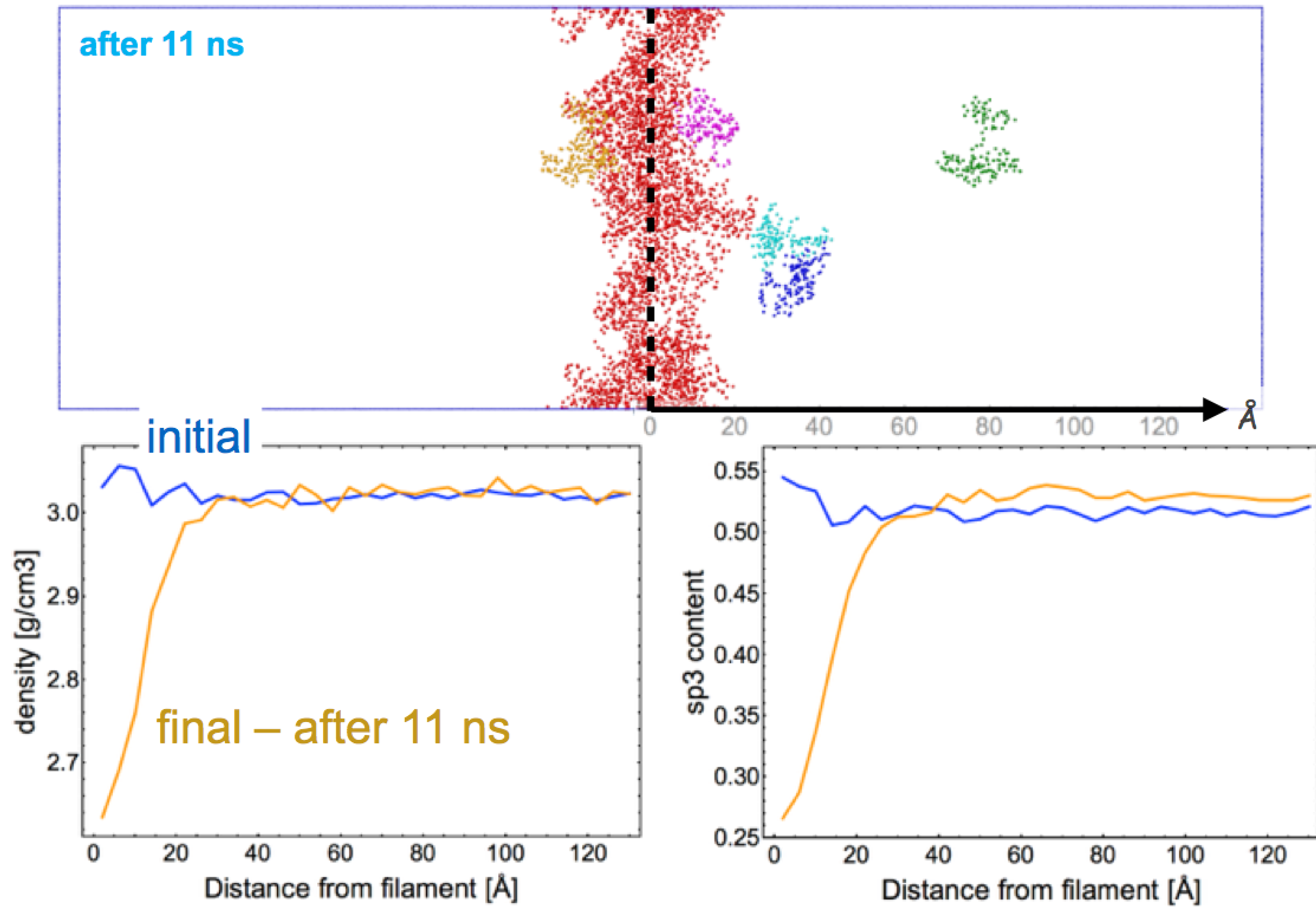


Figure A.4: The formation of a conductive filament (top) leads to a decrease in density in the vicinity of the filament (bottom left) in comparison to the initial state of the ta-C cell. The lower sp^3 content in the vicinity of the conductive filament (bottom right) is compensated by an increase of the sp^3 content further away from the filament.

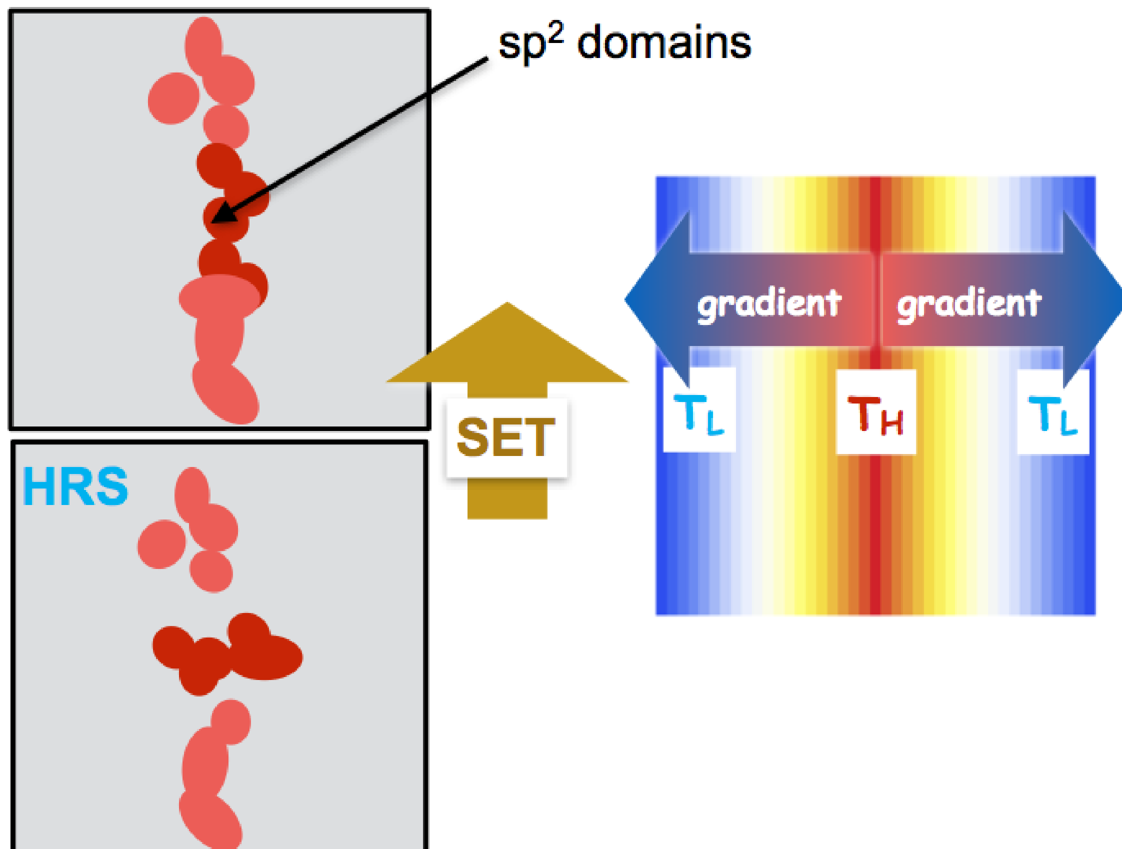


Figure A.5: The diameter of the conductive filament - formed in the SET process - is confined to small dimensions (few nanometers) in the presence of large lateral temperature gradients $(T_L - T_H)$.

A.4 RESET Process

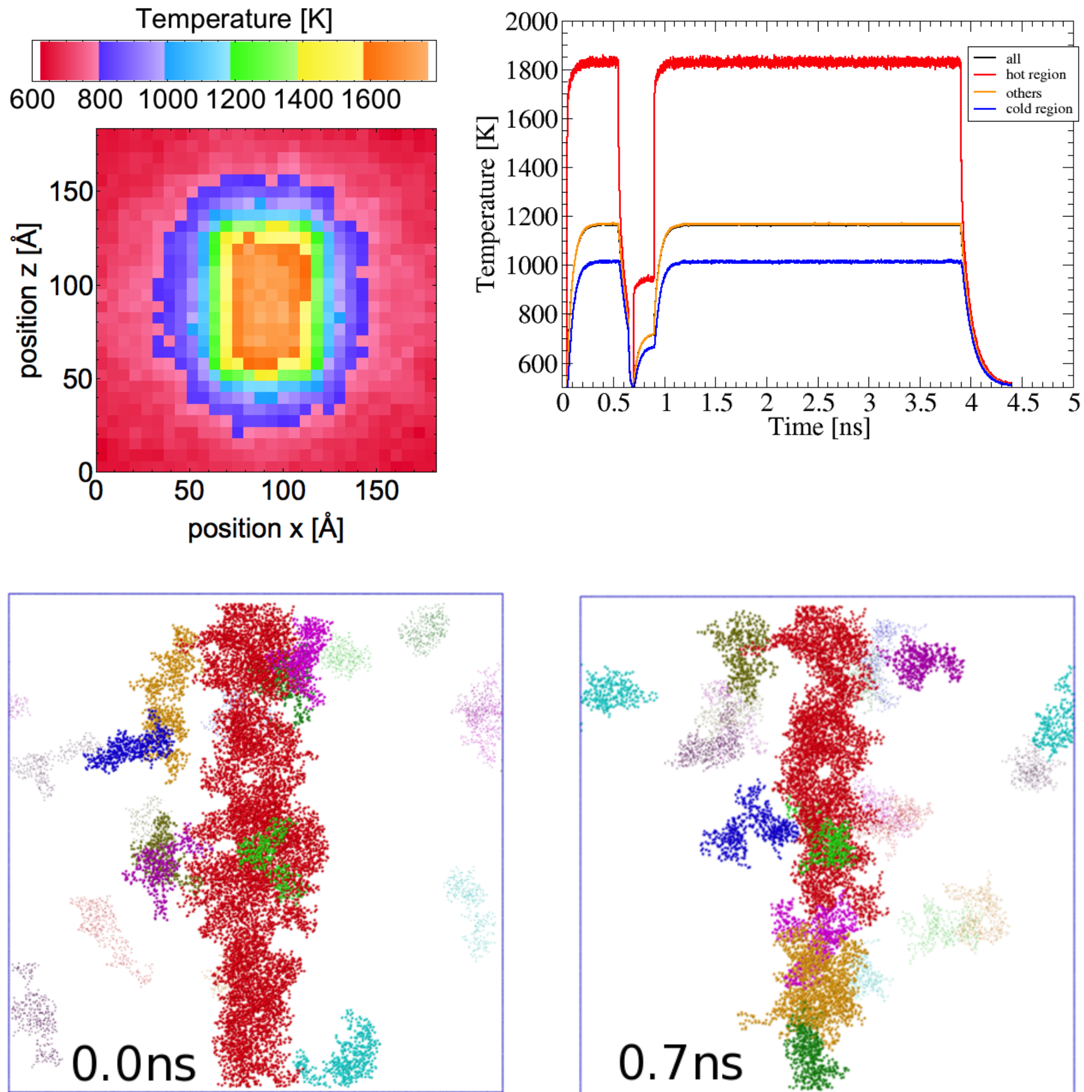


Figure A.6: Rupture of the percolating, conductive filament (bottom left in red) after the device was quenched by setting the thermostat temperatures $T_H = 1800\,\mathrm{K}$, T_L(side) $= 1200\,\mathrm{K}$ and T_L(bottom) $= 1000\,\mathrm{K}$ to $500\,\mathrm{K}$ within $0.2\,\mathrm{ns}$ (top right). The conductive path is ruptured after $0.7\,\mathrm{ns}$ (bottom right), i.e. after the quenching step [modified from [46]].

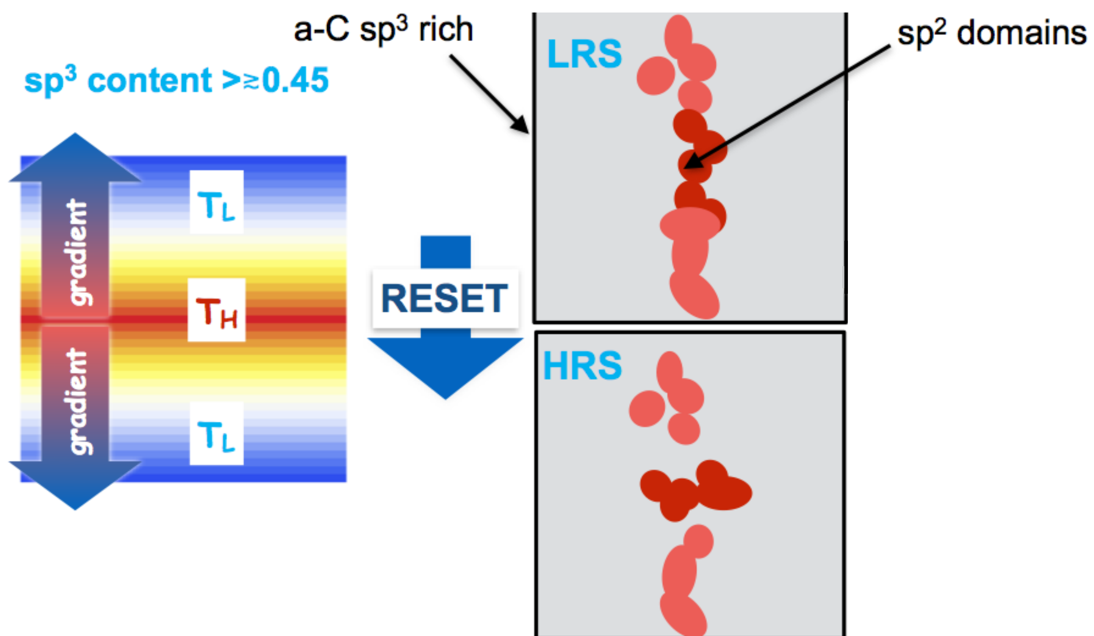


Figure A.7: The reverse switching process is promoted by large temperature gradients at the filament-electrode interface $(T_L - T_H)$.

A.5 Summary

The results of the MD simulations have shown that large lateral temperature gradients help to confine the diameter of the thermodynamically stable, sp^2-rich filament that is formed during the SET process. Further, simulations of the RESET process have shown that large temperature gradients at the filament-electrode interface help in destabilising the conductive filament and thus, promote the reverse switching process. These findings are important as they show ways of improving the cyclic endurance in ta-C based devices (see discussion in Section 2.5).

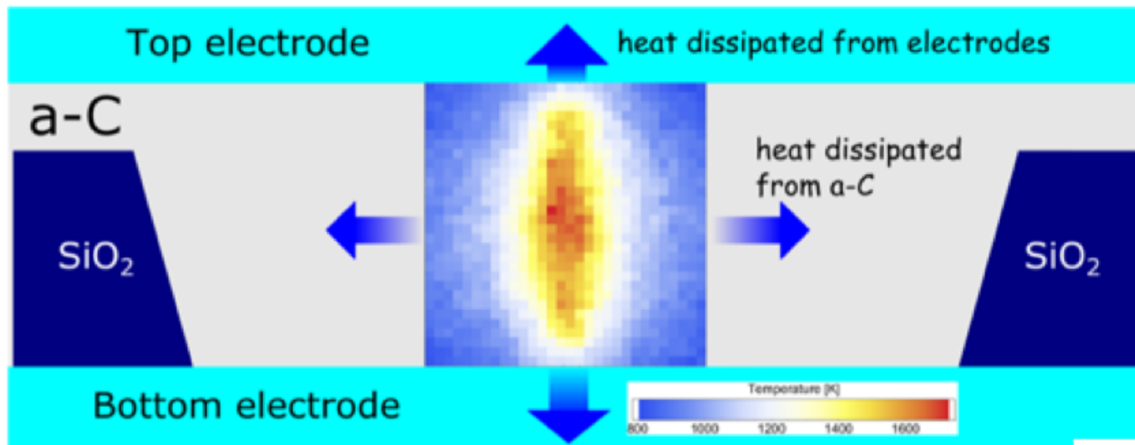


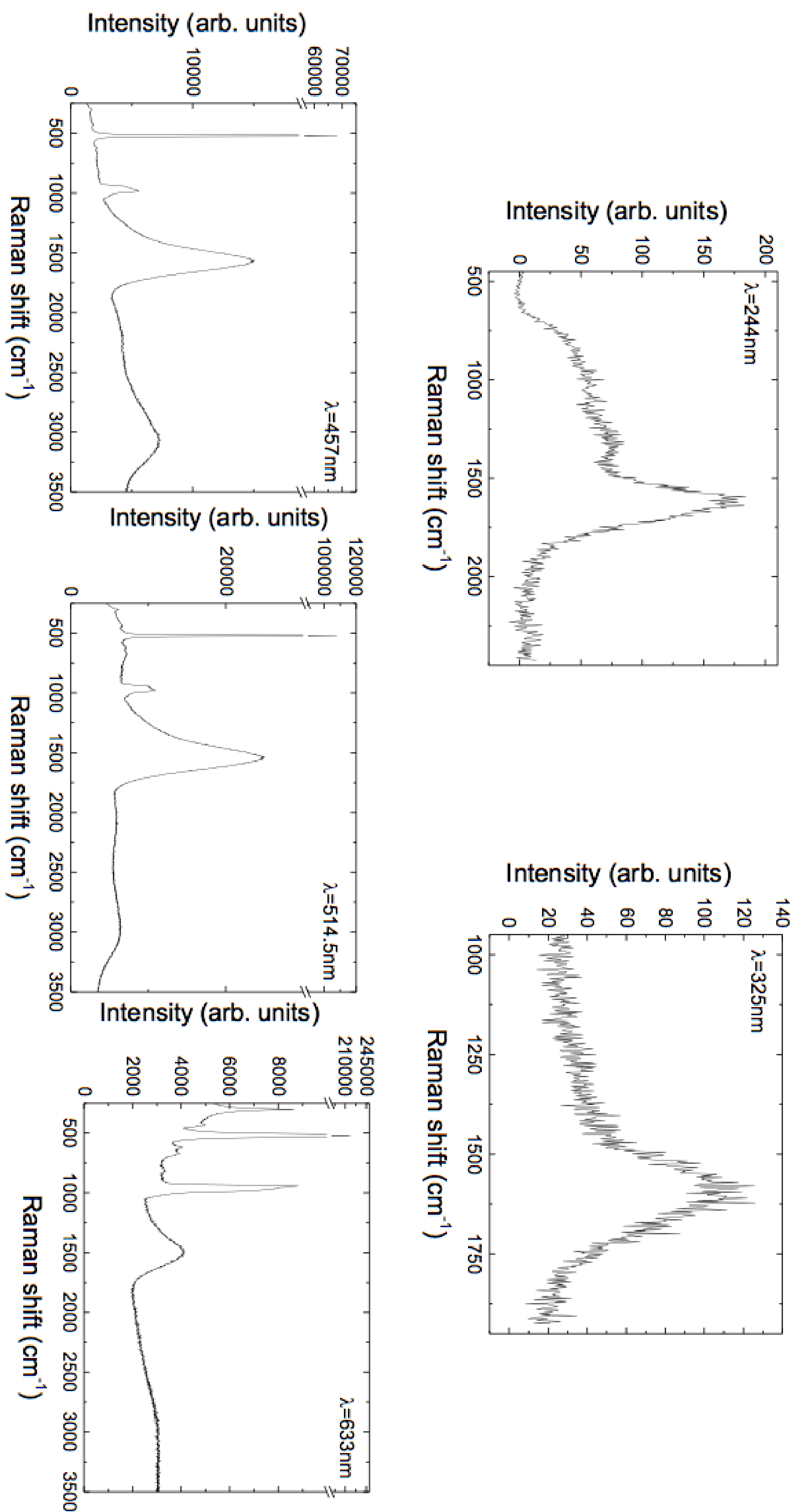
Figure A.8: Large lateral temperature gradients assist in confining the conductive filament laterally, and large temperature gradients at the filament-electrode interface aid the rupture of the filament.

Appendix B

Device Characterisation

B.1 Raman Spectroscopy

The multi-wavelength Raman measurements and analysis was carried out by Dr. A. K. Ott at Cambridge University under the auspices of the FP7 project CareRAMM.



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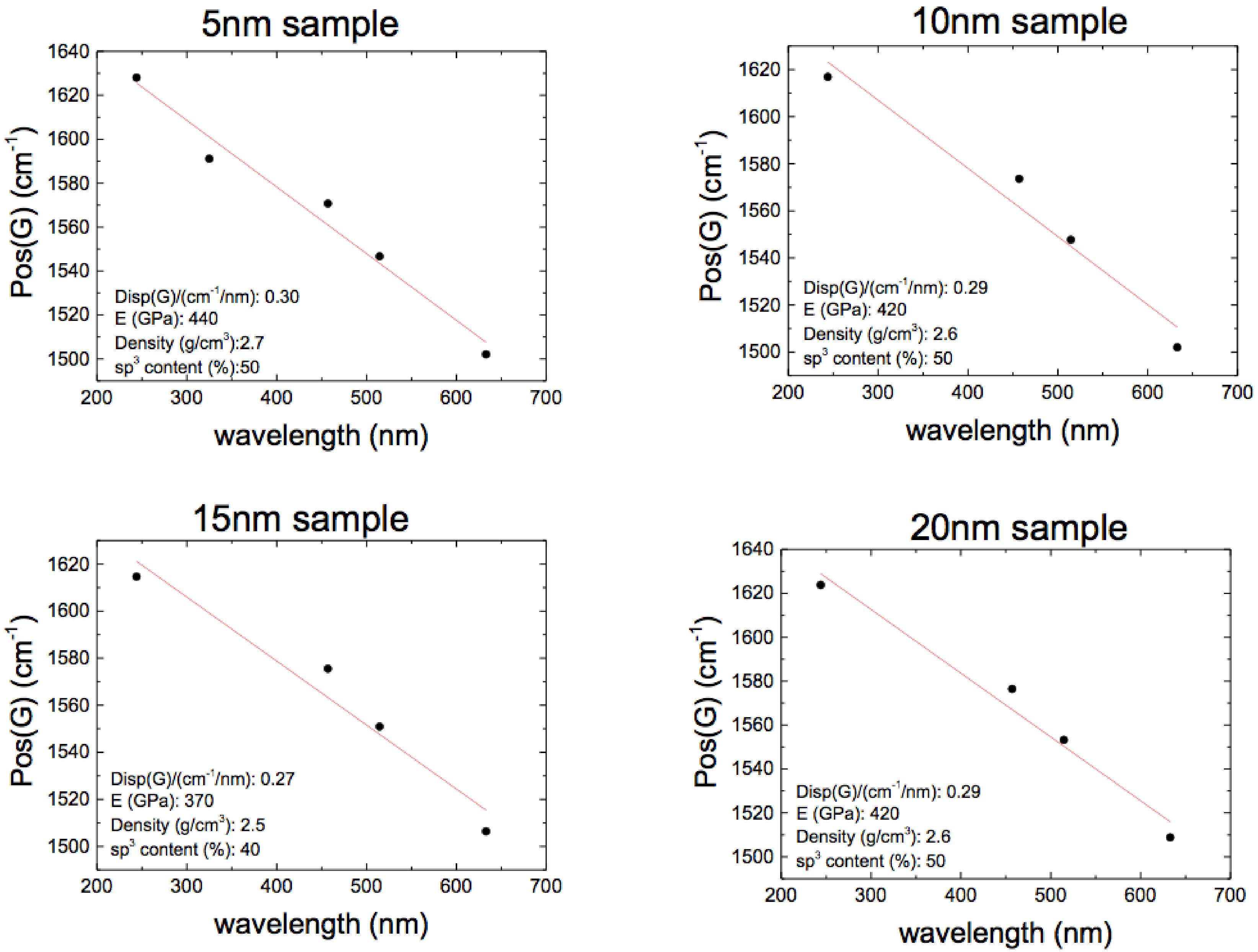


Figure B.2: G peak dispersion, Young's modulus, density and sp^3 content of 5 nm, 10 nm, 15 nm and 20 nm thick as-deposited ta-C films.

B.2 Cross-Bar Devices

Table B.1: Properties of ta-C cross-bar devices.

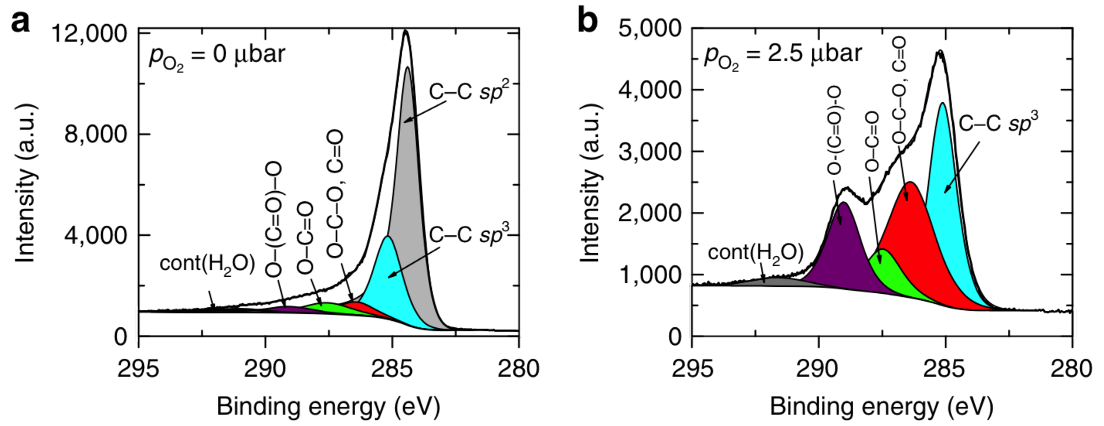
	Thickness	sp^3 content	Density	Young's Modulus
Batch 1	5 nm	0.5	2.63 g cm^{-3}	417 GPa
Batch 2	10 nm	0.7	2.87 g cm^{-3}	541 GPa
Batch 3	15 nm	0.6	2.71 g cm^{-3}	462 GPa
Batch 4	20 nm	0.7	2.92 g cm^{-3}	571 GPa

B.3 Confined-Cell Devices

Table B.2: Properties of ta-C confined-cell devices.

	Thickness	sp^3 content	Density	Young's Modulus
Batch 5	5 nm	0.5	2.66 g cm^{-3}	439 GPa
Batch 6	10 nm	0.5	2.62 g cm^{-3}	419 GPa
Batch 7	15 nm	0.4	2.53 g cm^{-3}	372 GPa
Batch 8	20 nm	0.5	2.62 g cm^{-3}	419 GPa

B.4 X-ray Photoelectron Spectroscopy (XPS)



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