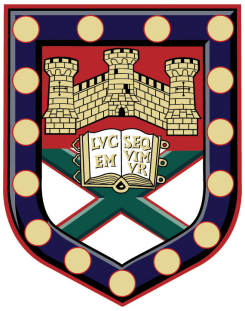
GROWTH AND OXIDATION OF GRAPHENE AND TWO-DIMENSIONAL MATERIALS FOR FLEXIBLE ELECTRONIC APPLICATIONS



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Dedicated to my family

ABSTRACT

The non-volatile storage of information is becoming increasingly important in our data-driven society. Limitations in conventional devices are driving the research and development of incorporating new materials into conventional device architectures to improve performance, as well as developing an array of emerging memory technologies based on entirely new physical processes. The discovery of graphene allowed for developing new approaches to these problems, both itself and as part of the larger, and ever-expanding family of 2D materials. In this thesis the growth and oxidation of these materials is investigated for implementing into such devices, exploiting some of the unique properties of 2D materials including atomic thinness, mechanical flexibility and tune-ability through chemical modification - to meet some challenges facing the community. This begins with the growth of graphene by chemical vapour deposition for a high quality flexible electrode material, followed by oxidation of graphene for use in resistive memory devices. The theme of oxidation is then extended to another 2D material, HfS_2, which is selectively oxidised for use as high-κ dielectric in Van der Waals heterostructures for FETs and resistive memory devices. Lastly, a technique for fabrication of graphene-based devices directly on the copper growth substrate is demonstrated for use in flexible devices for sensing touch and humidity.

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INTRODUCTION

1.1 GRAPHENE & 2D-MATERIAL ELECTRONICS

The technological implications of atomically-thin crystalline sheets could be wide-ranging and includes electronics, energy and sensing applications. The first demonstration of such materials began with graphene, which occurs naturally as a single layer of graphite. Arguably the most important contribution of graphene's discovery is that it was the first demonstration of a stable two-dimensional material, which has since led to the discovery of a host of other layered materials, that can be exfoliated down to just a few atomic layers[1]. Two-dimensional materials - that is to say one in which the bond-strengths along two-dimensions are similar and much stronger than along a third dimension[2] have since been shown to exhibit metallic, semi-conducting and insulating properties which form the material building-blocks of modern-day electronics. However, more than ten years since the discovery of graphene, a wide-reaching positive impact on society is still absent due to several roadblocks. These include developing cost-effective methods for production of high quality 2D materials, increasing the fundamental understanding of their rich physics and ultimately deciding its role in disruptive innovation. Even in the relatively brief history of graphene, there have been several approaches pursued to engineering the physical properties towards specific applications, which are now starting to be applied

across the ever increasing layered-material space. For example, chemical functionalisation of graphene has been demonstrated a viable way to tailor graphene through addition of molecules or ad-atoms to the graphene lattice. Of the various possible applications, the use for light-weight, flexible electronics shows real promise, owing to the outstanding mechanical properties of layered materials, which can be used independently or combined in the form of Van der Waals heterostructures. The issues facing scaling in conventional CMOS technologies means increased interest in developing technologies based on new materials or physical processes. Of the expansive field of CMOS-based devices, data storage represents an increasingly important and challenging area of development where the use of two-dimensional materials offers a new angle to approach such limitations.

1.2 CONVENTIONAL AND EMERGING NON-VOLATILE MEMORY TECHNOLOGIES

The non-volatile (permanent) storage of information is increasingly demanded in our data-driven society. As of 2007 the total amount of data storage humankind possessed was estimated to be 2.9×10^{20} bytes[3] and an IBM annual report from 2012 suggested an additional 2.5 billion GB of new data is generated each day[4]. As such, there is an ever increasing need for fast, high density, low power data storage. There are several types of data storage currently used in devices, as well as several emerging technologies suggested to replace them[5]. Non-volatile memory refers to that which maintains data when power is switched off, the most common example of which is 'flash' memory, as found in everyday USB-sticks and solid-state drives (SSDs). 'Flash' memory operates on the principle of local gating of a semiconductor by storing charges in a floating gate (e.g. poly-silicon) or charge-trap layer (e.g. nitride) and has proved hugely successful. However, as a conventional silicon CMOS technology, it is prone to the same scaling issues as any silicon transistor device, namely charge leakage resulting in decreased efficiency. The recent advent of 3D-Flash, that is the vertical stacking of flash memory arrays, is a solution to scaling, however there are other more conceptual limitations to 'flash' memory devices including power consumption, speed, cycling endurance. With these considerations in mind, research in the field of emerging non-volatile memory technologies is focussed on developing memory devices that not only out-perform flash with regard to speed, capacity, endurance and cost but also offer some additional functionality to complement other emerging technologies

such as neuromorphic computation and wearable electronics.

The use of pristine graphene and other layered materials in memory devices has to date mostly consisted of designing devices based on conventional principles of operation that rely on the trapping of charges in a floating gate or localised-charge trapping layer. There are several possible advantages to direct replacement of conventional CMOS materials with their two-dimensional counterparts including superior electrical properties, high transparency and mechanical flexibility making them ideally suited for implementing into a new generation of ever-more imperceptible electronics. However, there are more fundamental limitations to conventional device architectures including the high power consumption and gate leakage associated with ultra-thin dielectrics. As a result, there is tremendous effort going into designing new types of non-volatile memory devices based on different physical processes, solving the problems of conventional CMOS devices but with many of their own challenges. Of several memory technologies, resistive switching devices show strong potential owing to their high speed, low power and high scalability. An effect first observed by Hickmott in the 1960's[6], the reversible change in resistance in transition-metal oxides was quickly suggested as a future memory technology, with modern nano-scale characterisation techniques sparking renewed interest due to the ability to directly probe the physical origins of switching. The study of resistive switching in two-dimensional materials therefore offers an exciting avenue of research to pursue.

1.3 MOTIVATION FOR THIS THESIS

The motivation for this thesis began as an investigation into the use of graphene as a material for memory devices, both for an electrode and active/channel material. This begins with the growth of graphene by chemical vapour deposition, through oxidation and finally implementation into devices. While promising as an electrode, the use as a channel material in conventional transistor device architecture is limited by the absence of a band gap - resulting in poor on/off ratios of graphene FETs. Here, two solutions to this problem are explored; 1) Oxidation of graphene for use in resistive switching devices and 2) using graphene as an electrode in combination other 2D-materials such as layered insulators and semiconductors. Graphene oxide is a wide-gap semiconductor with a simple production route that make it ideal for flexible and printed electronics. Early demonstrations of graphene oxide resistive memory devices show promise, however the large number

of electrode configurations demonstrated made for a confusing picture with regards to the ultimate performance and mechanism of switching. As such the operation of graphene oxide-based resistive memory is developed and then combined with graphene electrodes, a step towards an all-carbon memory. Outside of the world of layered materials, hafnium oxide (HfO_2) represents a leading contender as a high-κ dielectric for gate-stacks and resistive switching material. Resistive memory devices based on HfO_2 show excellent performance in terms of speed, endurance, power consumption and environmental stability. The combination of such a material with 2D-materials may offer further improvements such as low power consumption, gate-tunable switching and ultra-thin device stacks. Of the layered material groups currently isolated, oxides are relatively untouched. Through oxidation of the hafnium-containing layered dichalcogenide, hafnium disulphide (HfS_2) resistive switching in 2D-material stacks is studied.

1.4 THESIS OUTLINE

In this thesis, the extraordinary properties of graphene such as its excellent mechanical flexibility and electrical conductivity are harnessed to pioneer new types of electronic devices. Furthermore, it is shown that the functionality of graphene and other 2D materials can be increased through chemical functionalisation. In particular, I focus on the oxidation of graphene and HfS_2 and demonstrate their implementation in both rigid and flexible devices. In chapter 2, the electronic properties of single layer graphene are outlined along with its limitations for using in electronics, specifically memory devices. This is followed by a review of the implementation of 2D materials in data storage based on conventional device architecture, with a focus on charge-trapping devices. Next I introduce some emerging non-volatile memory technologies, specifically resistive random access memory (ReRAM) and basic principles of operation are outlined. Chapter 3 details experimental methodology including chemical vapour deposition (CVD), Raman spectroscopy, chemical oxidation of graphene and hafnium disulphide, electrical characterisation and atomic force microscopy. Experimental results begin in chapter 4 with a study of the growth of large hexagonal graphene domains by chemical vapour deposition and the effect temperature on the growth of additional layers, followed by optical and electrical characterisation of graphene FETs. In chapter 5 graphene oxide thin films are implemented in mechanically flexible resistive memory devices. In chapter 6 the insulating properties of oxidised HfS_2

are investigated for use in devices and lastly, in chapter 7 CVD graphene is implemented into a flexible and transparent touch sensor and oxygen functionalised graphene humidity sensor.

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2

THEORETICAL CONCEPTS & LITERATURE REVIEW

2.1 INTRODUCTION

In this thesis the integration of graphene into resistive memory devices is investigated as a channel material and electrode. The unique electrical properties of graphene including its high room temperature carrier mobility and ambi-polar charge transport originate from its unique band structure. Experimentally, these properties can be probed using the field-effect transistor (FET) geometry, reflected in device resistivity. As such, I first outline the band structure and its relation to measurable channel resistance. While promising as an electrode with high optical transparency and mechanical flexibility, the limitations of pristine graphene as a channel material lie in poor ON/OFF ratio, limiting its use in transistors and convention charge trapping memory devices. One solution is through oxidation by chemical reaction or plasma doping, resulting in band-gap opening and larger ON/OFF ratios for memory devices. The layered transition metal di-chalcogenides are more suited to use as a 2D channel material owing to their semiconducting properties and can be combined with graphene in devices. As such, the operating principles and use of 2D-materials for non-volatile data storage are reviewed, based mainly on conventional charge-trapping

[†]Some of the ideas presented in this chapter have been published in: MF. Craciun, I Khrapach, MD Barnes, & S Russo *Properties and applications of chemically functionalized graphene.* Journal of Physics: Condensed Matter, **25** (2013) 423201

mechanisms. Fundamental limitations in conventional device architectures have led researchers to develop memory device based on entirely new physical processes. Resistive random access memory (ReRAM) is one of several emerging memory technologies poised to replace the state of the art, where the resistance of metal-insulator-metal sandwiches may be controlled. In this thesis, resistive switching effects based on 2D materials including graphene oxide and photo-oxidised hafnium disulphide are studied, and so the final part of this chapter is dedicated to an introduction to the principles of operation for such devices.

2.2 ELECTRONIC PROPERTIES OF SINGLE LAYER GRAPHENE

2.2.1 *Crystal structure & dispersion relation*

Graphene consists of a single layer of carbon atoms arranged in a honeycomb arrangement. The carbon atom has 6 electrons, consisting of a filled (2 electons) core $1s^2$ shell and partially filled (4 electrons) outer shell in the 2s and 2p states. Each carbon atom is covalently bonded to three neighbouring atoms through hybridisation of 2s, $2p_x$ and $2p_y$ orbitals, forming so-called σ-bonds. The remaining p_z electron orbital exists out-of-plane and forms the π-bands. It is the π-orbitals that give rise to the unique electronic properties, which can be calculated by applying the tight-binding approach[1]. The crystal structure of graphene is trigonal planar with a basis of 2 (A and B) as shown in 2.1(a) with lattice vectors;

$$a_1 = a\,(\,\sqrt{3}\,,\,0\,), \qquad ,a_2 = a\,(\,\frac{\sqrt{3}}{2}\,,\,\frac{3}{2}\,) \tag{2.1}$$

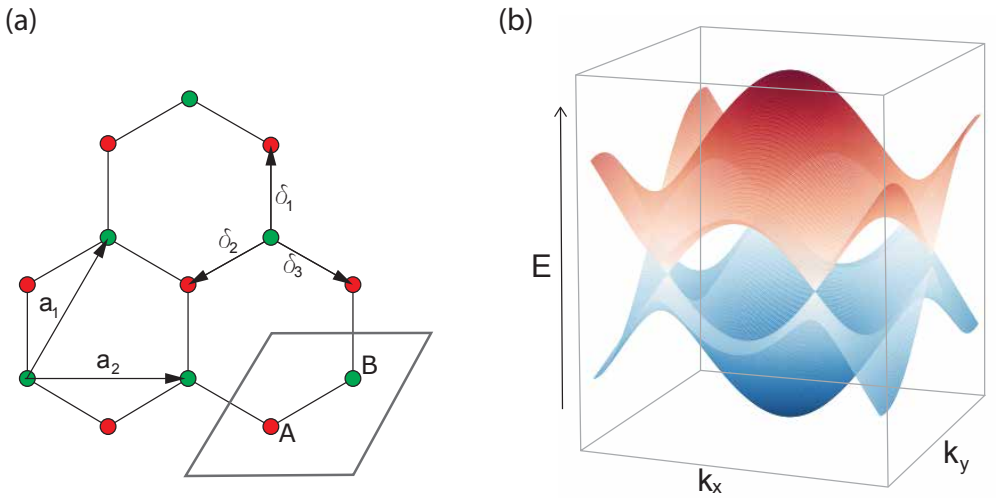

Figure 2.1: (a) The trigonal planar lattice of graphene with A and B sub-lattices where $\vec{a_1}$ and $\vec{a_2}$ are the primitive lattice vectors and $\delta_{1,2,3}$ are the nearest neighbour distances (b) resulting band structure of tight binding approximation for nearest neighbour hopping.

and corresponding reciprocal lattice vectors;

$$b_1 = \frac{2\pi}{3a}(\sqrt{3}, -1), \qquad b_2 = \frac{4\pi}{3a}(0, 1) \tag{2.2}$$

and inter-atomic spacing, $a = 1.42$ $\mathring{A}$. Following the nearest neighbour approximation of Wallace[2], when only hopping between A and B sub-lattices is considered the corresponding energy dispersion takes the form;

$$E(\vec{k}) = \pm t\sqrt{3 + f(\vec{k})} \tag{2.3}$$

where;

$$f(\vec{k}) = 2\cos\left(\sqrt{3}k_y a\right) + 4\cos\left(\frac{\sqrt{3}}{2}k_y a\right)\cos\left(\frac{3}{2}k_x a\right) \tag{2.4}$$

The dispersion relation is plotted in Figure 2.1(a) for t = 2.97 eV. The valence and conduction bands touch at E = 0, making single-layer graphene a gap-less semiconductor (or equivalently semi-metal)[3]. Expansion around the K and K' points yields linear bands with E = $\pm\hbar\upsilon_F|k|$ where $\upsilon_F \sim 10^6$ m s^{-1}. The resulting density of states (DOS) for monolayer graphene;

$$D(E) = \frac{g_s g_v |E|}{2\pi\hbar^2\upsilon_F^2} \tag{2.5}$$

accounting for spin (g_s=2) and valley (g_v=2) degeneracy yields;

$$D(E) = \frac{2|E|}{\pi\hbar^2\upsilon_F^2} \tag{2.6}$$

and can be re-written in terms of carrier density (n);

$$D(E) = \frac{dn}{dE} = \frac{2n}{k\hbar\upsilon_F} \tag{2.7}$$

which can be substituted into the Boltzmann conductivity;

$$\sigma = \frac{e^2\upsilon_F^2}{2} D(E)\tau(E) \tag{2.8}$$

where τ is the scattering time. Re-arranging we arrive at the Drude conductivity;

$$\sigma = ne(\frac{e\upsilon_F\tau(E)}{k\hbar}) \tag{2.9}$$

with charge carrier mobility, $\mu = \frac{e\upsilon_F\tau(E)}{k\hbar}$. For graphene FETs the convention is to measure the channel resistance (voltage drop) which is related simply by considering device geometry (length/width) where the channel resistance, $R = \frac{L}{W\sigma}$. In practice, modulation of carrier density is achieved through electrostatic doping using conventional SiO_2/Si^{++} substrates or polymer electrolytes, and is detailed further in the following

chapter.

2.2.2 *Band gap opening in graphene*

The problem of the absence of a band gap in graphene limits the use as a channel material in resistive memory devices and has been approached from a number of different angles, either by electrical manipulation of the pristine material or by chemical functionalisation. First, it has been shown that by breaking the symmetry of the A and B sub-lattice results in band-gap opening in few-layer graphene[4]. This has been demonstrated experimentally using double-gated transistor based on few-layer graphene (e.g. AB bilayer[5] and ABC trilayer[6]), where the Fermi-level of the top and bottom graphene layers can be tuned independently. However, the size of the band-gap in such devices limits its use to far-infra-red applications. A second and more versatile approach is through chemical functionalisation, which involves modification of the graphene lattice by adding functional groups or ad-atoms which directly effect the band structure. This has been demonstrated for a number of chemical species including oxygen[7], hydrogen[8] and fluorine[9], where the change from sp^2 to sp^3 hybridisation results in band gap opening.

Of the several approaches to band-gap opening, in this thesis I utilise chemical functionalisation, specifically oxidation, first of graphene and later of HfS_2. Graphene oxide (GO) is formed through covalent bonding of oxygen-containing functional groups onto the graphene sheet. The oxidation of graphite is well understood with production possible at industrial volumes. This has since been extended to graphene, where chemical analysis has revealed the presence of several functional groups including carbonyl, carboxyl, epoxy and hydroxyl groups present on the graphene sheets. The addition of functional groups results in a significant increase in sp^3 hybridisation of the material, yielding it insulating with a predicted band gap of 1.7-2.4 eV[10]. Further, the presence of functional groups also results in significant buckling of the once layered graphene sheet resulting in large amounts of disorder. As such the electrical transport in GO typically occurs by hopping conduction between highly conductive sp^2 clusters with measured values of sheet resistance on the order of 10^9 Ω[11;12]. Controlling the oxygen groups in GO has yielded several potential applications. The first is as a top-down approach to industrial production of graphene, where removal of oxygen groups by chemical or thermal reduction allows for some, if limited, recovery of graphene's electronic properties such as gate-tunable con-

ductivity[13]. It has also been shown that the oxygen functional group in GO thin films can be reversibly controlled using high electric fields, which allows for reversible control of conductivity on the device level and forms the basis of resistive switching memory devices, explained in detail below.

2.2.3 *Pristine graphene for non-volatile memory devices*

In the simplest terms, a non-volatile memory device is one that stores one or more bits of information and retains the information when any external bias (source-drain and gate) is disconnected. Several device characteristics are used to measure performance of non-volatile memory devices which are; write/read/erase speed, memory window (or ON/OFF ratio), cycling endurance, retention time and operating power. Write/read/erase speed is simply the time taken to achieve any given memory process and often defines the position in the memory hierarchy (see below). Device speed is closely linked to operating energy, which can be defined as operating power (P = IV) $\times$ voltage pulse duration, where the voltage pulse is used to SET or RESET the device. With the current trend of rapidly increasing data production rate, it is vital that future memory devices operate with the smallest possible write/read/erase energy. Memory window refers to the measurable difference between two or more data levels, often the measured drain current for a set voltage bias or resistance for ReRAM devices. The larger the memory window the simpler the data level is to read and is often quoted as an order of magnitude (10^{X}). Cycling endurance describes the number of times a device/element may be written, read and erased before failure, one limitation of conventional Flash-memory devices. Lastly, retention time is the duration over which the stored data is retained. The retention time is another deciding factor in the position within the memory hierarchy, depending on its long-term stability.

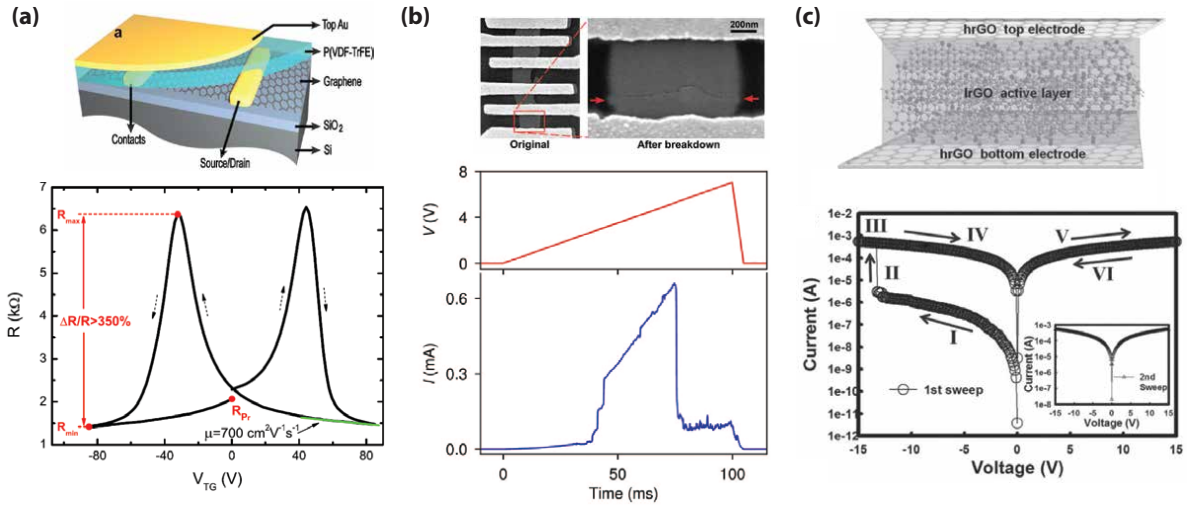

Figure 2.2: (a) Device schematic and typical gate response of a ferroelectric-gated graphene FET reported by Zheng et al.[14](b) SEM image and typical current-voltage cycle of a graphene-based physical switch reported by Standley et al.[15] and (c) write-once-read-many resistive memory device based on all-reduced graphene oxide layers of Liu et al.[16]. All panels adapted from the referenced works.

Predominantly the use of graphene in 2D-material-based electronics is as an electrode material owing to its high performance as a transparent, flexible and high mobility electrode, where it may be combined with other layered insulators (e.g. hBN) and semiconductors (e.g. MoS_2 & WS_2). A review of such devices is covered in the following sections. There are relatively few demonstrations of graphene as a channel material for memory devices owing to the low ON/OFF ratio of graphene FETs associated with semi-metallic electrical properties which makes it hard to distinguish between data levels. Figure 2.2(a) shows several notable works where graphene is incorporated into memory devices. Panel (a) Shows a device schematic and characteristic operation of ferroelectric graphene-RAM reported by Zheng et al. In such devices the memory level is measured as the graphene-channel resistance where the high (resistance) is taken near the charge neutrality point where the DOS is low (V_{CNP}), and the low far away where the carrier density is high. This yields an ON/OFF ratio of 3.5-times, lower than is typically required in integrated devices to achieve easily distinguishable data levels. The memory effect in such devices is attained through doping modulation by tuning the dipole orientation of a ferroelectric

gate material[14]. Figure 2.2(b) shows a planar resistive memory device based on a nanometre gap in a graphene channel. Here the graphene channel behaves as a physical switch, controlled by dissipation of relatively large electrical currents[15]. Application of large voltage directly to the channel results in formation of a nano-scale gap and an effectively open circuit (highly resistive) state. The switch can then be set to a conductive state by a subsequent electrical pulse, ascribed to the electric field driven migration of atomic carbon bridging the gap. Figure 2.2(c) shows a resistive memory device based on lightly reduced-graphene oxide channel material and highly reduced graphene oxide electrodes of Liu et al. The devices shows resistive memory operation over a single cycle, where the memory effect is attributed to permanent reduction of the GO active layer upon sufficient voltage bias[16]. While useful in some applications, this type of device is severely limited by the fact that it cannot be repeatedly written, read, erased.

2.3 CONVENTIONAL AND EMERGING NON-VOLATILE MEMORY DEVICES

2.3.1 *Floating gate & charge trapping Flash*

There are several types of data storage currently used in state-of-the-art device, as well as several emerging technologies suggested to replace them. The most common example of non-volatile data storage is flash memory, as found in everyday USB-sticks and solid-state hard-drives. 'Flash' memory operates on the principle of local gating of a semiconductor by storing charges in a floating gate (e.g. polycrystalline silicon) or charge-trap layer (e.g. nitride), and as such is prone to the same scaling issues as any silicon transistor device, namely charge leakage resulting in decreased efficiency. One may argue that the advent of 3D-Flash, that is the vertical stacking of flash memory arrays, is a solution to scaling, however there are other more conceptual limitations to 'flash' memory devices including power consumption, speed, cycling endurance and retention time. Incorporating 2D materials into flash-based memory devices has been suggested as a solution to several of the shortcomings. Figure 2.3(a) shows device structure and principle of operation for the a conventional flash memory cell.

*The term 'Flash' memory originates from the method in which entire blocks of memory cells can be erased simultaneously by the application of a voltage pulse (*flash erasure*)

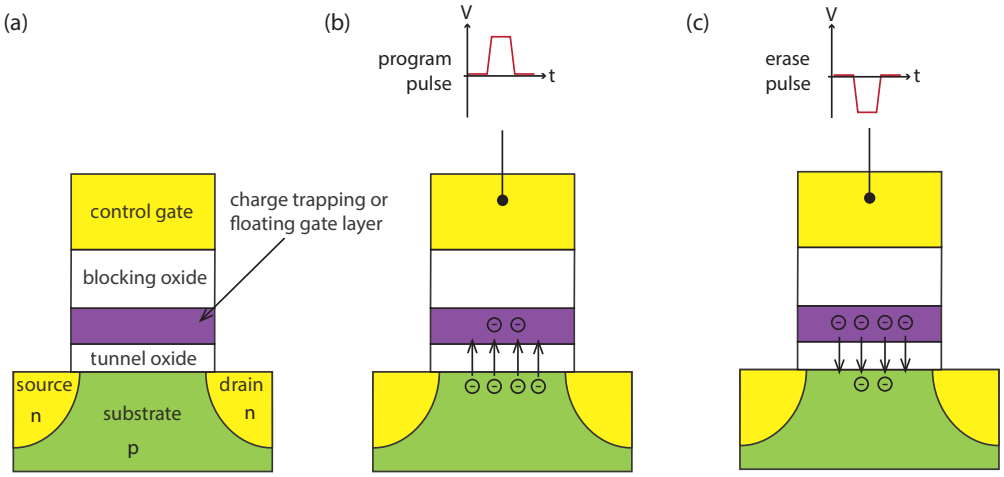

Figure 2.3: (a) Schematic representation of a conventional Flash memory cell, with either floating gate or trapping charge storage layer. Illustrations of the operating principle is shown for (b) programming and (c) erasing where charges are injected into the charge storage layer by Fowler-Nordheim tunnelling.

Conventional floating gate memories employ a conductive charge storage layer (e.g. polycrystalline silicon) where, upon application of a positive gate bias, charges are injected from channel to gate by hot electron injection and Fowler-Nordheim tunnelling. When the gate voltage is removed the electric field due to presence of stored charges results in a shift in threshold voltage of the channel; $\Delta V_{th} = \frac{-d_{tunnel} \cdot Q}{\varepsilon_{tunnel}}$. For a well defined read voltage (V_{read}) the measured drain current corresponds to a memory level. Charge trapping layers, on the other hand, are insulators (e.g. nitrides) and as such the stored charges are localised. For these devices injection of electrons through the tunnel oxide is by Fowler-Nordheim tunnelling, and subsequent movement of charge through the charge trap layer by Poole-Frenkel emission. Erasure occurs either by tunnelling of electrons back through the oxide or neutralisation of localised electrons by hot injection of holes from the channel.

2.3.2 *2D materials in conventional memory devices*

Several memory device architectures have been demonstrated using 2D-materials. Table 2.1 shows a summary of 2D materials implemented in the various layers and their associated performance criteria. The most commonly used 2D materials are MoS_2/black

Channel material	Tunnel dielectric	Charge storage	ON/OFF ratio	Cycling endurance	Retention time (s)	Ref
MoS_2	-	Plasma-treated MoS_2	10^3	100	2×10^3	[17]
SLG	-	Si_3N_4	7.3	-	10^3	[18]
Si	SiO_2	SLG, FLG	6V*	-	3×10	[19]
MoS_2, SLG	hBN	SLG, MoS_2	10^4	-	1.5×10^3	[20]
MoS_2	Al_2O_3	HfO_2	10^4	120	10^4	[21]
MoS_2	HfO_2	Metallic nano-crystals		-	2×10^3	[22]
BP	hBN	MoS_2		50	10^3	[23]
MoS_2	hBN	SLG	10^9	10^5	10^4	[24]
BP	Al_2O_3	HfO_2	10^2	120	10^5	[25]
BP	-	Al_2O_3	10^4	100	10^3	[26]
BP	Al_2O_3	BP	10^3	-	10^3	[27]
WS_2	hBN	FLG	10^3	-	10^4	[28]

Table 2.1: Summary of the incorporation of 2D materials in floating-gate and charge trapping flash memory devices with performance data. Data for this table is taken from the text and figures of the referenced articles. *Hong et al. measure the memory window as in a conventional silicon FET as a change in threshold voltage, $\Delta V_{th} = 6$V.

phosphorous (BP) for channel, hBN for the tunnelling layers and FLG/MoS_2 for floating gate. Of the devices presented, several show similar performance to that of conventional flash; good memory level retention, large memory window and high cycling endurance, as well as some demonstrations of flexible/stretchable devices. Of the works published, three particularly notable examples are presented in Figure 2.4. Panel (a) shows a charge-trap memory device based on a BP channel reported by Tian et al. The top-gate dielectric composed of Al_2O_3 also acts as both a blocking layer and charge trapping layer with the typical transfer curve plotted below for sweeping the top-gate voltage. Such a device is akin to a conventional charge-trap memory device where charges are localised within traps in the insulating oxide, combined here for the first time with the high mobility ambipolar transport properties of BP[26]. Panel (b) shows the charge trapping memory devices of Sup Choi et al., the first thorough demonstration of a 2D charge trapping memory device. Van der Waals heterostructures consisting of MoS_2/hBN/graphene layers enable efficient tunnelling of carrier between MoS_2 and graphene in which they are stored, akin to floating-gate devices[20]. Panel (c) shows the most recent work of Vu *et. al*, again based on a MoS_2/hBN/graphene stack, but the two-terminal operation is a key step-forward towards simplified, gate-free devices. The memory effect is again akin to floating-gate technology, only this time the injection of charges onto the floating gate is achieved using the drain electrode, thanks to a subtle change in device architecture[24].

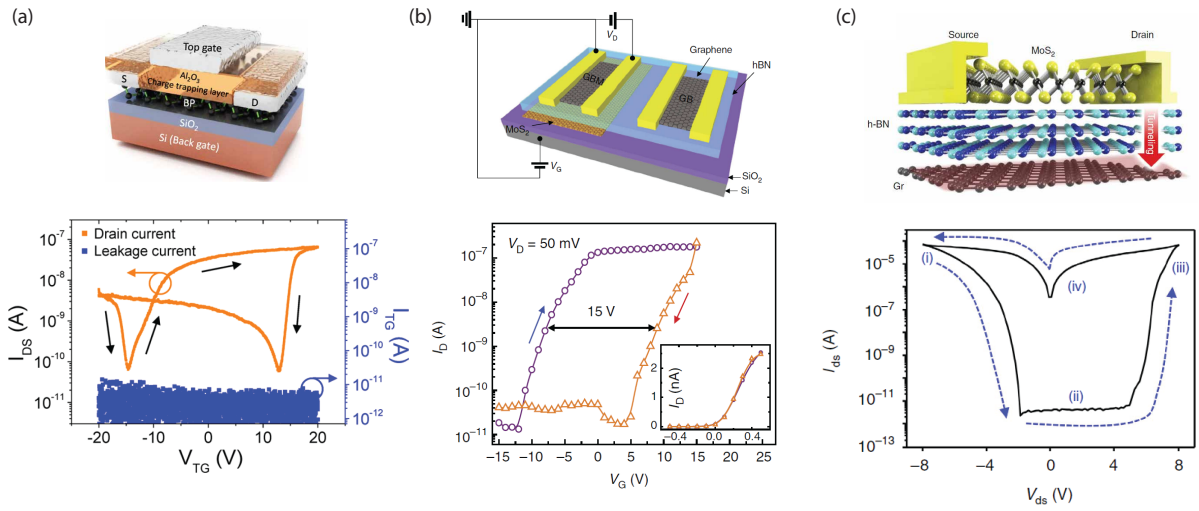

Figure 2.4: (a) Device structure of a charge trapping memory based on BP active channel and Al_2O_3 charge trapping and below the associated memory effect of Tian et al.[26] and (b) device schematic of graphene-hBN-MoS_2 charge-trapping devices of Sup Choi et al. with the associated memory effect plotted below[20]. (c) device schematic of two-terminal floating gate devices of Vu *et. al*, where charges are injected directly from the drain electrode to charge trapping graphene layer[24].

2.3.3 *Emerging non-volatile memory technologies*

Aside from direct replacement of the materials in current devices, several new technologies are emerging, both direct replacements of flash as well as entirely new approaches to non-volatile data storage. To visualise the scope of data storage device, the commonly referred to data storage hierarchy of today is outlined in Figure 2.5(a). Current technological limitations result in a large gap in performance between dynamic memory (e.g. DRAM) and non-volatile storage (e.g. HDD). Here we refer to memory as used to store information required immediately, which requires fast operation at the expense of low capacity with high cost. Storage on the hand is used to store data, e.g. HDD and tape. Storage is non volatile and high capacity, but lacks speed required to be useful for computation. Within the conventional von Neumann architecture of computing, the currently most sought after technology is a storage class memory (SCM). An SCM is one that effectively bridges the gap between memory and storage, providing both fast write/read times and large storage

capacity. Beyond the typical von Neumann computation is neuromorphic computation, designed to mimic synapses in the brain. In such devices singles elements that may be used for either memory and computation would require a dynamic device for which the function may be altered electrically. The extensive potential applications mean a great deal of both public and private research into the next 'flash' memory is under way. Until recently, future memory technologies, both emerging and prototypical were periodically reviewed as part of the International Roadmap for Semiconductors, presented in Figure 2.5(b).

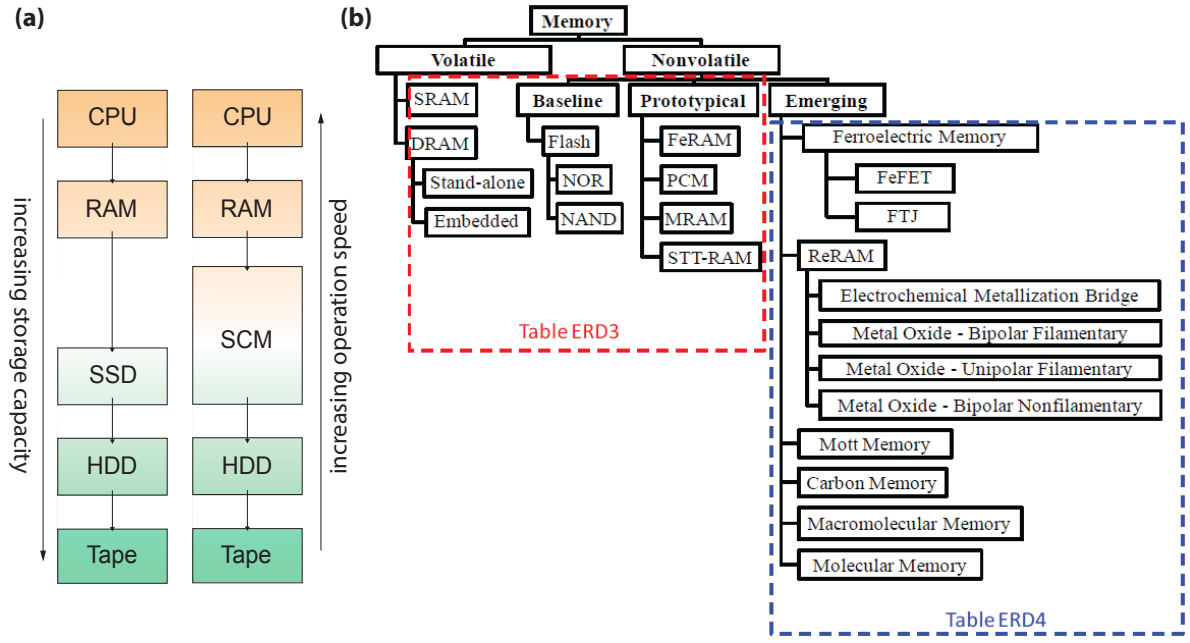

Figure 2.5: (a) Storage hierarchy for (left) conventional data flow with the position of SCM shown (right). (b) ITRS breakdown of conventional, prototype and emerging memory technologies adapted from[29].

2.3.4 *Resistive switching memory devices)*

Resistive switching memory operate on the principle of resistive switching, which describes the abrupt change in resistance observed in a material induced by an applied voltage/current. The effect was first observed by Hickmott in thin metal-insulator-metal sandwiches for various transition metal oxides[30] and shortly after by Gibbons et al. in NiO[31]. Since these early observations several distinctions have been made between re-

sistive switching devices based upon the operating characteristics. Following these early measurements, the devices were suggested for use in non-volatile data storage, where each resistance level corresponds to a data level. Since then resistive switching has been observed in several groups of materials including transition metal oxides, perovskite oxides and phase change alloys and much has been learned about the underlying physical mechanisms. While the principle of operation for resistive switching devices is highly dependent on the specific structure and variation of oxide material chosen, there are several unique properties that allow classification of the devices[32;33]. The first classification of resistive memory devices is according to the polarity of operation. Devices that may be switched between the high resistance state (HRS) and low resistance state (LRS) using a single polarity are termed unipolar. Bipolar devices require two opposite polarities for the SET and RESET operations and tend to operate based on an alternative principle. Figure 2.6 shows a typical metal-insulator-metal sandwich device structure used for ReRAM along with the current-voltage characteristics of both unipolar and bipolar operation. The physical mechanism behind the resistive switching typically dictates the type of operation, this is often a combination of several effects which makes for a complex model and is still an area of great debate within the community. It is noteworthy that resistive switching effects have been observed in the same materials used for conventional floating gate devices including polycrystalline silicon and silicon nitride (Si_3N_4). Chand et al. report conductive bridge resistive switching in polycrystalline silicon with 10^4 ON/OFF resistance, 10^6 cycling endurance and 10^4s retention time[34]. Silicon nitride-based devices have also been investigated, Kim et al. report 5nm-thick Si_3N_4 layers which exhibit 10^5 ON/OFF ratio with low power operation owing to the use of SiO_2 tunnelling layers[35].

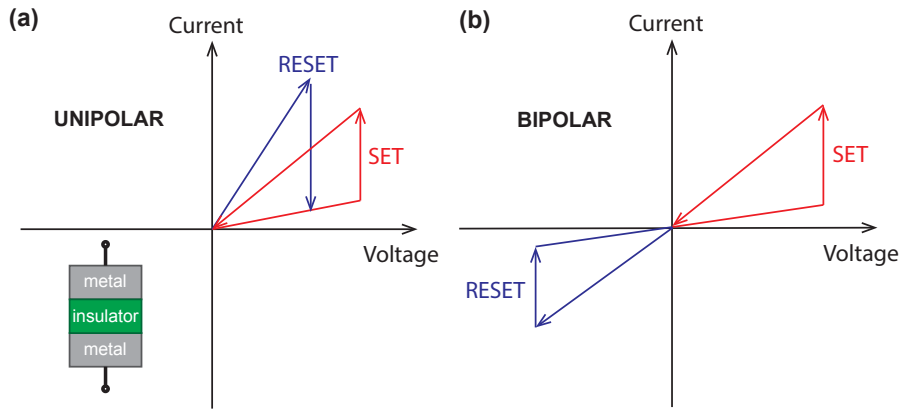

Figure 2.6: Typical current-voltage dependencies for switching in (a) unipolar and (b) bipolar operation. Inset in (a) shows the typical metal-insulator-metal sandwich device structure

In this thesis I focus on only bipolar resistive switching, which was observed for a variety of electrode configurations. All but one of the configurations use an asymmetry between top and bottom electrode material, which can assist in understanding the observed switching mechanism. Two switching materials are investigated in this thesis. Graphene oxide is used with a reactive (oxidising) top electrode (titanium and aluminium) and and inert bottom electrode (platinum and few-layer graphene). The second is hafnium oxide (HFO_x) which is again used with a reactive top electrode (chromium and titanium) and an inert bottom electrode (gold and graphene). In bipolar resistive the reactivity of the top electrode results in redox reactions with the active layer acting as a reservoir for oxygen ions and functional groups. It has been shown previously that bipolar operation is often due to the effect of reversible oxidation/reduction of the top electrode and active layer. The migration of either oxygen or metal atoms is induced through electro-migration or thermally-induced diffusion. Understanding the electrical transport in resistive switching metal-insulator-metal devices is useful in understanding of the mechanism of switching, this can be applied through temperature dependent measurements of the element resistance, where conducting filament formation in the LRS typically shows a metallic temperature dependence. However, elucidating the precise mechanism of switching is not trivial, and often requires high-resolution cross-sectional transmission electron microscopy and chemical analysis on the nano-scale as the conducting filaments often responsible for the LRS can be comprised of just a few atoms.

2.3.5 *Resistive switching of graphene oxide*

Several groups have demonstrated resistive switching in GO thin films, with large variations in performance and switching mechanisms reported. For a clear understanding of the switching mechanism, literature on resistive switching in graphene oxide thin films can be compared to gain an insight into the physical mechanism responsible. For implementation of reliable and commercially viable GO memory technologies, the precise mechanism of resistive switching should be understood. To date, this precise understanding has been lacking due to the plethora of GO memory materials and device structures investigated. The mechanism of switching has been ascribed to metal filament formation, oxygen ion migration, reduction/oxidation and diffusion of carbon atoms. While the switching behaviours observed include bipolar, unipolar, with forming and without forming. This makes for a muddled picture when reviewing the literature. Most examples of highly repeatable bi-polar resistive switching in GO is usually observed in devices with at least one reactive electrode, where the difference in affinity for oxygen mediates a repeatable exchange of oxygen between GO and the reactive metal electrode (of interface metal-oxide layer). Further, the effects are often a combination of physical processes, for example when using a reactive metal electrode (with high affinity for oxygen) an amorphous insulating layer is formed upon deposition as a result of oxygen migration. The resistive switching behaviour is due to diffusion of oxygen in and out of this amorphous layer upon application of a voltage, leaving behind conducting filaments in the amorphous layer.

The most thoroughly investigated electrode combination for GO thin films is Al-GO-Al, with several groups observing bipolar resistive switching with good retention times, cycling endurance and repeatability. Jeong et al. demonstrate a flexible, bipolar Al-GO-Al device with 10^3 ON/OFF ratio, retention time of 10^4 s and cycling endurance of 100 cycles[36]. A follow up work by Kim et al. investigates the switching mechanism in similar structures using high-resolution cross sectional transmission electron microscopy and observe the formation and and rupture of conductive aluminium filaments in the top interfacial layer with the respective SET and RESET processes as shown in Figure 2.7[37]. In these devices the interface layers form due to the high reactivity of the aluminium resulting in the formation of sub-stoichiometric Al_2O_{3-x}. Upon application of a negative bias to the top electrode the electric fields acts to force oxygen ions from the interface layer

into the GO film, leaving behind conductive aluminium filaments of low resistance (LRS). The device stays in the LRS until ample positive bias is applied to the top electrode to drive the oxygen ions back into the interface layer, resulting in oxidation of the conducting filaments and return to the HRS. The authors also note the importance of the bottom interface layer in preventing permanent breakdown of the devices. While the authors do not go into detail, the Al_2O_3 layer likely acts to limit the current and subsequently the size of the conducting filaments formed. In such a device the resistive switching is driven local formation of conducting filaments upon migration of oxygen ions away from the interface.

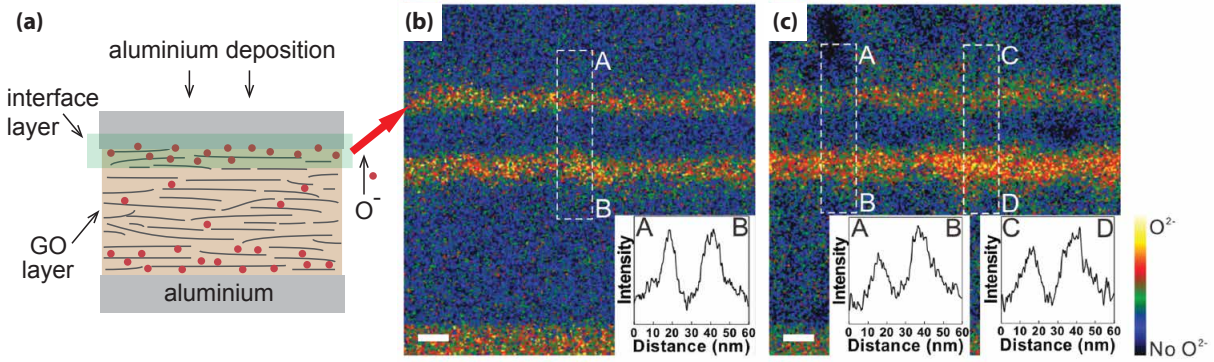

Figure 2.7: (a) Illustration of interface layer formation upon deposition of aluminium on a graphene oxide thin film. Panels (b) and (c) are cross-sectional TEM images from the work of Kim et al. showing oxygen elemental maps for (b) pristine state (HRS) and SET state (LRS)[37].

For inert electrodes such as Pt, Au and Pd the resistive switching is often unipolar and with limited cycling endurance. In such cases the switching can be ascribed to the irreversible reduction of the GO thin film. This has been demonstrated for lateral Au-GO-Pd devices[38] and for vertical Au-GO-Pt devices[39]. In both cases the switching observed was akin to that of write-once-read-many (WORM) memory with the virgin (oxidised) GO providing HRS and the SET (electrically reduced) GO providing the LRS (shown in Figure 2.2(c)). Similar single write devices have also been observed for highly-reduced GO (hrGO) electrodes with lightly-reduced GO (lrGO) active material[16]. Such devices show very large $V_{SET} \sim$ -13 V, with the switching from HRS to LRS due to the bias induced reduction of the GO film generating increased sp^2-fraction within the film and subse-

quently high conductivity. The benefits of an all-reduced-GO device is flexibility - where all components of the device show high mechanical flexibility. Lastly, resistive switching of GO thin films has also been ascribed to the reversible reduction/oxidation of the film itslef. In such cases the role of water in resistive switching has also been investigated, and is important to consider when using conductive-AFM for electrical contact, due to the inherent water meniscus that forms on the charged tip during switching. In such cases the mechanism of switching is attributed to the electrochemical reduction/oxidation of the GO film in the vicinity of the tip[40;41], where the size of the meniscus can be few μm for high relative humidity. In such experiments the top electrode may be considered the combined tip/meniscus system, markedly different from a metal-GO-metal structure presented in the following chapters due to the size of the top electrodes used. Our recent investigation into resistive switching of hybrid titanium-GO devices suggest an exchange of oxygen between the titanium and GO, which was simulated using molecular dynamics, shown in Figure 2.8.

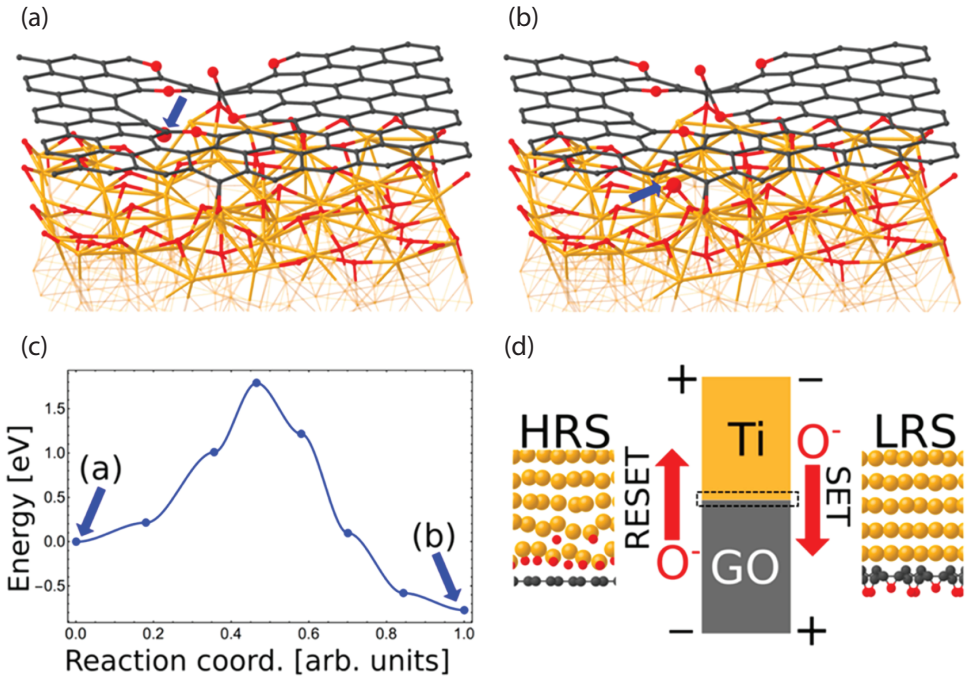

Figure 2.8: Molecular dynamic simulation of Ti-GO showing (a) initial and (b) final position of oxygen in reversible transfer across the interface. (c) minimum energy pathway for the exchange (d) proposed set and reset process for the Ti-GO system. All panels adapted from[42].

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2.3.6 *Resistive switching in hafnium oxide*

Compared to GO, resistive switching effects in the transition metal oxides (TMOs) is more well- established. Of these, hafnium oxide is among the most promising active materials for ReRAM devices[33]. Performance of hafnium oxide-based ReRAM is among the high reported and is well summarised by the group of Philip Wong[43]. Fully optimised CMOS-integrated HfO_x device stacks exhibit upto 5 ns switching speeds[44], 10×10 nm^2 cell area[45], 10^3 ON/OFF ratio and endurance over 10^6 cycles[46]. Also, recent reports even detail integration into 3D-CMOS architectures.

Turning to the mechanism of resistive switching, bipolar resistive switching may be achieved using asymmetric electrode material and originates from the migration of oxygen in and out of the HfO_x. As such, a defect-rich sub-stoichiometric oxide tends to give the optimum switching characteristics. While TMOs are perhaps the most well-researched,

a single concrete model to describe the resistive switching is still lacking. Early devices showed that including a reactive metal top-capping layer, strips oxygen from the HfO_x leaving many oxygen vacancies and acting as an oxygen reservoir for the subsequent switching cycles. In these structures, bipolar resistive switching mechanism is understood to be driven by the reversible migration of oxygen within the HfO_x layer resulting in the formation of metallic filaments with high electrical conductivity, as illustrated in Figure 2.9(b). For some devices based on HfO_x a forming step is required before any repeatable resistive switching is induced. This forming step consists of the application of a large voltage bias (+) to the top electrode that strips oxygen ions (-) from the HfO_x active layer. For a reactive top electrode, the generated oxygen ions are stored by means of oxidation of the metal electrode material at the top electrode/HfO_x interface. Commonly used reactive metal capping layers include titanium and tantalum, chosen for the large number of available oxidation states[47]. As such, the platform of hafnium oxide offers an interesting avenue of research when combined with 2D materials such as graphene electrodes for development of flexible ReRAM based on HfO_x.

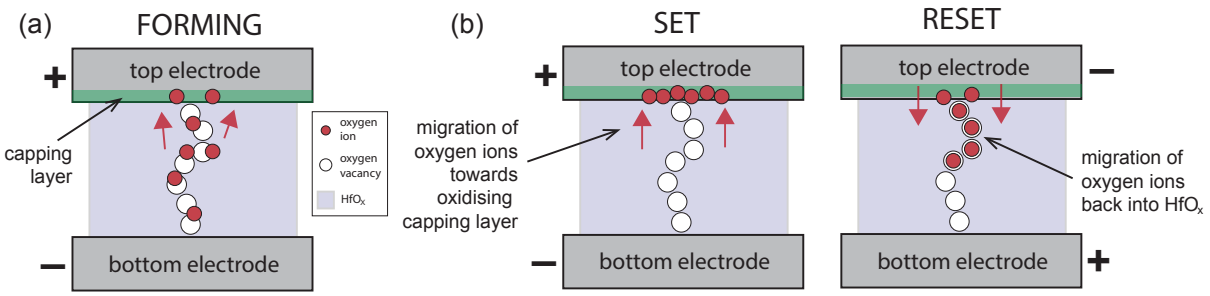

Figure 2.9: Illustration of oxygen ion migration in (a) forming, (b) set and (c) reset processes in HfO_x-based ReRAM.

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3

EXPERIMENTAL METHODOLOGY

This chapter details the experimental methodology used throughout the thesis, focussing on the growth, fabrication and characterisation of graphene/thin film devices and methods of functionalising graphene and TMDCs. First the method for growth of graphene by chemical vapour deposition is outlined followed by the various techniques for functionalising graphene including wet-chemical oxidation, plasma oxidation and photo-assisted oxidation. Next, the various characterisation techniques used throughout are explained, which includes Raman spectroscopy, atomic force microscopy and electrical measurement of graphene FETs and resistive memory devices.

3.1 CHEMICAL VAPOUR DEPOSITION

Chemical vapour deposition of graphene is perhaps the most viable technique for large scale production of high quality graphene films. Figure 3.1 shows a simplified schematic of the home-built furnace system used for CVD growth. Such a system is designed for both atmospheric and low-pressure growths. The growth substrate chosen is either copper foil (25 μm thick, 99.999%) for standard growth or for melted copper a thick copper foil (250 μm thick, 99.999%) is loaded onto a tungsten support foil. Tungsten acts as a wetting support for the molten copper, as it does not wet to the quartz tubes/boats. For all growths the same pre-growth procedure is followed. First, tube is pumped to a

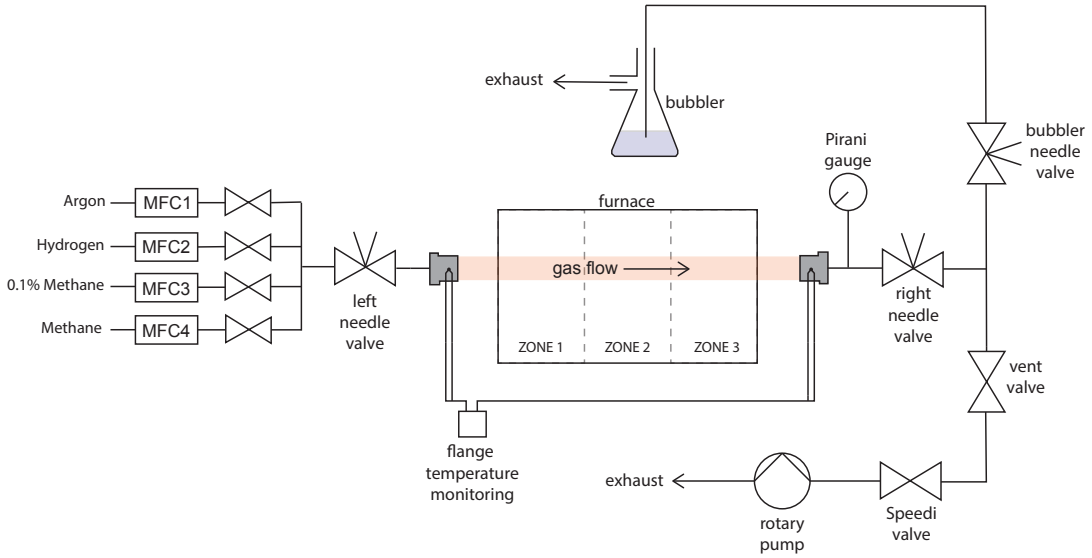

Figure 3.1: Simplified schematic of home-built CVD system for low-pressure and atmospheric-pressure CVD of graphene.

base pressure $\sim$ 20 mTorr the tube is brought to atmospheric pressure by back-filling with argon followed by purging for 15 minutes, this ensures minimal oxygen/moisture in the tube which can effect the growth. Melting and re-solidification of copper has been demonstrated as a simple technique to grow large single crystal graphene domains without the necessity for any pre-treatment of the copper foils as first developed by Moshin *et. al*[1]. For growths on re-solidified copper the same pre-treatment is used, where the temperature is ramped above the melting point of copper (1084 °C for p = 1 atm) for 30 minutes in a reducing atmosphere, before being slowly re-solidified by ramping down to 1075 °C at a rate of 1 °C min^{-1} allowing for gradual re-solidification.

It has been shown that melting/re-solidification allows for reduction of nucleation density when combined with high growth temperature under atmospheric pressure conditions (APCVD). Another potential advantage is that APCVD is not self-limiting over the same parameter space as it is for low-pressure CVD (LPCVD), allowing for the growth of bilayer and few-layer graphene of high crystal quality. However, the growth mechanisms of atmospheric pressure CVD is less-well understood. To date the literature on the use of melted/re-solidified copper as a growth substrate is limited, none of which report the growth of bi- and tri-layer graphenes. To enable a study of the growth dynamics

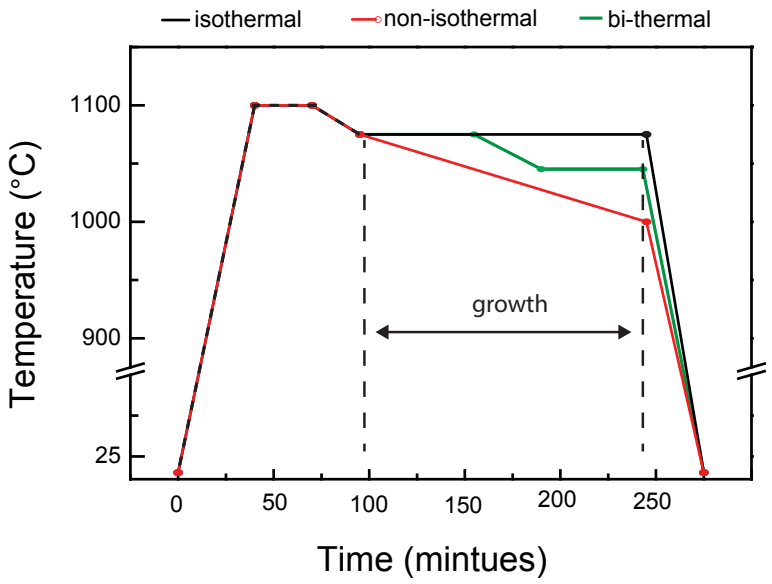

Figure 3.2: Temperature profiles for several types of growth used to investigate ad-layer formation on melted/re-solidified copper substrates.

of ad-layer formation we utilise various temperature profiles during growth as illustrated in Figure 3.2. After growth the foils are unloaded from the furnace tube and prepared for transfer by electro-chemical de-lamination. First, a thin poly-methyl methacrylate (PMMA) support-layer ($\sim$ 150 nm) is spin coated onto the graphene-copper surface followed by curing under vacuum. For de-lamination graphene-copper forms the anode, platinum the cathode and sodium hydroxide (NaOH) the electrolyte, with a DC voltage source providing $\sim$ 10 V and corresponding two-terminal current of $\sim$ 500 mA measured over $\sim$ 1 cm.

3.2 RAMAN SPECTROSCOPY

Raman spectroscopy offers a fast and non-destructive technique to characterise graphene and TMDCs. After optical microscopy, it is the go-to technique for characterising graphene and can be used to determine a vast range of material properties including layer number, doping, strain, disorder and stacking orientation. As such it is particularly well suited for determining the degree of functionalisation. The Raman process involves the inelastic scattering of light by a material in which the sample is illuminated with a monochro-

matic source with incident photon energy $E_i = E_{laser}$ and momentum $k_i = k_{laser}$. During such a scattering event an electron is excited from the valence band to conduction band upon photon absorption. The excited electron is then scattered by emission (Stokes) or absoprtion (anti-Stokes) of a phonon, followed by relaxation of the electron to valence band by emission of a photon with energy, E_{Sc}. The absorption/emission of a phonon results in a difference in energy of the emitted light, where the phonon energy, $E_\Omega = E_i - E_{Sc}$. Typically (Stokes), the intensity of scattered light is plotted as a function of energy where Raman shift (cm^{-1}) = $(\frac{1}{\lambda_i} - \frac{1}{\lambda_{Sc}})$, allowing direct measurement of phonon frequency. Further, the gap-less dispersion relation of graphene make it ideally suited for characterisation using Raman spectroscopy, as the continuous density of states allows for satisfaction of the resonance condition for all phonon energies in un-doped samples, yielding large signal/noise. Measurements are performed using a Renishaw Raman microscope, for which the schematic is shown in Figure 3.3(a), where the sample is typically illuminated with ∼10 mW green light (532 nm) through a 50x or 100x objective lens with a spot diameter ∼1 μm.

3.2.1 *Raman spectra of graphene*

Raman scattering in graphite, carbon nano-tubes, diamond and amorphous carbon material is well documented[2]. A typical Raman spectra of graphene always shows characteristic peaks in the G-band at $\sim$ 1580 cm^{-1} and 2D-band at $\sim$ 2700 cm^{-1}, as shown in Figure 3.3(b). The G-band originates from the E_{2g} phonon at Γ and is present in all forms of carbon. The G-band shows stiffening upon doping and is also useful in determining layer number. In samples with some degree of disorder in the sp^2 lattice (e.g. missing carbon atoms, sp^3 hybridisation, grain boundaries) the defect activated D-band at $\sim$ 1345 cm^{-1} is present, where the intensity is directly proportional to the number of defects. This peak originates from inter-valley scattering by a defect of an excited electron. Similarly the D'-band is defect activated and typically measured at the edges of flakes, originating from intra-valley defect scattering. As such the D'-band can be activated by perfect zig-zag or arm-chair edges in the absence of the D-band. The 2D-band is the overtone of the D-band and does not require a defect for activation. The 2D-band is particularly useful for determining layer number and stacking orientation for thin graphene layers. For single graphene layers the 2D-band can be fitted with a single Lorentzian, while for increasing

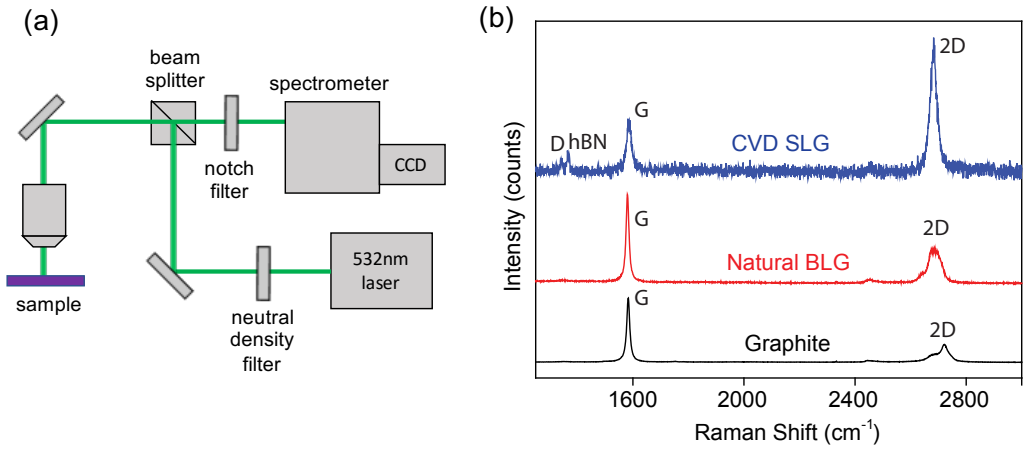

Figure 3.3: (a) Schematic of setup used for Raman spectroscopy measurements (b) Typical Raman spectra for graphite (black), natural bilayer graphene (red) and CVD single-layer graphene (blue) collected using $\lambda = 532$ nm excitation wavelength.

layer number the number of possible transitions increases resulting in splitting of the band, shown in Figure 3.3(b)(red) for natural bilayer graphene. In the following chapters several terminologies are used to describe the Raman spectra including peak position (e.g. Pos(G)) quoted in wave number, peak intensity (e.g. I_G) and peak-width (FWHM) measured as the full-width at half maximum intensity. Such values are extracted by fitting the raw data with one (or more in the case of the 2D-band of 2- and 3-layer graphene) Lorentzian. Further, for extraction of layer number and defect density often the ratio of intensities is quoted; e.g. estimation of distance between defects/functional groups the ratio of intensities for the D- and G-bands are quoted as I_D/I_G.

3.3 OXIDATION OF GRAPHENE AND 2D MATERIALS

Chemical functionalisation of graphene and 2D materials may be achieved by several techniques and can be used to modify material properties through the introduction of functional molecules or ad-atoms in addition (replacement) to (of) the pristine material. For graphene, several challenges faced by the device community have been addressed through chemical functionalisation, such as opening a band gap, reduction of sheet resistivity for transparent electrodes and increasing selectivity of sensors to specific stimuli. Here I outline three methods of oxidation; Hummers method, plasma functionalisation

and laser-assisted oxidation.

3.3.1 *Wet-chemical oxidation*

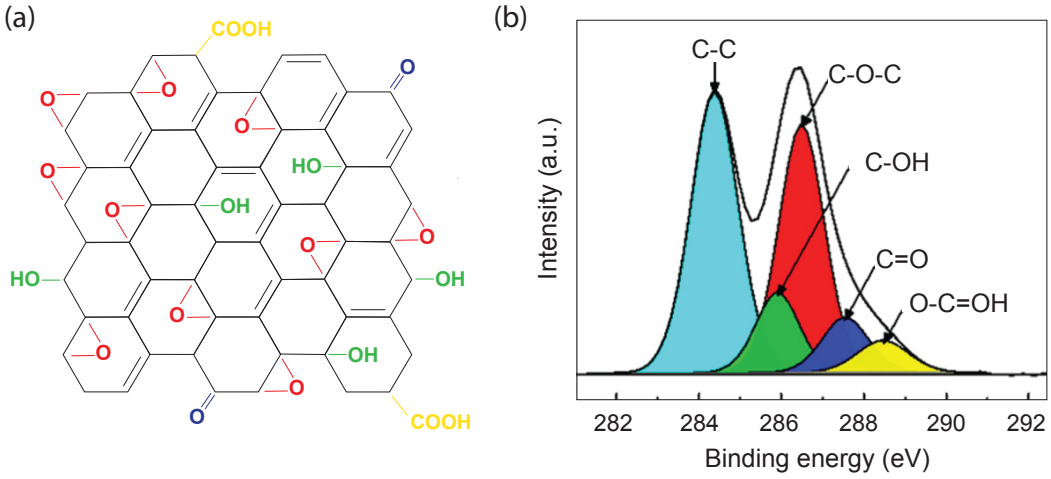

Figure 3.4: (a) Typical distribution of oxygen on a graphene sheet with epoxide (C-O-C), carbonyl (C=O), hydroxyl (C-OH) and carboxyl (C-COOH) functional groups (b) Measured XPS spectra for the C1s shell of wet-chemical GO, adapted from[3]

Functionalisation of graphene with oxygen can be achieved by a number of different routes, typically determined by the choice of starting material and application in mind. Solution processable materials offer a simple and low-cost option for the fabrication of flexible devices on an industrially viable scale. Chemical oxidation of graphite, such as that sold commerically, is achieved using Hummers' method[4] in which graphite flakes are treated with a mixture of sulphuric acid, sodium nitrate and potassium permanganate. The reaction allows for large-scale production of graphite oxide and is already well implemented industrially. The resulting material typically exhibits an atomic carbon/oxygen ratio of 2.1-2.9, with epoxide (C-O-C), carbonyl (C=O), hydroxyl (C-OH) and carboxyl (O-C=OH) functional groups typically present at both the edges and on the basal plane. After removing residuals of the chemical reaction the solution is subject to several hours of ultra-sonication to exfoliate the oxidised graphite down to just a few layers. A simplified structure of one oxidised plane is shown in Figure 3.4(a) along with a typical XPS spectra for the C1s shell. In reality the structure is often complex, where the increased fraction of

sp^3 hybridisation, causes the graphite sheet to lose its well defined planar structure and become buckled. It has been shown that the quality both of the specific oxidants and graphite flakes used have a significant effect on product of the reaction, and as such there is often large variation in material properties presented in the literature[5]. The increased fraction of sp^3 bonded carbon results in band-gap opening and large disorder with sheet resistance typically > G $\Omega/\square$. The large amounts or disorder can be observed in the Raman spectra as broad line-width of the D and G-bands as well as pronounced D-band and suppression of the 2D-band, where the ratio of I_D/I_G shows an increase with removal of oxygen (reduction).

3.3.2 *Plasma-assisted functionalisation*

The successful functionalisation of graphene with reactive species generated by plasma has been demonstrated using oxygen[6], fluorine[7], chlorine[8], ammonia[9] and hydrogen[10] and as a surface functionalisation technique is particularly well suited to monolayer graphene. Typically, graphene is placed inside a reactive-ion-etching system and exposed to mild reactive plasma. By applying a large voltage across two electrodes in the presence of a gas (e.g. O_2, SF_6, Cl_2, NH_3, H_2), the oscillating electric field ionises the molecules forming highly reactive ionic species which react the sample either chemically or physically by bombardment (sputtering). For functionalisation of graphene samples it is important to minimise damage by bombardment, so the plasma power is kept < 5 W or the samples are placed out of the direct plasma stream. Regarding electrical properties, the addition of oxygen and fluorine by plasma to the graphene lattice results in an increase in sp^3 hybridisation causing band-gap opening[11], yielding the materials insulating. The degree of functionalisation by plasma is typically inspected with Raman spectroscopy and XPS, Raman spectra for graphene functionalised with oxygen and fluorine are shown in Figure 3.5(a) as the blue and green lines. Both treatments result in a substantial loss of sp^2 hybridisation (and an increase in sp^3) giving rise to enhanced D-band and D'-band while the inter-valley scattering associated with the 2D band is suppressed. Broadening of the bands is also observed due to the relaxation of the selection rules. For functionalisation a reactive ion etcher is used at low power. Graphene on copper or SiO_2 is placed either in the centre of the stage (SF_6) or out of the plasma stream (O_2). A DC plasma is used for short periods (<10 seconds). Figure 3.5(b) shows the evolution of the Raman spectra

for few-layer graphene grown on nickel foils. Evolution of the Raman spectra shows near saturation after just $\sim$ 10 seconds exposure, suggesting saturation in the degree of functionalisation. Even after 60 s the Raman spectra did not show signatures of highly oxidised graphene compared to the monolayers which may be explained by lower reactivity of few-layer graphene, consistent with the literature[12].

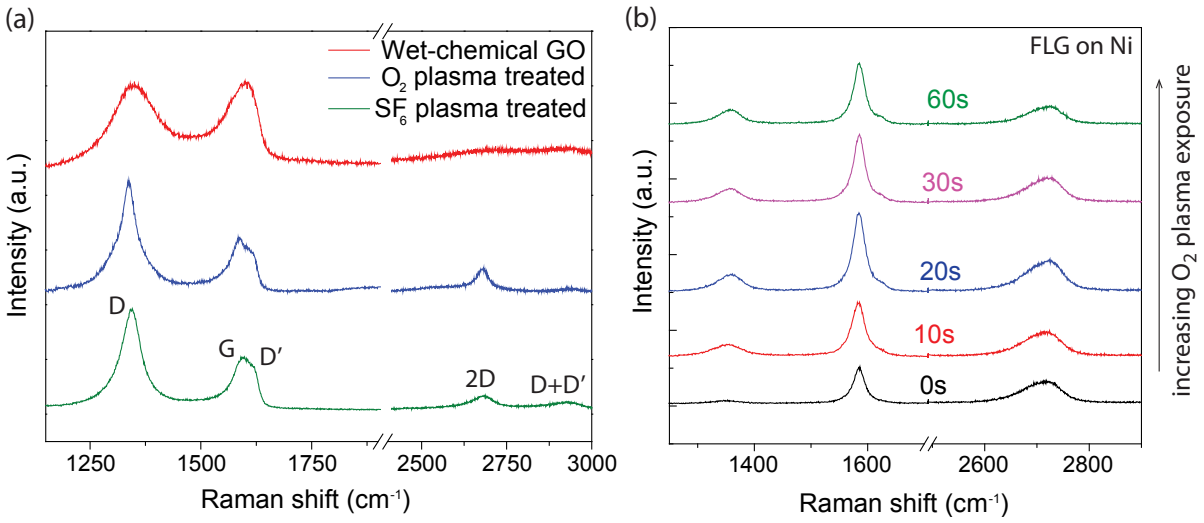

Figure 3.5: (a) Raman spectra of several functionalised graphenes; wet-chemical GO (red) and plasma treated graphene using oxygen (blue) and sulphur hexafluoride (green) gases (b) Evolution of Raman spectra for FLG exposed to mild oxygen plasma.

3.3.3 *Photo-oxidation of 2D-materials*

The poor chemical stability in ambient conditions of some 2D materials is well-known, and has required the development of expensive and complex glove-box systems where the sample is kept in inert atmosphere for all processing steps and measurement. Such instability has been observed for many 2D materials including several of the layered dichalcogenides; $MoSe_2$, $MoTe_2$, WSe_2, WTe_2 and HfS_2, as well as for BP. The degradation is driven by the single or combined reactions between the material and ambient oxygen, water, temperature or light. Direct evidence of light-induced oxidation has been observed for BP, where the effect of key environmental factors including temperature, light and humidity on degradation of BP is studied. The highest rate of degradation occurs for a combina-

tion of light with humidity[13]. Laser-assisted oxidation of WSe_2 has been presented by Tan et al., where the resulting WO_x shows doped semiconductor behaviour, losing its well-defined ON/OFF behaviour[14].

In the last chapter of this thesis the selective photo-oxidation of Hafnium-disulphide (HfS_2) is demonstrated for use as a dielectric/switching material for graphene FETs and resistive switching devices. HfO_2 (hafnia) is a wide-bandgap (E_g = 5.7 eV) material with $\kappa = 25$. In these experiments flakes of HfS_2 are exfoliated and then irradiated with laser light in ambient conditions, resulting in oxidation of the material. Laser-writing of high-κ dielectrics into selected areas of 2D materials has a multitude of possible applications including ultra-thin, flexible dielectrics for top/side gating FETs, tunnel barriers and tunable switching regions for ReRAM devices. Controlled oxidation of HfS_2 has not previously been demonstrated. Of the limited literature reported on thin layers of HfS_2, Chae et al. observe oxidation upon exposure to ambient conditions, observed as a reduction in contrast of the material and degradation of device performance[15]

3.4 ELECTRICAL CHARACTERISATION

3.4.1 *Field-effect transistors*

Electrical characterisation of FETs is performed using both AC and DC measurements. A device schematic is shown in Figure 3.6(a). Measurement of graphene FETs is performed in four-terminal configuration to negate contact and line resistances. Typically a graphene Hall bar is fabricated using the method outline in Appendix A. In constant-current, a small AC voltage ($\sim$ 10 mV) is applied across a resistor (R_b) which is connected to the sample. The resistor value is chosen such that $R_b >> R_{sample}$ (typically R_b = 1-10 MΩ) for a well-defined constant current ($I_{cc} \approx V_{osc}/R_b$). A lock-in amplifier is then used to measure the voltage drop either along (V_{xx}) or across (V_{xy}) from which the resistivity ($\Omega/\square$) is calculated. Figure 3.6(b) shows a typical gate-voltage dependence of resistance. Modulation of the chemical potential is achieved by applying a DC voltage to the highly doped silicon (Si^{++}) back-gate electrode across an $\sim$300 nm SiO_2 gate dielectric. The carrier density (n) in the channel is then extracted assuming a parallel plate capacitor model, where;

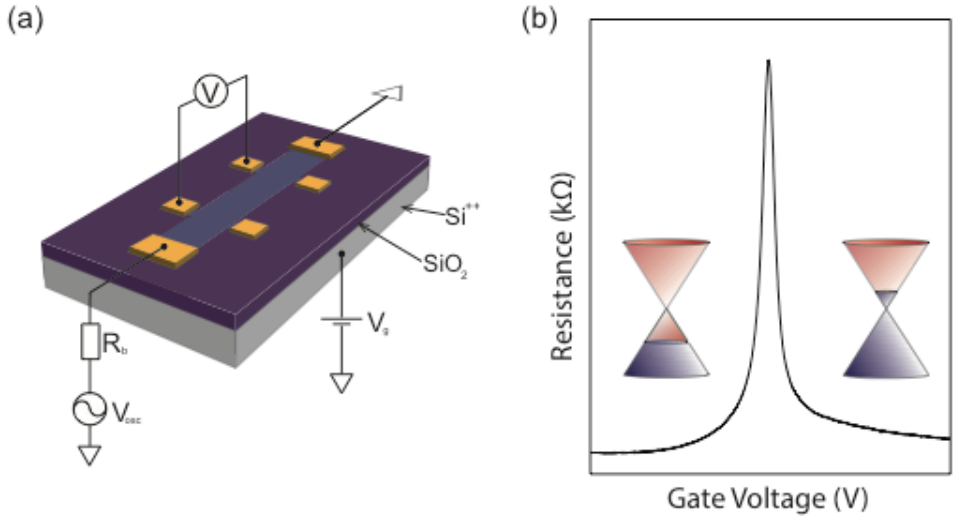

Figure 3.6: (a) Illustration of Hall bar geometry FET with measurement circuit (b) Typical measured resistance-gate characteristics of a CVD graphene FET.

$$n = \frac{\epsilon_r \epsilon_0}{e \cdot d} \cdot V_g \tag{3.1}$$

The field effect mobility can be estimated from where;

$$\mu = \sigma(V_{bg})/en(V_{bg}) \tag{3.2}$$

where σ is the conductivity ($\square$ / Ω), where typically the carrier mobility is typically quoted for a value of carrier density away from the charge neutrality point.

Temperature dependent measurements are performed using a home-built dipping probe where the sample is bonded into a 20-pin lead-less chip carrier (LCC) and mounted into the probe via spring-loaded pins. A commercially available LakeShore AlGaAs diode is used to monitor temperature from 300-4.2 K. This probe also serves as an annealing probe for the removal of adsorbed moisture and contaminants where the samples may be heated to 400 K just above the helium liquid if required.

3.4.2 *Resistive switching devices*

Electrical measurements of resistive switching devices are performed in DC in 2-terminal configuration. For clarity, throughout this thesis the current-voltage characteristics of devices are measured using a DC voltage source applied to the top electrode with the bottom electrode grounded, as shown in the schematic in Figure 3.7(a). Devices are categorised as either cross-bar or cylindrical-cell. Cross-bar devices are typically wire-bonded into a LCC and loaded into a vacuum/cryogenic probe or measured in a probe station. Cylindrical-cell devices are measured using conductive AFM, where the blanket-film bottom electrode is grounded and the bias applied to a conductive AFM tip. The most important consideration in measurement of ReRAM devices is the use of a well controlled compliance current or load resistor to prevent permanent breakdown of the device, where an irreversible switching to the LRS is observed for insufficient current limiting. The physical origin can be ascribed to a variety of breakdown of insulating interface layer, strong reduction of oxide by excessive Joule heating, or formation of over-sized conducting filaments. A typical current-voltage dependence is shown in Figure 3.7(b).

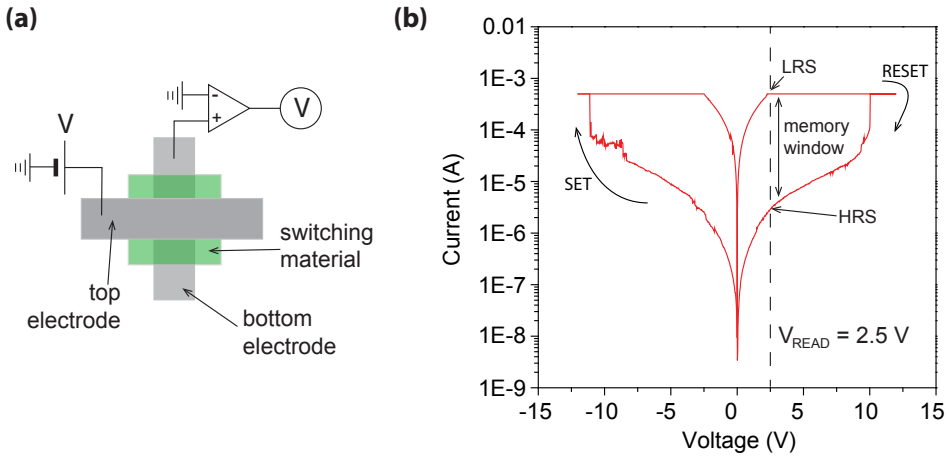

Figure 3.7: (a) Cross-bar electrode configuration with approx measurement circuit (b) typical semi-log current-voltage characteristics of a resistive switching cycle with important parameters included.

Pulsed switching measurements are also performed to determine the speed of operation

and cycling endurance for ReRAM devices. For these tests a pulse generator is connected in parallel with the voltage source via a two-way switch/relay. After application of a pulse the switch can be flipped to the voltage source - used to perform a low-range current-voltage sweep, from which the resistance can be calculated. For such measurements the IV_{read} range is significantly less than the threshold voltage to avoid un-wanted switching. For cycling endurance the pulse generator is used to apply several switching cycles and IV characteristics may be periodically measured. Lastly, temperature dependent measurements are used to learn about the origin of switching in devices, to assess the mechanism of carrier transport in devices. For these measurements devices are switched into either the LRS or HRS after which the resistance is measured as a function of temperature while dipping into a liquid ^{4}He bath.

3.5 ATOMIC FORCE MICROSCOPY

Atomic force microscopy (AFM) is used to determine step heights of flakes and films as well as measurements of surface topography/roughness on the nanometre scale. Also, for some systems the AFM tip is used to make electrical contact as is demonstrated in Chapters 5 & 6. AFM is a scanning-probe microscopy technique consisting of a cantilever with a sharp tip (radius ∼10 nm) at one end where the spring constant of the cantilever is defined by the ratio of thickness/length. The tip/cantilever is typically made from a piece of doped silicon coated in a material such as Al, Pt or diamond-like carbon (DLC). A laser is focussed onto the the cantilever and reflected onto a position sensitive photo-diode called a quadrant photo diode (QPD). The output voltage of the QPD is a function of position which is in turn a function of the deflection of the cantilever. In this thesis both contact and non-contact modes are used, depending on the desired measurement. In contact mode the tip is in direct contact with the surface of the sample and force on the cantilever is kept a constant via feedback loop while the cantilever is scanned across the sample in the x-y direction. The typical contact area (tip radius) for a new tip is ∼10 nm^2, resulting in large pressure ($\sim 10^8$ Nm^{-2}) which can lead to sample damage. As such in this thesis contact AFM is used only for making electrical contact to resistive switching devices, where an electrically conductive tip is placed in contact with the top electrode of the device, acting as an electrical probe. For conductive-AFM (C-AFM) tips used are antimony-doped silicon coated in either platinum or diamond-like carbon. Tapping mode

is less invasive and used for the measurement of surface topography to extract data such as step heights (flakes and films) and surface roughness. In tapping mode a piezo-electric element is used to drive the cantilever near its resonant frequency ($\sim 10^2$ kHz). As the tip is scanned across the sample the tapping amplitude and phase is monitored and the tip held just above the surface, allowing for accurate measurement of the surface while not inducing any damage to the sample.

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4

CHEMICAL VAPOUR DEPOSITION OF LARGE HEXAGONAL GRAPHENE

4.1 INTRODUCTION

For commercialisation of graphene grown by chemical vapour deposition there are several important factors to consider. Namely the process should be robust, highly repeatable, tunable, safe and cost effective. Our group has shown previously that the principal cost in the CVD process is in the cost of the metallic growth substrate[1]. Further, the trend in CVD graphene research using copper substrates is towards that of single crystalline graphene on large scale. Towards this end there has been significant progress with several copper pre-treatments showing encouraging results. Here, I investigate the effect of temperature and copper purity on the growth of graphene on melted/re-solidified copper under atmospheric pressure conditions. I then provide a thorough characterisation of the as-grown graphene using Raman spectroscopy and electrical measurements.

The unique properties and promising applications of graphene materials are leading to an increased emphasis on efficient production of large single crystal graphene domains with high quality and multiple functionality. To date, much of the research has been focussed on the growth of polycrystalline graphene films, however the presence of grain boundaries has been shown to negatively affect the electrical[2;3] and mechanical[4;5] properties of the

material. As well as crystal quality, another factor limiting its implementation in electronics is the absence of a bandgap in single layer graphene (SLG)[6]. It has been shown that the electronic properties of graphene materials are layer-number and stacking-order dependent. For example Bernal stacked bilayer graphene (BLG) shows a gate-tuneable bandgap of $\sim$250meV[7] and twisted BLG exhibits a low energy Van Hove singularity at specific values of interlayer twisting angle[8].

The growth of single crystal monolayer graphene on copper by chemical vapour deposition (CVD) has been studied extensively, with several methods proposed for producing large single crystal domains through different methods of establishing control of graphene nucleation. The growth of large single crystals may be achieved by reducing the density of nucleations and thus the possibility of individual domains coalescing into a polycrystalline film. The nucleation step of the growth is probabilistic in nature and relies on an interaction between the carbon precursor and the substrate, therefore suppression of nucleation may be achieved by reducing the probability of an interaction[9]. Aside from employing diluted or localised carbon feeding, the nucleation may controlled through surface engineering of the growth substrate. Regarding the surface morphology, it has been shown that interactions prefer surface irregularities such as copper grain boundaries, wrinkles, rolling marks or crystal facets[10]. There have been numerous methods proposed to reduce such irregularities including extended hydrogen annealing[11], electro-polishing[12], chemical etching[13] and melting/re-solidification of the copper surface[14]. In addition to the physical structure, it has also been shown that the catalytic activity of the surface may be largely passivated with oxygen except for a few nucleation centres[15]. Growing multiple graphene layers has been demonstrated using either copper or nickel as the growth substrate[16;17]. Both transition metals act as a catalyst for the de-hydrogenation of methane but differ in their affinity for carbon, with a solubility at growth temperature of around 0.001% and 0.008% respectively[18]. Owing to the increased carbon solubility of nickel, few layer graphene may be grown relatively easily, however the number of layers and domain size is not easy to control due to the precipitation of carbon during cooling. Copper is most often used for monolayer graphene growth, as the majority of CVD conditions yield single-layer films due to a self-limiting growth regime. The various types of nucleation control mean that large area few-layer single crystal graphene domains are achievable on copper if the self-limiting growth mechanism is overcome. There are several recently published works that present solutions to this end including the use of Cu/Ni alloy[19], non-uniform car-

bon concentration between the inside and outside of a copper enclosure[20], large-molecule carbon feedstock[21], high H_2/CH_4 ratio[22] or non-isothermal growth conditions[23]. Growth of graphene on melted copper has been demonstrated previously, however a systematic study of growth dynamics is lacking, and the controlled growth of additional layers has not been observed.

First, I investigate nucleation, growth rate, domain size and layer number. As a starting point, the work of Moshin et al. presents growth of large single-layer graphene on melted copper, where suppression of nucleation density is ascribed to the reduced roughness of the melted/re-solidified copper surface. CVD growth is performed as outlined in the previous chapter, using the growth procedure set out in Figure 4.1(a), where the copper is melted and re-solidified in a reducing atmosphere prior to growth. The ratio of gases used is laid out in Table 4.1. Tapping AFM is used to measure the surface of the copper foil before and after a growth as shown in Figure 4.2(a) and (b), showing a significantly smoother growth surface after melting/re-solidification. It is also observed that the melting/re-solidification process yields large ($\sim$ 5 mm) copper grains, indicated by well aligned graphene domains across the entire copper grain as shown in Figure 4.2(c).

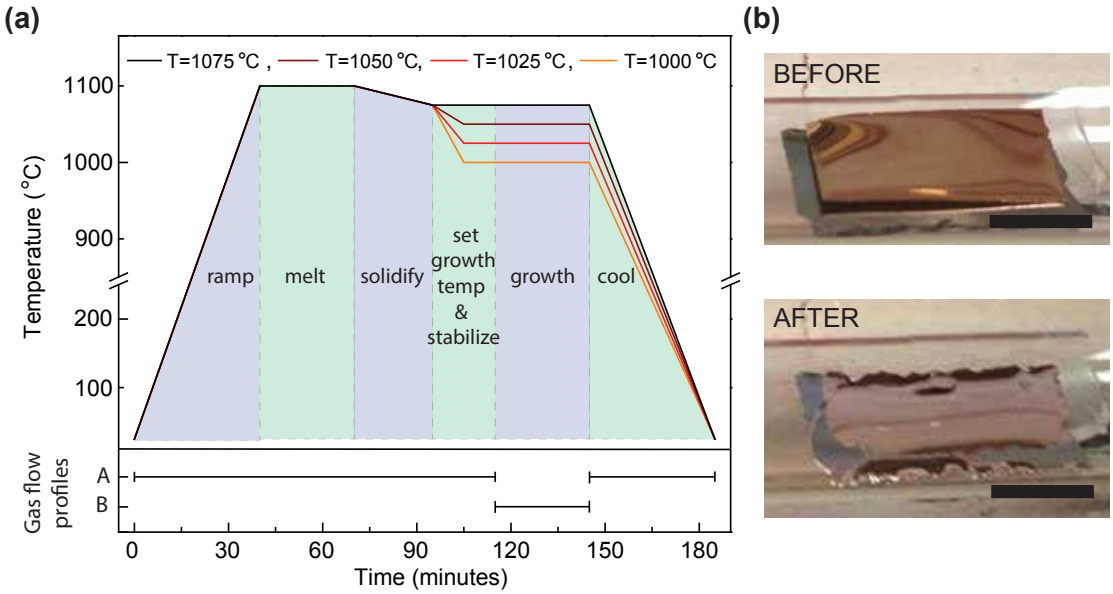

Figure 4.1: (a) Typical growth procedures for isothermal growths with several growth temperatures and (b) photographs of copper growth substrates on tungsten foil supports before and after the melting/re-solidification step. Scale bar is 1 cm.

Table 4.1: Gas flow rates corresponding to flow profiles A and B in Figure 4.1(a)

	gas flow rate (sccm)		
	Ar	H_2	0.1 % CH_4
A	275	25	0
B	250	25	25

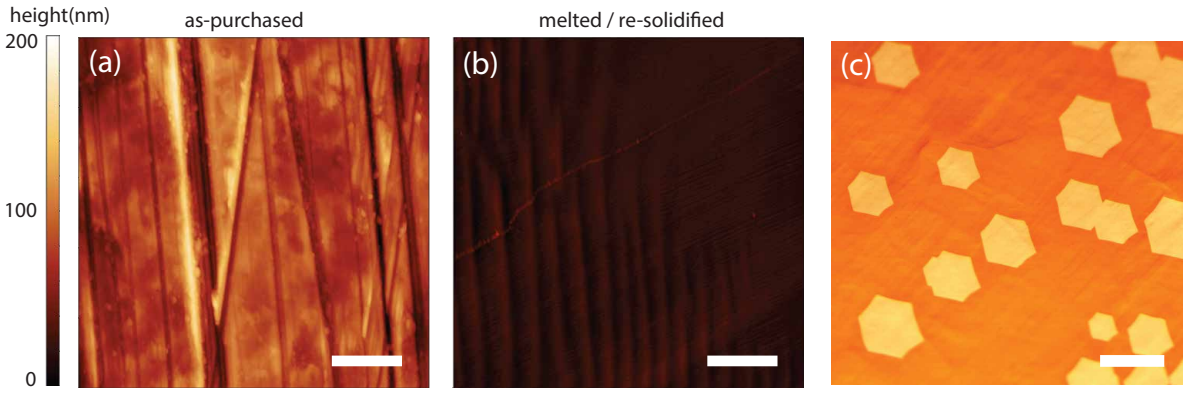

Figure 4.2: Tapping AFM of the copper foil surface (a) before and (b) after the melting and re-solidification of the copper surface. (c) Highly aligned graphene domains on the re-solidified copper surface. Scale bars in (a) and (b) are 2 μm and 100 μm in (c).

4.2 EFFECT OF COPPER PURITY

Of the various control parameters explored, choosing sufficiently pure copper was found to be crucial. During a typical growth of large hexagonal graphene domains, copper is melted onto a refractory metal support (tungsten/molybdenum) before introducing any carbon precursor. For high purity copper (99.999%), this results in substantially smoother surface morphology and large copper grains. However, for lower purity copper (99.8 %), the surface morphology after melting and re-solidification is substantially rougher showing signs of the aggregation of slag on the surface indicated by the red arrow in Figure 4.3(a). These surface impurities showed the highest density in the centre of the foil (thickest region) suggesting it may be linked to a bulk effect. Often impurity particles are present at the centre of some graphene domains which may result in increased probability of nucleation, as shown in Figure 4.3(b). A similar result is observed when a trace amount of

aluminium is introduced onto the underside of the copper (1.5 nm thermally evaporated) before melting/re-solidification. Again, following melting and re-solidification surface impurities are present, suggesting diffusion of the impurities through the copper during the melt as outlined in Figure 4.3(c). The introduction of aluminium impurities into high purity copper results in combined high nucleation density and migration of impurities to the surface of the copper, likely during the molten-phase. These experiments show that the presence of intrinsic and artificially introduced metal impurities results in poor surface quality after melting/re-solidification, important when considering the platform as a re-usable growth substrate.

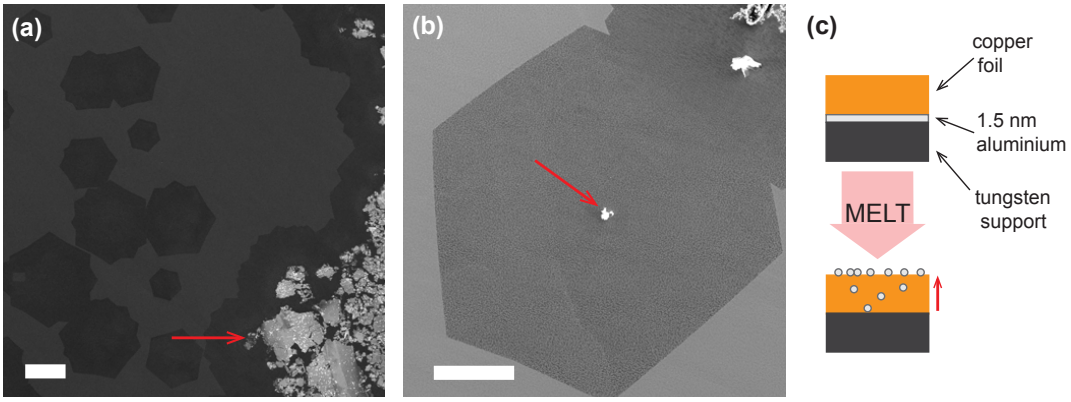

Figure 4.3: SEM micrographs of graphene domains grown on low purity copper with a melting/re-solidification step. (a) shows graphene domains at the edge of a foil with aluminium impurities indicated by the red arrows (b) shows a single layer graphene domain with an impurity particle in centre. Scale bars are 100 μm.

4.3 EFFECT OF GROWTH TEMPERATURE

A systematic study is performed for various growth temperatures. For these experiments all foils are subject to the same melting/re-solidification pre-treatment. The effect of growth temperature was found to have a significant effect on both nucleation density and growth rate, in-line with previous reports for other pre-treatments of the copper growth substrate. As is typical of CVD the growth rate, R, was observed to follow; $R = R_0 exp(\frac{E_A}{k_B T})$, where T is the growth temperature. Following growth, copper foils were oxidised for visualization, shown in Figure 4.4(a).

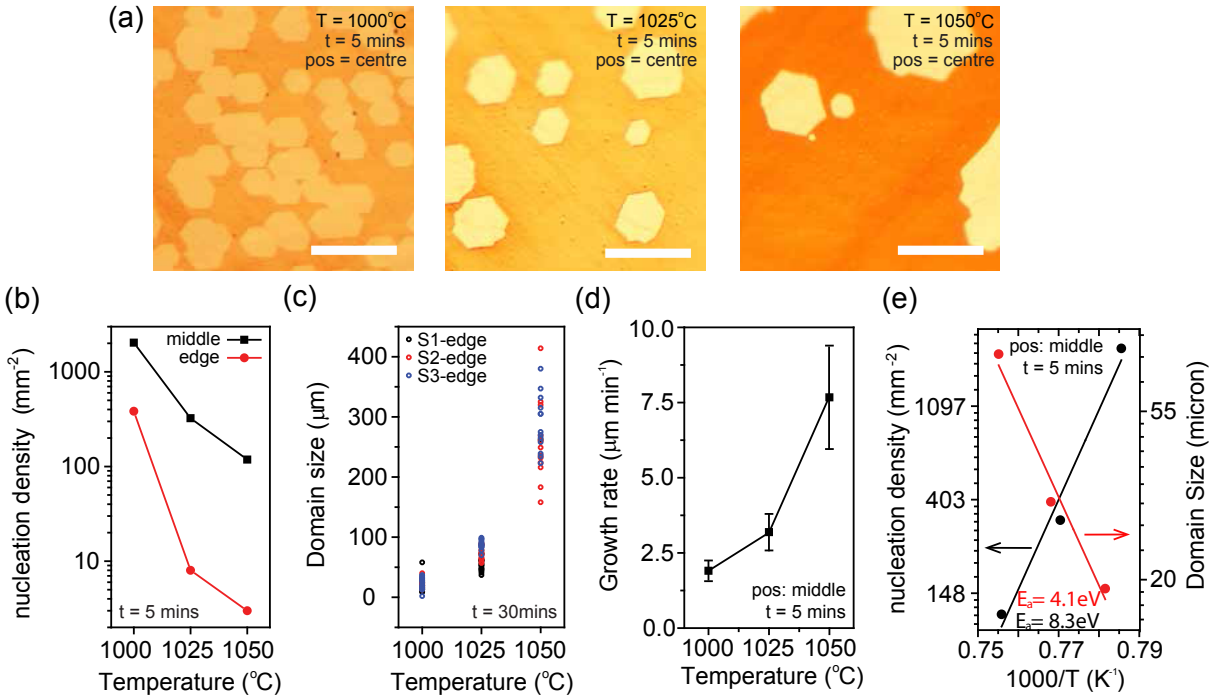

Figure 4.4: (a) Optical microscope images of graphene domains on copper (oxidised) for increasing growth temperature. Scale bars are 50 μm. (b) nucleation density vs. temperature (b) domain size vs. temperature for 3 different growth foils (c) growth rate vs. temperature and (d) natural logarithm of nucleation density and domain size vs. 1000/T for extraction of activation energies.

The nucleation density showed strong dependence on temperature, with higher temperatures yielding high suppression of nucleation. Figure 4.4(b) shows the effect of temperature on nucleation density. The analysis was performed using optical microscopy to count graphene domains per area at the centre of foils (black) and at the edge (red), where individual hexagonal domains are counted. Interestingly a much greater density of graphene domains is observed in the centre of the copper foils where the result of the melting means it is substantially thicker. This suggests that there may be some bulk effects playing a role. In the centre of the foils there was a reduction of one order of magnitude in nucleation density (mm^{-2}) for an increase in temperature of 50 °C corresponding to a negative activation energy of $\sim$ 8.3 eV, as shown in Figure 4.4(e). This value is in line with previous systematic studies of APCVD for electro-polished copper substrates ($\sim$ 9 eV[24]), having been previously ascribed to carbon-cluster desorption.

Growth rate is calculated by measuring the size (d) of hexagonal domains from point-to-point. Assuming a constant growth rate (r) from a single nucleation point in the centre of the domain for the duration of feedstock supply (t_{growth}) giving, $r = \frac{d}{2t_{growth}}$. Figure 4.4(d) shows the growth rate as a function of temperature for 5 minutes growth, with the highest growth rate of 7.5 μm/min observed for T = 1050 °C. This value corresponds to 0.125 μm s^{-1}, which is comparable to previous studies of growth rate (0.03-0.36 μm s^{-1}) for oxygen-free growth. It is noteworthy that we observe faster still growth rates for T = 1075 °C, for domains grown for optical and electrical characterisation (see section 4.4). Both nucleation density and growth rate can be fitted with to an Arrhenius relation, where the activation energy for growth rate was calculated to be $\sim$ 4.1 eV, as shown in Figure 4.4(e).

4.4 OPTICAL AND ELECTRICAL CHARACTERISATION

4.4.1 *Monolayer hexagonal graphene domains*

It is well documented that the quality of electrical and optical properties of graphene films grown by CVD show large variability when reported in the literature. Such variance is dependent on several factors including; 1) the quality of the as-grown graphene film (i.e. number of defects, grain size, layer number), 2) the quality of the transfer (transfer induced wrinkles, lattice damage, strain, metal/polymer etc.) and lastly is the final device architecture, which accounts for the quality of dielectric environment in which the graphene lies - that is to say that a dielectric free of dangling bonds with comparable lattice spacing (such as hBN) gives optimum results. To assess the crystalline quality of the as grown graphene domains they are transferred either directly to SiO_2/Si^{++} or onto hBN flakes exfoliated on SiO_2/Si^{++} with a home-built electro-chemical de-lamination setup using a method similar to that previously reported[25].

An isothermal growth with T = 1075 °C and growth time, t = 60 mins, results in predominantly monolayer hexagonal graphene domains as shown in Figure 4.5(a) and (b) with a typical domain size of 500-750 μm measured point-to-point. For visualisation with optical microscopy the growth substrates are baked on a hot-plate for 10 minutes at T=250 °C resulting in oxidation of the bare copper surface, whereas the areas with graphene are protected[26]. The hexagonal shape is typical of single crystals and there appears little

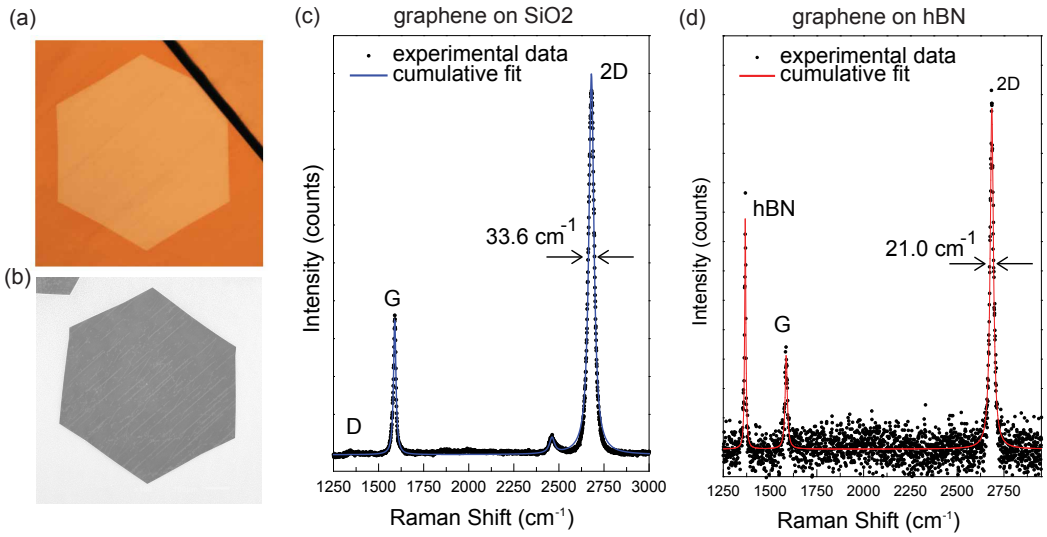

Figure 4.5: (a) Optical micrograph and (b) scanning electron micrograph of a monolayer hexagonal graphene domain on copper. (c) and (d) show Raman spectra for CVD monolayer graphene transferred to SiO_2 and hBN-SiO_2 respectively.

or no tapering of the edges suggesting an adequate supply of carbon feedstock. Raman spectra are shown for graphene transferred to SiO_2 and hBN-SiO_2 in Figure 4.5 (c) and (d) respectively. First, graphene on SiO_2 is absent of a D-band with a I_{2D}:$I_G \sim 2$, typical of monolayer graphene with high crystalline quality. Panel (d) shows the Raman spectra of graphene transferred to hBN flakes, with the characteristic BN peak at 1367 cm^{-1} originating from the E_{2g} phonon mode. It should be noted that the increased noise in panel (d) is due to the use of a shorter integration time. Again, the sample shows no significant D-band with I_{2D}:$I_G \sim 2$. Graphene on hBN shows a significantly lower FWHM of 21.0 cm^{-1} compared to 33.6 cm^{-1} for SiO_2 indicating significantly reduced strain/doping on the nanometre-scale[27;28]. For single layer graphene, Hall-bar devices are fabricated for graphene on hBN flakes to assess the electrical properties using the standard device fabrication outlined in Appendix A. To estimate the mobility in the samples, gate sweeps are performed under vacuum in four-terminal under zero-bias. The resulting resistance vs. gate-voltage sweeps for room temperature and liquid helium temperatures is shown in Figure 4.6(a). Devices show negligible residual doping and little or no hysteresis while performing gate sweeps, with $V_{CNP} \sim 0$ V. Panel (b) shows the mobility as a function of gate voltage, calculated by simple application of the Drude model with a

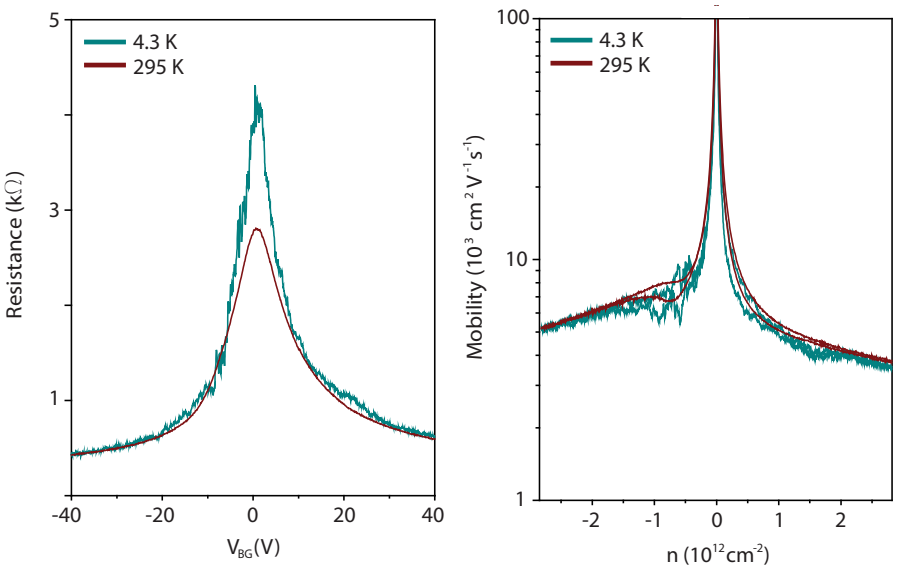

Figure 4.6: (a) Resistance vs. gate voltage for as-grown SLG transferred to hBN flakes on SiO_2 measured in four-terminal under zero-bias conditions (b) Carrier mobility vs. carrier density for the same device.

carrier mobility approaching 10,000 $cm^2V^{-1}s^{-1}$ near n = 2.5×10^{11} cm^2 and maintaining $\sim$ 5,000 $cm^2V^{-1}s^{-1}$ far from the neutrality point at V_{CNP} $\pm$40 V. It should be noted that devices have not been cleaned following fabrication by annealling in reducing gas prior to measurement, which would likely improve the measured mobility further but is outside the scope of this study.

4.4.2 *Bilayer hexagonal graphene domains*

To date the growth of ad-layers on re-solidified copper has not been observed. Interestingly some bilayer graphene domains are present in all growths, however the number of bilayer domains is enhanced enormously by using either an isothermal growth with T < 1075°C or a non-isothermal growth where the temperature of the growth is gradually reduced during the duration (ΔT = -1 °C min^{-1}). The resulting ad-layers are predominantly bilayer domains that occur both in the centre and off-centre of the large single-layer domains, observed both on the copper on following transfer, as shown in Figure 4.7(a) and (b). Combined optical microscopy and Raman spectroscopy reveals that the bilayers show a range of twisting angles relative to the larger monolayer domain and are plotted

in Panel (c) where the exotic Raman features associated with specific twist angles (θ) are observed due to the unique twist-angle dependent JDOS. This includes the presence of R' and R-bands typically observed for θ = 9-12° and the large enhancement of the G-band for $\theta = 12°$ associated with an additional van Hove singularity. Most commonly the relative twist angle observed is for $\theta \sim 0°$ showing strong coupling typical of Bernal-stacking. The 2D-band for such a domain transferred to hBN is plotted in Figure 4.7(d) showing a well-defined shoulder and four-Lorentz-fit typical of Bernal stacking. Further, it should be noted that domains transferred directly to SiO_2 instead exhibit a broad 2D-band with no well defined features likely due to the adverse strain and doping effects of the substrate.

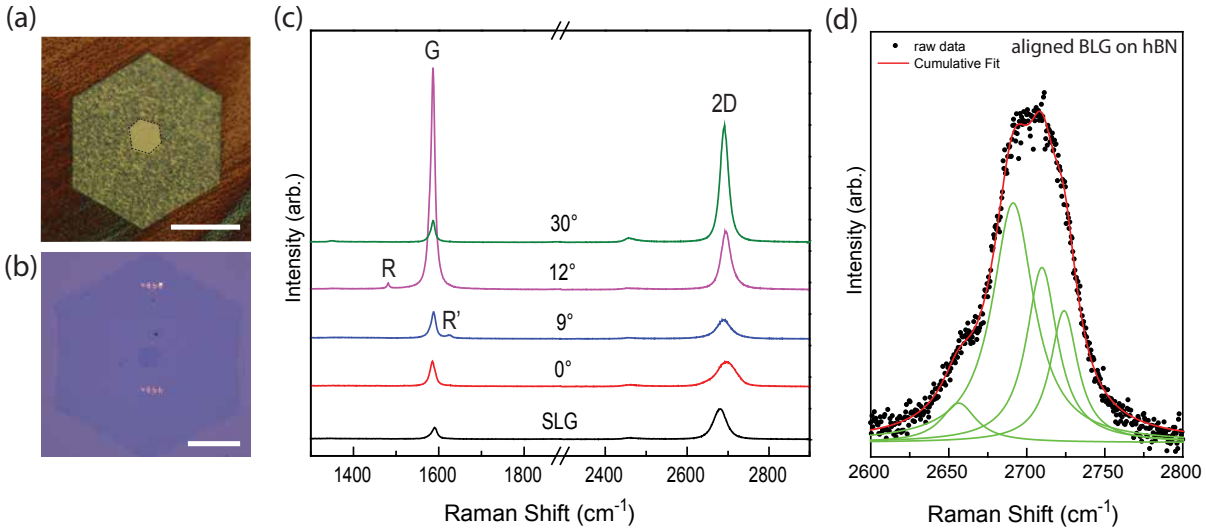

Figure 4.7: Optical micrograph of a bilayer graphene (a) on copper and (b) transferred to SiO_2. (c) Raman spectra collected for a number of different twisting angles, where the value is estimated from optical microscopy and comparison with previous reports in the literature. (d) 2D-band of bilayer graphene on hBN with $\theta \sim 0°$ typical of Bernal stacking

Finally, to investigate the uniformity of the graphene domains scanning Raman spectroscopy is performed for both single and bilayer graphene domains. Figure 4.8(a) and (b) shows Raman mapping of SLG transferred to an hBN flake on SiO_2 substrate. Here, the graphene is only partially supported by the hBN. Panel (a) shows a map of intensity of the hBN E_{2g} phonon around 1367 cm^{-1}, to the position of the hBN. Panel (b) shows a map of Γ_{2D} of the transferred graphene, with a value of ~23 cm^{-1} and ~31 cm^{-1} for hBN

and SiO_2 -supported regions. Panel (c) shows Raman mapping spectroscopy of Γ_{2D} for a well-aligned (top) and mis-aligned (bottom) bilayer region transferred to SiO_2. Uniform Γ_{2D} suggests domains contain only one twisting angle.

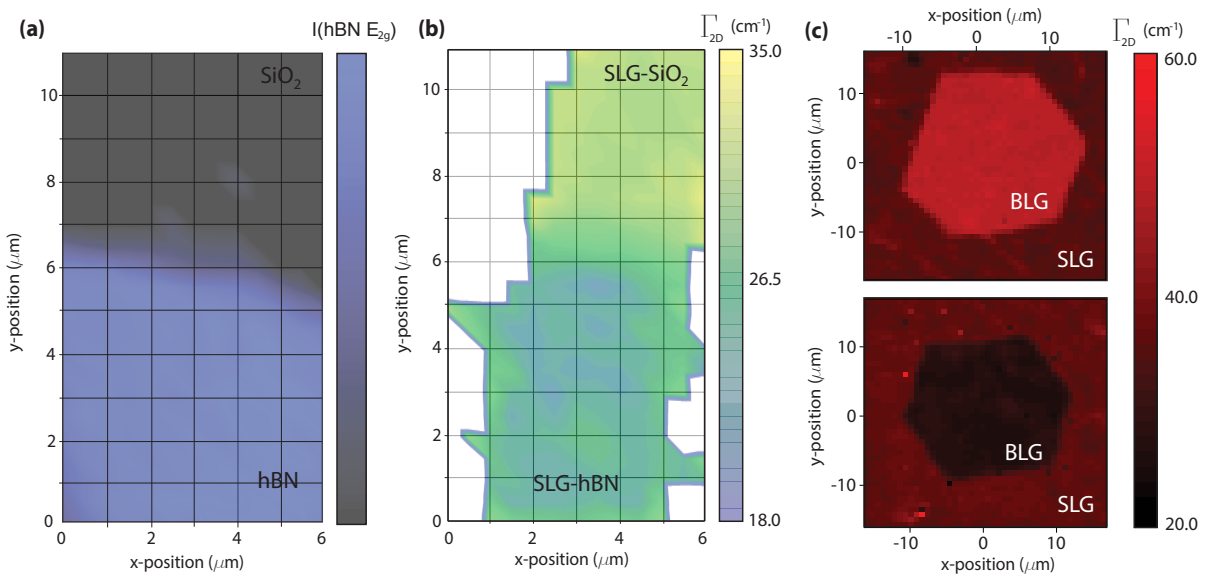

Figure 4.8: Raman mapping of as-grown single-layer graphene partially transferred to hBN and SiO_2 for a direct comparison (a) shows the position of the hBN layer shown as I(hBN E2$_g$) and (b) shows the Γ_{2D} for the graphene. (c) Raman maps of Γ_{2D} for bilayer graphene domains for small (top) θ and large (bottom) θ

4.5 CONCLUSIONS

In this chapter the growth of single and bilayer graphene on melted/re-solidified copper substrates is investigated. A systematic study of the effects of temperature on nucleation density and growth rate with all other parameters kept constant is performed. Maximum growth rate and minimum nucleation density was found for the highest growth temperature of 1075 °C, with a growth temperature of 1000 °C yielding continuous films in t < 10 minutes. An empirical activation energy, $E_a \sim 8.3$ eV for nucleation (negative) and $E_a \sim 4.1$ eV for growth rate was calculated. The effect of copper purity was investigated and it was found important to keep tight control of copper purity when using a melting step, as low purity copper showed significant impurities on the graphene surface following growth. Next I characterised the optical and electrical properties of the as-grown

graphene, all of which suggest high crystal quality. Using a lower growth temperature or non-isothermal growth was found to enhance additional layer formation, which showed a variety of stacking orientations as characterised by Raman spectroscopy with well-aligned domains showing Raman spectra typical of Bernal stacking when transferred to hBN. Electrical properties of the graphene domains were characterised by producing graphene Hall bars on SiO_2 and hBN substrates, with the latter showing high mobilities of upto 10,000 $cm^2V^{-1}s^{-1}$ near n = 2.5 $\times$ 10^{11} cm^2.

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5

FLEXIBLE GRAPHENE OXIDE RERAM

5.1 INTRODUCTION

Graphene oxide resistive memories offer a route to highly flexible and transparent resistive memories at low cost and with simple fabrication techniques. While there have been several demonstrations of resistive switching in graphene oxide films in the literature, the ultimate performance and clear understanding of the switching mechanism is still lacking. Further, while most articles presenting graphene oxide memory devices mention flexibility, few actually demonstrate it. In this chapter I investigate bipolar resistive switching in graphene oxide-based devices. First the controlled deposition of GO thin films is optimised, followed by characterisation with a combination of AFM, Raman spectroscopy and electrical transport measurements. GO thin films are then incorporated into flexible ReRAM devices based on Pt-Ti-GO-Pt stacks which are characterised using conductive-AFM. The flexible devices show the best performance (w.r.t. speed, cycling endurance and retention time) demonstrated to-date and the reversible switching is attributed to redox reactions with the reactive (Ti) metal top-electrode. Devices show flexibility over

[†]Parts of this chapter have been published in: VK. Nagareddy, MD Barnes,F. Zipoli, KT. Lai, AM. Alexeev, MF. Craciun & CD. Wright *Multilevel Ultrafast Flexible Nanoscale Nonvolatile Hybrid Graphene Oxide–Titanium Oxide Memories.* ACS Nano 11 (3), 3010-3021

[‡]Conductive-AFM characterisation of flexible Pt-Ti-GO-Pt devices was performed by Dr. V.K. Nagareddy and included with his permission

5000 bending cycles and ultimately failure for a bending radius of 4 mm, attributed to cracking of the metal bottom electrode. With this in mind I then investigate replacing the metal electrodes with few-layer graphene in ReRAM, beginning by testing the performance of graphene on flexible and stretchable substrates before integrating a few-layer graphene bottom electrode into flexible, bipolar GO-graphene ReRAM.

5.2 PREPARATION & CHARACTERISATION OF GO FILMS

As is outlined in the previous chapters, oxidation of graphene results in bandgap opening. For use in ReRAM, it is found that wet-chemical GO is the suitable material (over plasma oxidised graphene) due to the large oxygen content and insulating propeties. Many variations of wet-chemically derived graphene oxide have been shown to exhibit resistive switching. Differences in the material including graphene oxide quality (i.e. % wt. of monolayers), degree of oxidation, percentage fraction of various oxygen functional groups, average flake thickness, film thickness, method of production may result in the observed disparity in reported performance. To minimise such adverse effects, a reproducible vacuum filtration method for film production is developed similar to that of Eda et al.[1] using heavily diluted, commercially available graphene oxide solutions (Graphenea). Following dilution of the concentrated graphene oxide solution it is filtered through a mixed cellulose ester membrane with pore size of 25 nm, as shown in figure 5.1(a). After filtration the GO film is transferred to a substrate of choice (demonstrated for polyethylene terephthalate (PET), polyethylene naphthalate (PEN), glass and SiO_2/Si^{++}), either by de-lamination in water followed by 'fishing' or by a in-house developed soak-dry-peel technique where the film is wetted in de-ionised water, placed face down on the substrate with downward pressure and then the filter paper is gently blown with dry nitrogen and peeled away. The strong GO-substrate interaction combined with drying of the membrane allows for fast ($<$ 1 minute) total transfer time. Previous reports on the reduced graphene oxide thin films use long ($\sim$ 10 hours) drying in ambient conditions. Here, dry nitrogen acts to de-laminate the membrane from the GO film, observed as a change in contrast of the membrane upon release of the GO layer. It was noted that pre-soaking of the cellulose-ester membrane was crucial for producing uniform films, and that for macroscopic devices multiple transfers were used to eliminate the adverse effects of pin-hole shorts. Figure 5.1(b) shows an optical microscope image of GO films after 1, 2 and 3 transfers with

a typical tapping-AFM of topography scan plotted in panel (c). The use of multiple transfers allows for control over GO film thickness, shown in Figure 5.1(d), where film thickness increases by $\sim$ 50 nm per transfer. While the films presented in Figure 5.1 are approximately 50 nm per transfer, it is noted that for devices much thinner films are used ($\sim$ 10 nm) by reducing solute concentration to 8×10^{-2} mg/ml. Finally the as-transferred GO films are characterised by Raman spectroscopy as shown in Figure 5.1(e). After several days exposure to ambient conditions some partial reduction of the films (removal of oxygen groups) is observed, shown by the increase in I_D/I_G, suggesting the the stability of GO should be considered when using in applications.

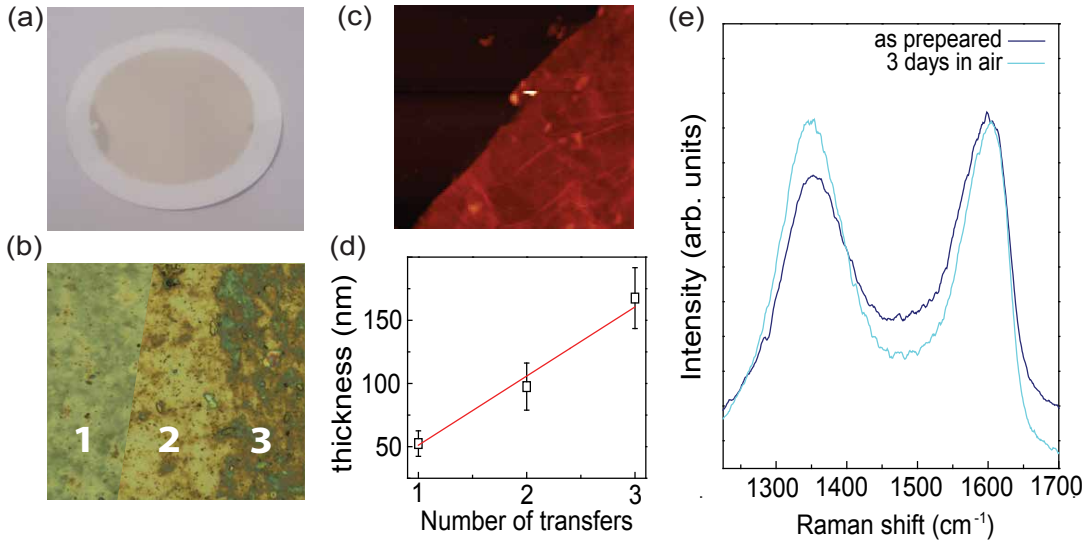

Figure 5.1: (a) Graphene oxide on cellulose ester membrane (r = 2.5 cm) after vacuum filtration (b) optical microscope image of 1, 2 and 3 subsequent transfers on glass used for control of film thickness (c) Typical tapping AFM image of the as transferred film on glass, showing high uniformity and low surface roughness (d) measured film thickness for 3 transfers of filtrate, error bars are meausred std. dev. of film thickness across scanned area (e) Raman spectra for as-transferred graphene oxide solution on SiO_2 substrate measured immediately after transfer and again after several days exposed to ambient conditions.

Thin films of graphene oxide platelets are highly disordered due to the breaking of the conductive sp^2 network that occurs upon oxidation. The degree of oxidation in GO depends on the method of oxidation and is reduced with time exposed to ambient conditions.

Electrically, this results in a change from semi-metallic to semiconducting behaviour. It has been shown that the electrical transport in single GO flakes is by variable range hopping between sp^2-rich regions, where the number of available hopping sites increases with chemical/thermal reduction[2]. Such carrier transport exhibits a temperature dependent resistance with $\ln(R) \propto T^{-\frac{1}{3}}$[3]. The electrical transport in thin films of graphene oxide (that is to say comprised of many overlapping flakes) has been reported to occur by much the same mechanism, differing only in that the film has a non-negligible thickness, and so $\ln(R) \propto T^{-\frac{1}{4}}$[4]. As such, after optimisation of the transfer technique, temperature dependent electrical measurements of GO thin films are performed. For characterisation of the highly resistive film a pair of inter-digitated gold electrodes are prepared onto the GO film is transferred, shown in Figure 5.2(a). Such device geometry yields an effective channel width/length ratio = 1100, reducing the total impedance of the device allowing for a reliable measurement of sheet resistance. To measure temperature dependence the sample is mounted on a cryogenic probe in a ^{4}He Dewar with a resistive heater to vary the temperature from 325 K - 4.2 K. The IV characteristics for various temperatures are in Fig 5.2(b) where the resistance of the films increases exponentially with $T^{-\frac{1}{X}}$, where the best fit is for $X = 4$, corresponding to variable range hopping for a 3-dimensional system, consistent with previous studies on GO - albeit produced using alternative methods such as drop-casting or spin coating. For T = 250 K, the total device resistance is $\sim$4 MΩ. Assuming the the resistance of the device is dominated by the GO film, this yields a sheet resistivity is 4.4 G$\Omega/\square$.

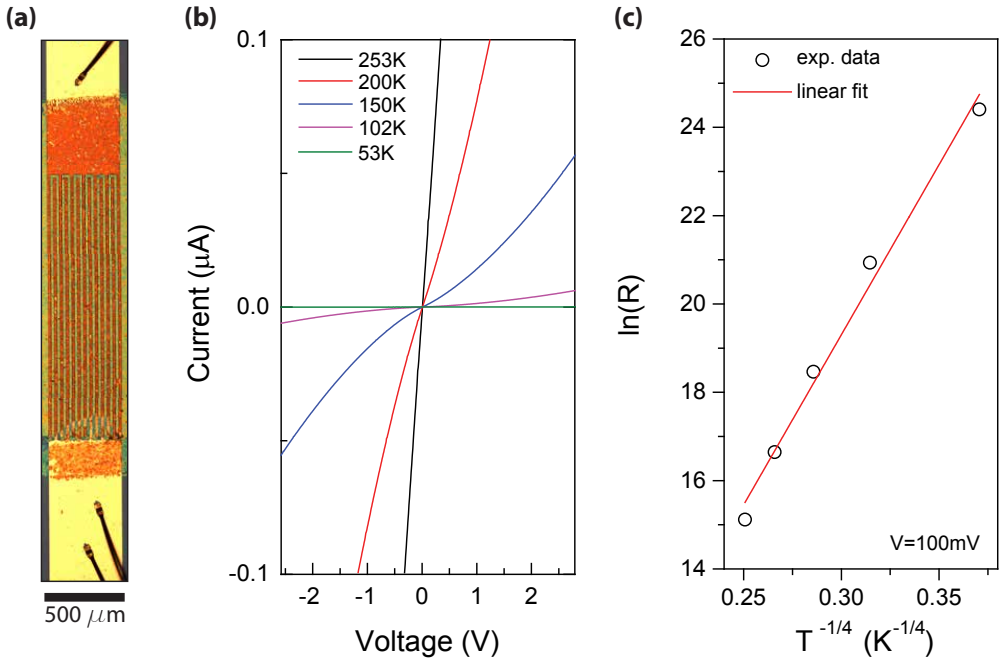

Figure 5.2: Optical microscope image of graphene oxide transferred to a pair of interdigitated gold electrodes (W/L = 1100) (b) current-voltage characteristics of the device for several temperatures, measure in ^{4}He atmosphere (c) Natural logarithm of two-terminal resistance vs. Temperature$^{-1/4}$).

5.3 FABRICATION & MEASUREMENT OF FLEXIBLE GO RERAM

Flexible resistive memory devices were fabricated on flexible polyethylene napthalate (PEN) substrates. First a blanket film of platinum is deposited to form the bottom electrode by DC sputtering. Then a GO thin film was transferred onto the using vacuum filtration, with thickness of 8 nm. Following deposition of the GO, top electrode pads were patterned in a PMMA mask with electron-beam lithography followed by deposition of a Pt-Ti top electrode by DC sputtering. After lift-off, the flexible device was mounted on a conductive-AFM stub with the bottom Pt contacted electrically with silver paste. For resistive switching experiments the sample is loaded into a Bruker Innova AFM system, and electrical connection to the top contact is made with a conductive AFM tip. In this study the tips used were heavily doped silicon with Pt/Ir coating and for extended switching studies tips coated with diamond-like carbon (DLC) were used due to their long

lifetime under repeated voltage pulsing. All resistive switching was performed with the tip biased and bottom electrode grounded as shown in Figure 5.3(a). A 4.7 kΩ resistor is mounted in series with the tip to avoid permanent breakdown and pulse switching is made possible using an arbitrary function generator with 50 Ω impedance matching resistor on the tip mount. Current-voltage characteristics of a typical switching cycle is shown in Figure 5.3(b) for devices shown in the inset. For the Pt-Ti-GO-PT device structure, no forming voltage was necessary to induce switching with devices initially in the high resistance state (HRS) where R ∼ 200 kΩ for V = 0.4 V.

5.4 PERFORMANCE OF FLEXIBLE HYBRID PT-TI-GO-PT DEVICES

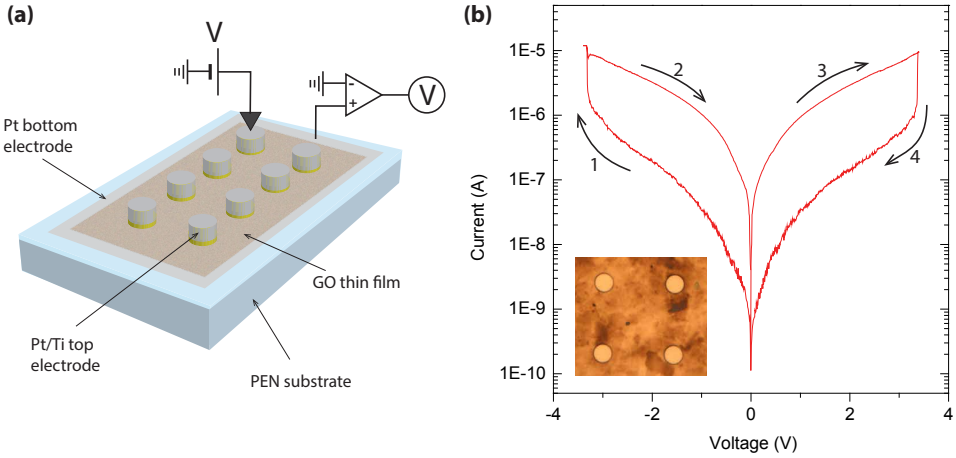

Figure 5.3: (a) Pt-Ti-GO-Pt device structure & measurement scheme (b) Current-voltage characteristics of a typical switching cycle, inset shown an optical microscope image of devices with 10 μm top-electrode diameter

For increasingly negative bias an abrupt change in resistance is observed at -3 V, where the current in the stack increases by $\sim 10^2$, corresponding to the SET process. Once in the low-resistance-state (LRS) the voltage is swept back through 0 V to +3 V where the current drops suddenly and the device returns to the HRS. Finally the voltage is ramped back down to 0 V, thus completing one switching cycle. After establishing several stable switching cycles the memory performance of devices is characterised. Figure 5.4(a) shows the resistance levels measured over 1000 switching cycles for a read voltage of 0.4 V. A

constant memory window of $\sim 10^2$ is observed for the entire range. The retention time for both the HRS and LRS is measured periodically after switching, shown in Figure 5.4(b), for $\sim$ 20 hours. The devices show some small variations in measured resistance but maintain a stable memory window for the duration of the measurement.

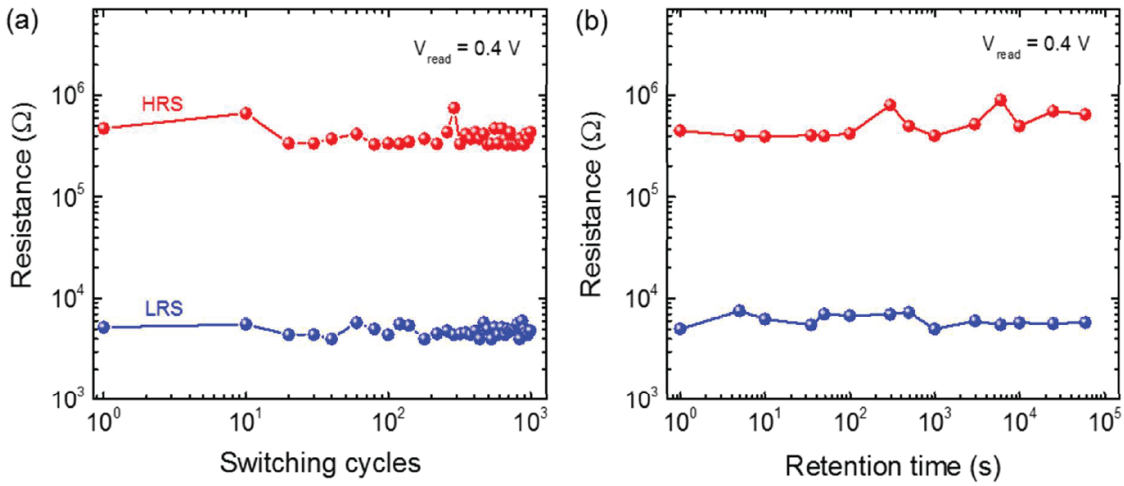

Figure 5.4: (a) Cycling endurance and (b) retention time for Ti-GO device on flexible PEN substrate in 1-bit operation. Adapted from[5].

While several studies of resistive switching in GO devices have been published, to date there is little information regarding the operating performance of devices with regards to speed of SET and RESET processes and while the flexibility of devices has been investigated, its combination with other additional functionalities such as multi-bit storage are lacking. Multilevel switching of devices is presented in Figure 5.5. Multilevel switching can be achieved by varying either the SET-pulse duration or SET-pulse amplitude. Figure 5.5(a) shows 2-bit operation for varying the SET-pulse amplitude for 60 ns pulse duration, where the larger pulse amplitude results in lower resistance of the LRS. Figure 5.5(b) shows the that each of 4 resistance levels for 2-bit operation are stable for $> 10^3$ seconds with nearly one order of magnitude memory window.

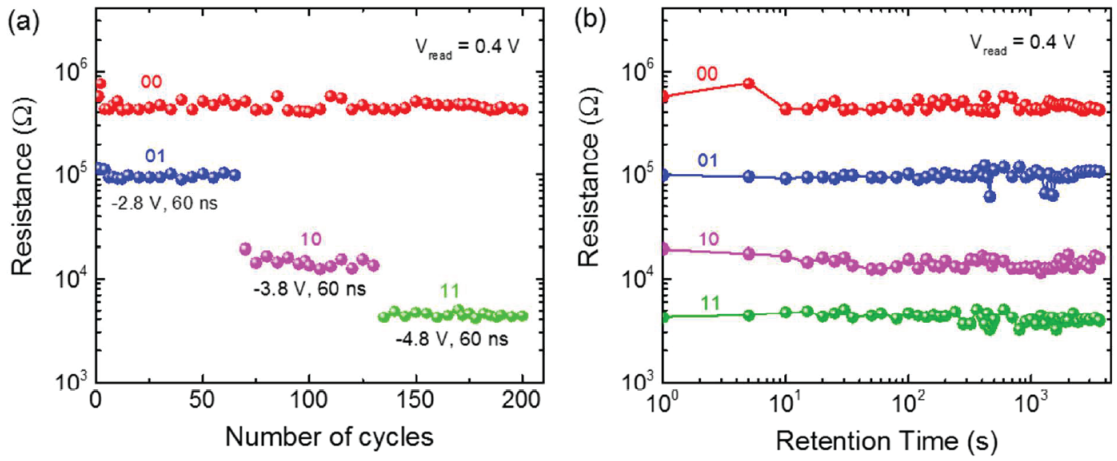

Figure 5.5: (a) Resistance levels measured for multilevel operation of Pt-Ti-GO-Pt devices achieved by varying the pulse amplitude for a 60 ns pulse width (b) Stability of resistance levels over 4×10^3 seconds. Both panels for a read voltage of 0.4 V. Adapted from[5].

The mechanical flexibility of devices is determined by measuring the switching performance with for periodic bending cycles and is shown in Figure 5.6(a) with no significant loss of memory operation after 5000 bending cycles (r = 9 mm). Figure 5.6(b) shows device breakdown occurs for a bending radius of 4 mm, where the device can no longer be SET into the LRS which may be explained by degradation of the Pt bottom electrode upon bending.

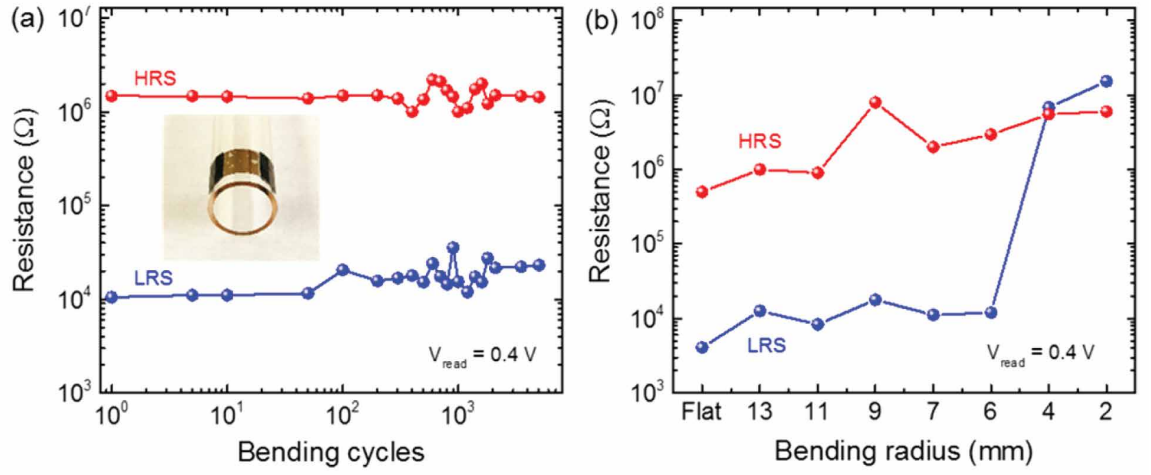

Figure 5.6: (a) HRS and LRS extracted from current-voltage cycling after several bending cycles, measured for bending radius r = 9 mm. Inset shows the flexible sample (b) HRS and LRS measured for increasing bending radius. Adapted from [5].

As mentioned above, the literature reports several mechanisms of resistive switching for GO thin films and often it is ascribed to a combination of several. For the presented devices the stack consists of Pt-Ti-GO-Pt, where the top Pt layer acts to cap the reactive Ti layer acting as an oxygen barrier. As such the active structure may be considered as as Ti-GO-Pt, with one reactive electrode in Ti (Φ = 4.35 eV) and one inert electrode in Pt (Φ = 5.6 eV). Previous studies demonstrate that the metals with a high affinity for oxygen often results in the formation of a sub-stoichiometric interface oxide upon its deposition onto switching material. Spectroscopic analysis of our devices, namely XPS and Raman spectroscopy confirm the presence of an interface layer between the titanium and graphene oxide as being formed during electrode deposition. The resistive switching behaviour may be ascribed to modification of this interface layer upon transition from SET to RESET. The observation of multi-bit operation can also be useful in understanding the switching mechanism and is consistent with redistribution of oxygen between the GO layer and the interface layer formed upon deposition of titanium top electrode. Figure 5.5(a) shows the resistance levels for four data levels achieved by varying the amplitude of the SET pulse. A larger SET amplitude results in a lower resistance LRS, consistent with the redox picture. Larger SET amplitude results in a larger net movement of oxygen from the interface layer to the GO layer, resulting in a larger reduction in resistance

of the interface layer. Computer aided molecular dynamic simulations also support the formation of such a layer is consistent with our experimental data, where migration of oxygen from the titanium to the GO results in an increased electrical conductivity of the interface[5]. Further experiments to elucidate the switching mechanism would be useful for design of an optimised device. Such experiments could include cross-sectional TEM of the interface layer for both LRS and HRS, similar to that presented bv Kim et al. where elemental analysis could be used to assess the precise distribution of oxygen ions in each state.

5.5 GRAPHENE ELECTRODES FOR BIPOLAR GO RESISTIVE SWITCHING

In the previous section we learn that the performance of flexible GO ReRAM using a reactive metal (Ti) top electrode with inert (Pt) bottom electrode shows fast switching speeds, high cycling endurance, large memory window and flexibility down to a bending radius of 4 mm before failure. Microscopic invesitgation of devices after failure suggested cracking of the metal for small bending radius. With this in mind it is reasonable to consider changing the bottom platinum electrode in devices with graphene for increased performance under bending, owing to its high mechanical stability. Turning to the literature, notable works include that of Lee et al. from the Stanford group who use a graphene edge electrode with HfO_x switching layer and TiN counter electrode[6]. Liu et al. report a cross-bas geometry non-volatile memory device based on rGO, with highly-reduced GO electrodes and lightly reduced GO switching layer[7]. The authors demonstrate reliable SET process however are unable to reset the device, which is attributed permanent reduction of the GO active layer. Such a device is limited to use as a write-once-read-many (WORM) memory device, useful for ROM but less useful in re-writeable memory applications. Kim *et al.* present a $SrTiO_3$ resistive memory with graphene nanoribbon (GNR) planar electrodes separated by a 30 nm gap formed by electro-burning[8]. Here, the authors demonstrate bipolar switching with low power consumption but are limited to some $\sim$ 200 cycles. Finally, Yang et al. present a transparent ZnO-based device with ITO electrodes and observe improved yield and reduced SET voltage upon inserting a graphene layer under the top electrode, attributed to elimination of undesired surface effects[9]. While these studies do indeed show resistive switching, the demonstration of a bipolar, all-graphene memory is still lacking. Such a device may hold the answer to

low-cost, low-power RRAM with high flexibility if the lack of reversible switching can be overcome. To approach this problem consider we that the combination of GO with a low work-function, reactive electrode such as Ti, Al or Cr gives repeatable bipolar switching which can be attributed to reversible reduction-oxidation processes that occur between the GO layer and top electrode, as observed for titanium. The study of Lee et al. also suggests that platinum ($\Phi = 5.64$ eV) may be replaced with a low work-function material like graphene ($\Phi = 4.56$ eV) without losing the resistive switching effect. With this in mind, the use of a bottom graphene electrode with reactive aluminium top electrode is investigated.

First, graphene is inserted into an Al-GO-graphene (top to bottom) stack, fabricated on SiO_2. In this device a long and thin graphene bottom electrode is patterned on SiO_2 using a hard silicon mask to avoid resist contamination. Next, several GO thin films are transferred to the graphene bottom electrode using vacuum filtration - here multiple transfers eliminate pin-hole shorting in the films. An aluminium top electrode is then thermally evaporated onto the GO thin film through a shadow mask. Finally the graphene electrode is capped with Cr/Au for making electrical contact. Figure 5.7 shows the typical switching characteristics, with a DC bias applied to the top aluminium electrode. As with Al-GO-Al devices, the virgin-state was of high resistance (see appendix for Al-GO-Al switching). It can be seen in Figure 5.7(a) that upon application of positive bias (Al) the device switches from the HRS to LRS at +1.7 V, showing an memory window of upto $\sim$ 10 times ($V_{read} = 0.5$ V). Then, upon application of a negative bias, the device switches back from HRS to LRS at $\sim$ -2 V. The immediate jump observed for the SET process and gradual RESET is consistent with formation and rupture of conducting filaments. The switching is repeatable for several cycles, with some slight variation in switching voltage, as shown in Figure 5.7(b). It is also noted that no compliance resistor was used for the initial device without observing permanent breakdown, this is likely due to the relatively high resistance of the graphene bottom electrode ($\sim$ 5 kΩ). Interestingly, and in contrast to Al-GO-Al devices (both those fabricated in house and those reported in the literature), the SET process occurs for application of a positive bias to the top aluminium electrode, opposite to the previously reports of Sung et al., who observe the SET process for application of a negative bias to the top aluminium electrode.

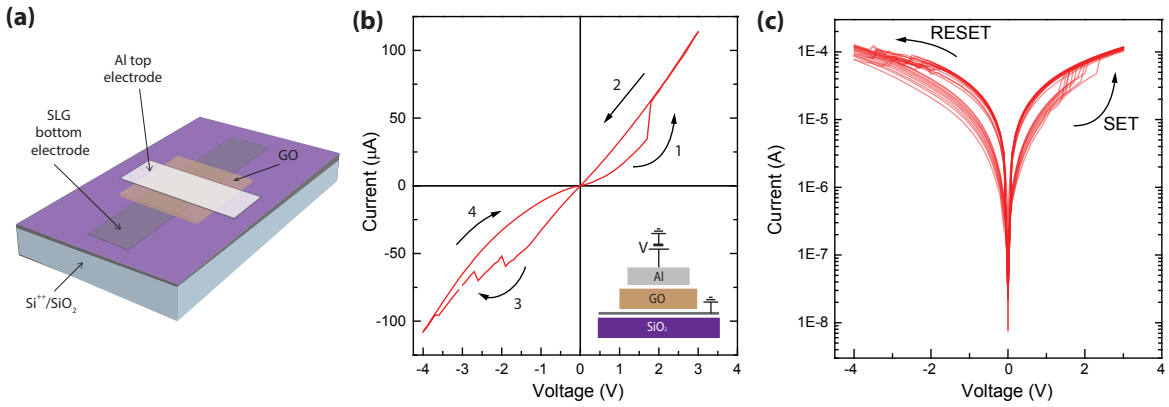

Figure 5.7: (a) Typical current-voltage characteristics for an Al-GO-graphene device where the bias is applied to the aluminium top electrode with the graphene grounded. (b) Cycling of the same device with area (500 × 500 μm) showing repeatable, reversible switching.

5.6 GRAPHENE AS A FLEXIBLE/STRETCHABLE ELECTRODE

Next, the performance of graphene on both flexible and stretchable substrates is investigated. In a home-built setup the response to mechanical strain was investigated; 1) the change in resistance during stretching/bending and 2) the change in resistance over several cycles. It is noted that in most reports of flexible graphene electrodes the resistance during cycling is overlooked. However, for use in end-user applications such as wearable technology it is of course crucial that the device performs when under strain. Further that trends in the related research suggest the increased importance of developing electrodes that are compatible not only with flexible substrates but also stretchable ones. With this in mind, few-layer graphene grown by CVD is transferred to two flexible substrates; one flexible plastic (125 μm PET) and one stretchable elastomer (PDMS). Figure 5.8(a) shows a sheet of FLG on a polydimethyl siloxane (PDMS) substrate, where the inset illustrates the typical deformation obtained under stretching. Following transfer the device is loaded into a home-built stretching rig and probed electrically while subject to repeated stretching cycles. Electrical contact is made with conductive silver paste and the two-terminal resistance measured with a Keithley 2400 source-meter. Figure 5.8(b) shows the resistance measured during several stretching cycles, where the maximum resistance was measured at the point of largest extension, for an approximate extension/length of

$\sim$ 2 %. Figure 5.8(c) shows the resistance after 100 cycles, where it is important to note that the observed increase in resistance is due to poor adhesion of the silver contacts. Next, a similar experiment was performed for a bendable plastic substrate (PET). Figure 5.8(d) shows the graphene on PET loaded into a home-built bending-rig. The resistance during cycling and resistance after 100 cycles is plotted in Figure 5.8(e) and (f). Both for stretchable and bendable substrates the graphene showed little change during the strain cycle and negligible change (channel) after 100 cycles. This shows that few-layer graphene grown by CVD is suited for both substrate materials and highlights the importance of developing compatible contact materials, as in both cases it was found that it was the metal contacts that degraded rather than the graphene channel.

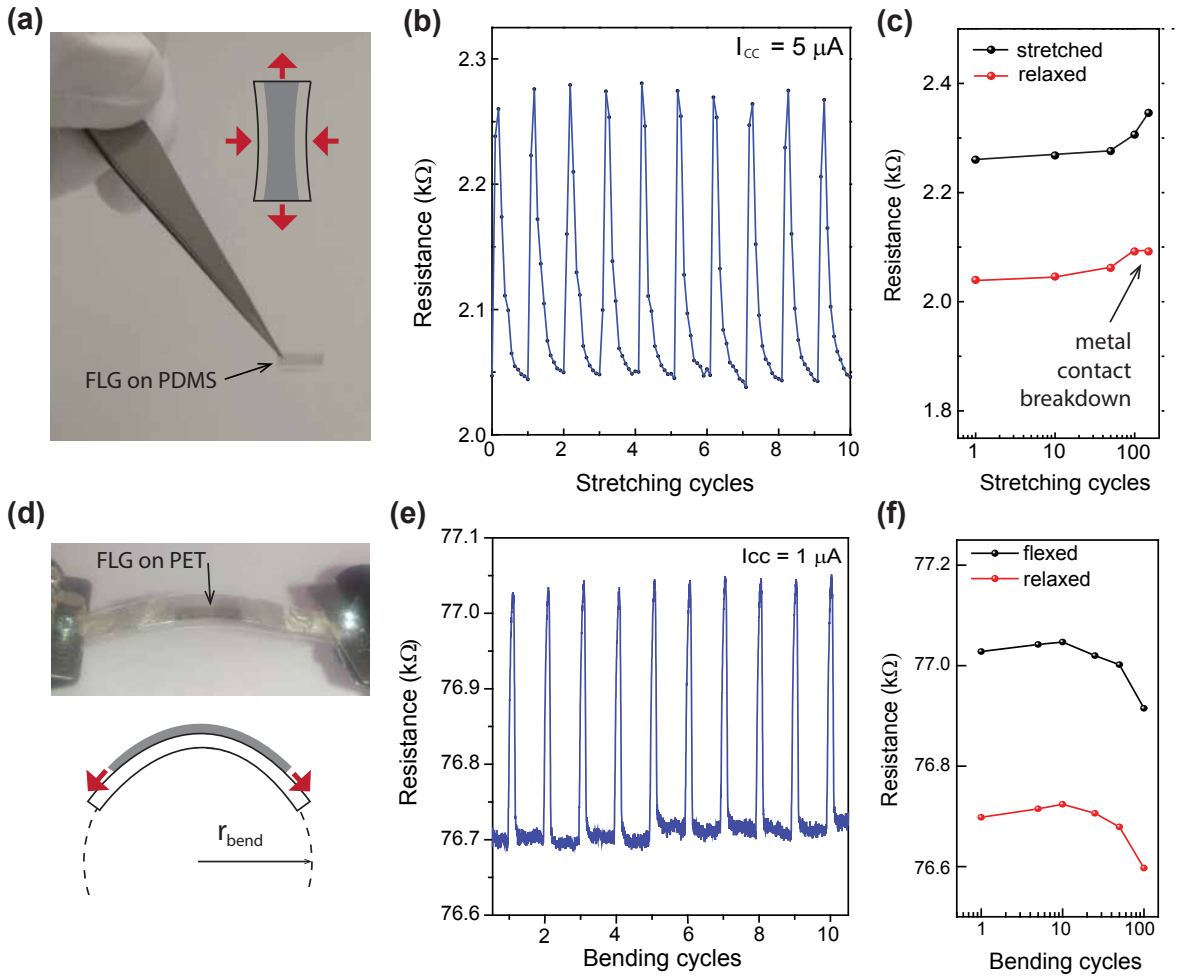

Figure 5.8: Performance of graphene on stretchable and bendable substrates (a) Photograph of few-layer graphene on stretchable PDMS substrate, (b) resistance of graphene during several stretching cycles and (c) the resistance of over 100 cycles (d) Photograph of graphene on PET in the jaws of a home-built bending-rig (e) resistance during several banding cycles and (f) the flexed and relaxed resistance over 100 cycles.

5.7 PERFORMANCE OF FLEXIBLE AL-GO-GRAPHENE RERAM DEVICES

The rigid device structure was then combined with the flexible graphene electrode. Al-GO-graphene devices were fabricated on PET substrate as shown in Figure 5.9(a). Here the long-thin device consists of one common gaphene bottom electrode with several top Aluminium electrodes. Devices were fabricated as part of a cross bar-array. However

for characterisation the array is then separated into individual strips to avoid cross-talk (sneak-paths between SET cells). Devices are characterised using simple two-terminal DC current-voltage cycles using a Keithley 2400 source-meter with a current compliance of 100 μA, in order to preserve the switching effect for many cycles. Devices fabricated on PET show almost identical switching characteristics to those fabricated on the SiO_2, with the devices initially in the HRS showing forming-free behaviour. The typical switching characteristics are shown in panels (b) and (c) of Figure 5.9. Application of an increasing positive bias to the aluminium top electrode results in a non-linear increase in drain current. Then at $\sim$ 2 V the device shows an abrupt switching to the LRS. While sweeping the voltage back through 0 V the device maintains a LRS until reaching $\sim$ -2.5 V when the device gradually switches back to the HRS. The combination of the abrupt SET process and gradual RESET process is typical of filamentary behaviour, and is consistent with devices fabricated on SiO_2. Just as for devices fabricated on rigid SiO_2 substrates, the SET process occurs when a positive bias is applied to the top Al electrode. Devices show switching over many cycles with easily distinguishable HRS and LRS, which is extracted at V = 200 mV. After an initial characterisation the devices are subject to repeated cycling. Figure 5.10(a) shows a semilog plot of 50 switching cycles. The SET voltage showed some mild variation but was always observed above 1 V. Devices showed stable cycling over 500 cycles with some degradation of memory window (reduced to $\sim$ 10).

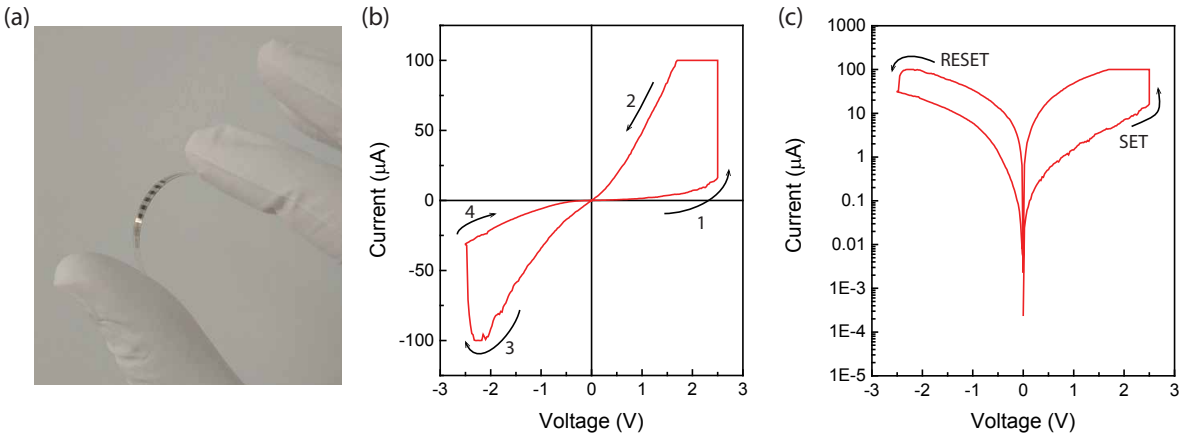

Figure 5.9: (a) Al-GO-FLG device stack fabricated on flexible PET substrate (b) Typical current-voltage characteristics of one cell measure in air with 100 μA current compliance (c) Semi-log plot of the data in panel (b).

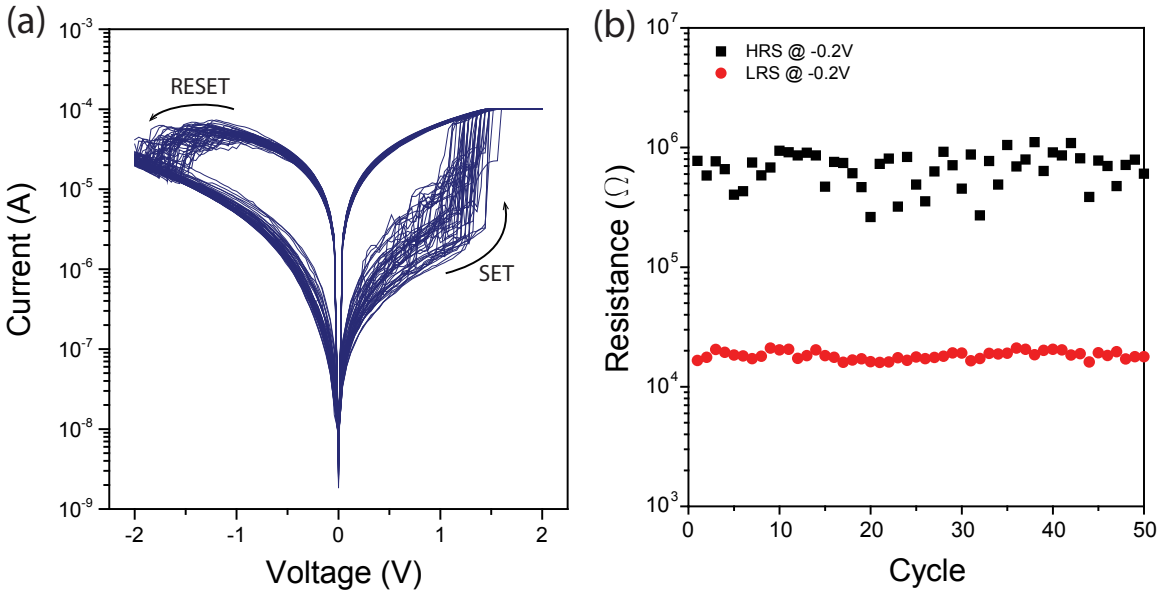

Figure 5.10: (a) Semi-log current-voltage characteristics of 50 switching cycles (b) extracted HRS and LRS from the cycles shown in (a).

5.8 CONCLUSIONS

In conclusion the resistive switching in GO thin films is investigated, with particular attention paid to testing the ultimate performance in an optimised device structure. Flexible devices based on hybrid Ti-GO switching layer exhibit a memory window of 10^2 for $> 10^3$ cycles and $> 10^5$ seconds. Devices also show additional functionality, operating for over 10^3 bending cycles and capable of storing multiple bits (4 resistance states). The flexible device presented here represent to the best of our knowledge the highest performance to-date for GO ReRAM. The mechanism of resistive switching is investigated and ascribed to the formation of an interface layer between titanium and GO upon deposition of the top electrode. Titanium's high affinity for oxygen is believed to act as a reservoir for the back and forth exchange of oxygen with the GO layer, supported by Raman, XPS, electrical transport and MD simulation[5]. This result suggests that the combination of graphene oxide with a reactive top electrode is key for high performance, similar to resistive memory devices based on other oxide layers. As such graphene is inserted as a bottom electrode owing to its mechanical flexibility in an Al-GO-graphene structure on flexible substrates,

showing repeatable bipolar switching. This is an important step towards an all-graphene resistive memory device.

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6

OXIDISED HAFNIUM DISULPHIDE DIELECTRICS FOR FETS AND RESISTIVE SWITCHING DEVICES

6.1 INTRODUCTION

Laser assisted modification of 2D materials - specifically the creation of oxides for resistive switching devices and high-κ dielectrics has, to the best of our knowledge, not yet been demonstrated. The possibility to write high-κ dielectric material into a semiconducting channel or Van der Waals heterostructure has numerous possible applications including as a tunnel barrier, gate dielectric, charge trap layer or resistive switching material. It was recently discovered by our group that upon laser exposure, layers of HfS_2 may be oxidised in ambient conditions for use in optoelectronic devices[1]. Hafnium dioxide as a gate dielectric material is one of the most promising oxide materials for use in high performance CMOS MOSFETs. The use of high-κ dielectric materials for gate stacks in CMOS fabrication is becoming increasing common due to several limitations associated with conventional SiO_2 gate. Most notable perhaps is the large leakage currents as a result of direct tunnelling in ultrathin ($\sim$ 2-3 nm) layers[2]. The high relative dielectric constant of HfO_2 ($\kappa = 25$[3] & $E_{gap} = 5.8$ eV) means increased capacitance for ultrathin layer ($C = \frac{\kappa\varepsilon_0 A}{thickness}$). Further, use of HFO_x in resistive ReRAM devices is well established with several groups showing extremely high performance[4]. Fully optimised CMOS-integrated HfO_x

device stacks exhibit upto 5 ns switching speeds[5], 10×10 nm^2 cell area[6], 10^3 ON/OFF ratio and endurance over 10^6 cycles[7]. The interest in reversible resistive switching in layered materials is growing with recent reports of bipolar resistive switching in CVD-grown hBN[8]. The incorporation of conventional ReRAM materials into flexible devices is limited due to the weak adhesion between the component layers, resulting in failure upon rigorous mechanical flexing. Further, the layered structure of 2D materials could offer a route to ultra-thin devices, just a few atoms thick.

In this chapter I present a study on the use of photo-oxidised hafnium disulphide (HfS_2) as a dielectric layer in FET and ReRAM devices based on 2D-materials and Van der Waals heterostructures. Upon exposure to laser-light in ambient conditions it is shown that the HfS_2 can be controllably oxidised. Upon optimisation of the oxidation of HfS_2 it is found that there is a fine window in terms of power density between oxidation and ablation of material. I demonstrate that this technique may be used to write insulating oxides in 2D-semiconductor stacks by fabricating FET devices incorporating a graphene gate electrode with oxidised HfS_2 gate dielectric for electrostatic gating of graphene and MoS_2. It is found that the oxide formed is composed of hafnium oxide, however further studies (under-way) are needed to establish the precise stoichiometry and physical structure. Next the resistive switching characteristics of oxidised HfS_2 is investigated using a configuration with a reactive metal (Cr/Au) as the top electrode and few-layer graphene as the bottom electrode which shows bipolar resistive switching. Finally I investigate ReRAM based on the incorporating oxidised HfS_2 and graphene electrodes into a VdW-heterostructure. It should also be noted that upon preparation of this chapter I became aware of a similar work of Mleczko *et. al* from the group of Eric Pop in Stanford[9], however the devices demonstrated, materials used and method for oxidation are entirely different.

6.2 EXPERIMENTAL

Devices are fabricated using a standard dry transfer technique outlined in Appendix A. First, flakes of graphene/graphite are exfoliated using tape and transferred onto a SiO_2-Si^{++} substrate after treatment with oxygen plasma which was performed using a JLS reactive ion etching system with 30W power for 30 seconds at 20 mT pressure. Next, a bulk crystal of HfS_2 is exfoliated using a PDMS stamp. A suitably thin and uniform flake is identified with optical microscopy and then transferred onto the graphene

flake. At this point devices are either completed with a metal top electrode or a second graphene/graphite electrode is stamped on top of the HfS_2 forming the top electrode of the VdW heterostructure. Electrical contact to the graphene electrodes is made by patterning a PMMA mask with electron-beam lithography followed by thermal evaporation of 50/5nm of Cr/Au. Finally the device is scribed and wire-bonded into a 5 $\times$ 5 mm leadless chip-carrier package. Measurements of devices are performed in a home-built dipping-probe in the neck of a helium Dewar (T $\sim$ 270 K). DC electrical measurements of the vertical stacks are made using either a Keithley 2400 source-meter, or combination of a Xitron Voltage source, Femto DLCPA-200 current amplifier and Agilent 3410A Voltmeter. Laser assisted photo-oxidation is performed in a home-built laser microscope system using a fibre coupled 532nm excitation source through a LWD 50x objective described in[10]. The power density is on the order of 5 mW μm^{-2}, higher powers result in apparent ablation of the material.

6.3 CONTROLLED OXIDATION OF HFS_2

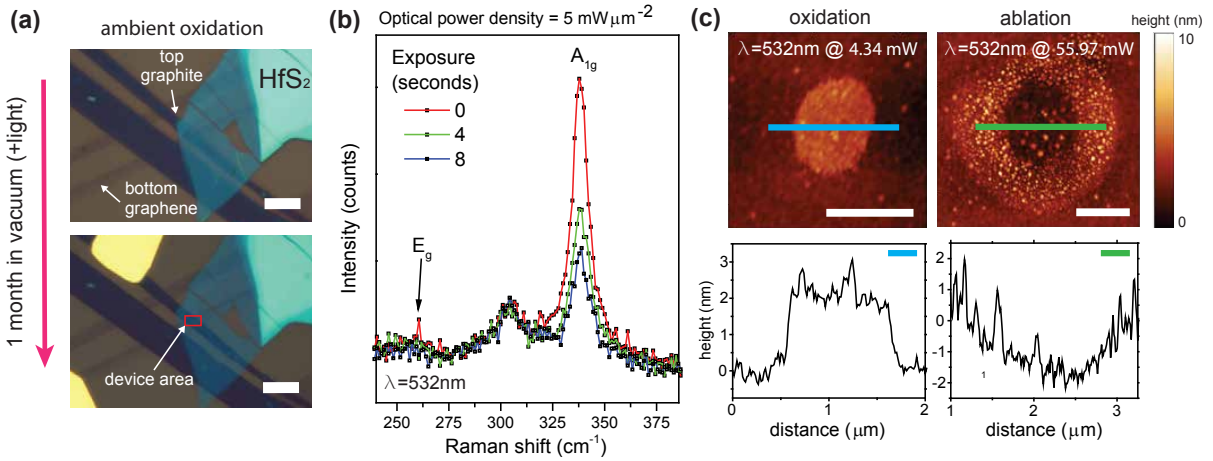

Figure 6.1: (a) Evolution of natural oxidation over 1 month for a sample stored in mild vacuum, scale bars are 5 μm. the HfS_2 layer in the bottom image has become more transparent compared to the top image, which is consistent with the conversion from a semiconductor to an oxide (b) Shows the evolution of the characteristic HfS_2 Raman spectra for laser exposure time - consistent with oxidations (c) shows an AFM topography of HfS_2 after exposure to laser light of two different powers, showing oxidation (left) and ablation (right). Scale bars in panel (c) 1 μm.

The formation of a native oxide on HfS_2 upon exposure to ambient conditions has been reported previously by Chae *et. al*[11] who observe a reduction in contrast after several hours as well as the formation of localised residues on the surface of the flakes. Upon exfoliation and preparation of flake stacks a similar effect is observed, which can be reduced by storage in vacuum/dark conditions. Figure 6.1(a) shows a graphene-HfS_2-graphite stack before and after device processing and storage in mild vacuum (sample desiccator). The small reduction in contrast is consistent with oxidation. It was found by our group that upon exposure to intense laser light, the rate of oxidation could be increased for use in optoelectronic applications. Using this as a starting point I first develop the controlled oxide formation. An optical power density of ~ 5 mW μm^{-2} was found to give optimum results for thin flakes (< 10 nm), which can be directly observed as the decay of intensity of the characteristic Raman peaks with exposure time, shown in Figure 6.1(b). Oxide

formation resulted in a slight increase in flake thickness, as shown in the left panel of Figure 6.1(c) - consistent with conversion of crystalline HfS_2 to an amorphous oxide. Higher powers (> 15 mW μm^2) resulted in ablation of material, which was measured as small pits in the material after laser exposure, right panel in Figure 6.1(c). It was also noted that the electrical properties of these laser-thinned regions do not show the same insulating behaviour as for the lower optical powers, measured using C-AFM. The characteristic Raman-active bands, E_g at 260 cm^{-1} and the A_{1g} at 338 cm^{-1} are clearly identifiable and both show strong reduction in intensity with increasing laser exposure[12]. Within the resolution of the instrument (Renishaw Raman system) the E_g is no longer visible after 8 seconds of exposure, while the stronger A_{1g} mode saturates, suggesting either incomplete oxidation (spatially) caused by to the decay of optical power with Gaussian spreading of the beam. For all samples, after ~ 10 seconds direct laser exposure, the white-light optical contrast reduces until almost negligible. Unless stated otherwise the devices presented in this chapter are oxidised using $\lambda = 473$ nm, with measured optical power of 4.3 mW focussed through a LWD 50x objective. Assuming the Abbe limit this corresponds to an optical power density of 11.7 mW μm^{-2}.

6.4 OXIDISED HFS_2 AS HIGH-κ GATE DIELECTRIC

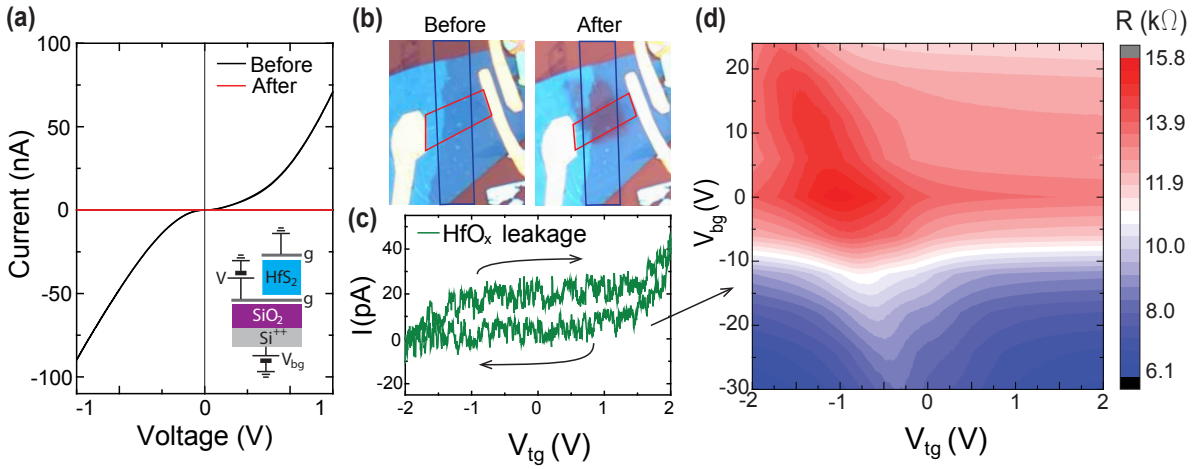

Figure 6.2: (a) DC current-voltage characteristics for a graphene-HfS_2-graphene stack before and after laser-assisted oxidation. Inset illustrates measurement arrangement (b) optical microscope image of the same device before and after oxidation where the blue and red boxes show the position of the graphene top and bottom electrodes, the region where the electrodes cross is oxidised (c) Measured DC leakage current through the HfO_x obtained during the dual-gating measurement (d) Colour map of four-terminal resistance of the graphene channel for sweeping Si^{++} bottom-gate and graphene top-gate, measured in four-terminal AC with zero-bias at T = 4.8 K.

Typically HfO_2 for CMOS is deposited using atomic layer deposition. Here I develop the oxidation to selectively oxidise material within a VdW-stack. Attempts to measure thin HfS_2 transistors with their native dielelectric resulted in inconclusive results, as the oxidation effect appeared to continue with increased exposure to ambient conditions, consistent with reports from other groups who suggest encapsulation to slow the degradation[11;9]. To examine the use as a gate dielectric, I fabricated devices consisting of graphene-HfS_2-graphene. The tunnelling characteristics are measured immediately after fabrication and then the devices are subject to laser-assisted oxidation and re-measured shown in Figure 6.2(a). In these measurements one graphene electrode is voltage biased with respect to the other and the current through the HfS_2 measured. As fabricated the device shows the non-linear current-voltage typical of tunnelling behaviour. Then, laser-assisted oxidation

is performed on the sample. Interestingly it is observed that the HfS_2 may be oxidised through the top graphene electrode. This opens up a host of possibilities for writing dielectrics at specific positions in a VdW-stack. Optical microscope images of the device before and after laser-asisted oxidation are shown in Figure 6.2(b). After oxidation, we observe almost zero DC-current over the same measured range and note that both top and bottom graphene electrodes show the same values of 4-terminal resistance providing evidence that the graphene electrodes are not damaged during laser-exposure. Further, the optical densities used are well within the safe limits for probing graphene. Next, dual-gating of the bottom graphene layer using the Si^{++} substrate and the top graphene as respective back and top gate electrodes is performed. The measurements are performed dipped in liquid Helium in 4-terminal constant current configuration at zero-bias ($V_{drop} < 360\ \mu V$). The gate voltages are applied with a DC voltage source and the leakage currents measured. Figure 6.2(c) shows the measured leakage of the oxidised HfS_2 across the entire measured range ($\pm$ 2 V). It is negligible and shows a hysteresis loop typical of capacitive displacement current. Figure 6.2(c) shows a colour map of graphene channel resistance measured for sweeping top and bottom gates. Modulation of the Fermi level is achieved with both top and bottom gates, where the back gate shows a stronger gate response. This is most likely due to the device geometry - as the top gate does not cover the entire channel area which would result in non-uniform gating of the channel. However all of these measurements support the formation of oxidised HfS_2 and we demonstrate for the first time its use in a dual-gated graphene FET.

Next the laser-oxidised HfS_2 is applied as a gate dielectric in an MoS_2 FET. This time the device consists of a graphene bottom electrode, on top of which is HfS_2, then MoS_2 is stacked. Finally Au/Cr contacts are made using standard device fabrication. Figure 6.3(a) shows the device before and after oxidation (red box), where this time the laser-assisted exposure is performed through the Au/Cr top electrodes. Again we observe a reduction in optical contrast with laser exposure. The lower part of Panel (a) shows the low-bias current-voltage characteristics for the device before performing laser-assisted oxidation, exhibiting a strong temperature dependence, suggesting that prior to oxidation transport through the graphene-HfS_2-MoS_2-Au stack is thermally activated. Following oxidation I then perform two-terminal DC transport measurements of the MoS_2 channel using the oxidised HfS_2 as the gate dielectric. Figure 6.3(b) shows a typical transfer curve collected for source-drain bias of 25 mV at T = 266 K. In ^{4}He atmosphere there is negligible

hysteresis for the up/down sweeps. The transfer curves are plotted on a semi-log scale in Figure 6.3(c) for several values of source-drain bias, showing typical MoS_2 FET behaviour across an applied gate voltage range of 3.5 V. The measured $I_{ON/OFF} = 10^3$ is lower than the ideal values likely due to poor injection of the gold contacts[13]. This could be addressed in future devices however is outside the scope of the study. The subthreshold swing of devices measured was extracted as ∼100 mV dec^{-1}, and the mobility estimated to be ∼1 $cm^2V^{-1}s^{-1}$ for few-layer MoS_2 The inset shows the measured leakage current in through the oxidised HfS_2 is ∼ 1 % of the measured drain current suggesting minimal leakage. We note the interesting voltage dependence of the leakage current and suggest it may be caused by incomplete oxidation when performing laser exposure through the Au/Cr contacts.

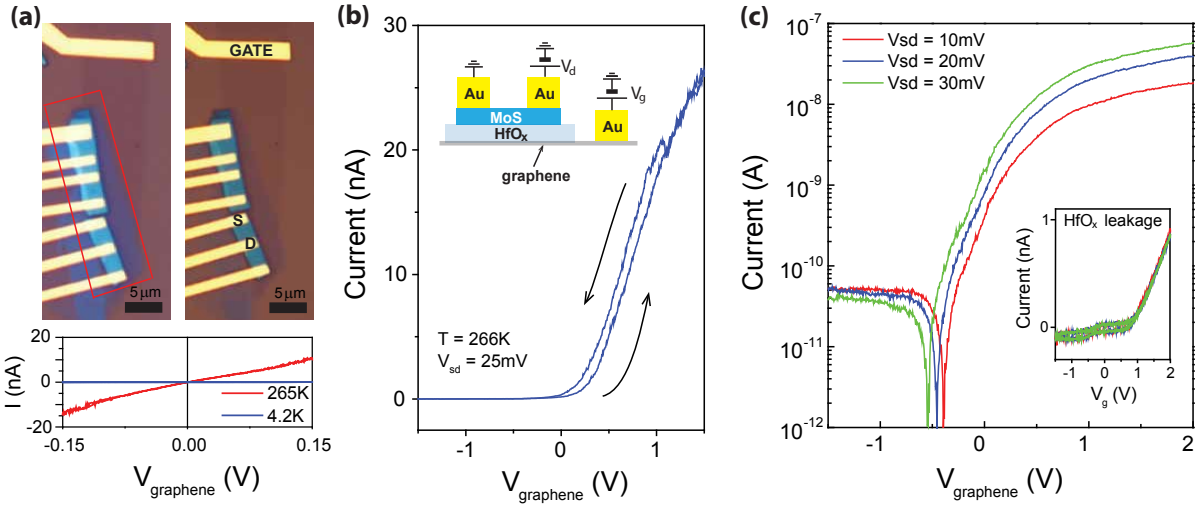

Figure 6.3: (a) Optical microscope image of an MoS_2 FET utilising oxidised HfS_2 as the gate dielectric and graphene as the gate electrode, S and D indicate the source and drain electrodes used for electrical measurements. (b) device schematic and transfer characteristics measured for V_{SD} = 25 mV at T = 266 K in a ^{4}He atmosphere (c) Semilog transfer characteristics for several values of V_{SD}, the inset shows the measured leakage current of the oxidised HfS_2.

6.5 RESISTIVE SWITCHING IN OXIDISED HFS_2

Turning now to resistive memory devices we investigate resistive switching in HfS_2 after oxidation. First, devices consisting of graphene-HfS_2-metal are fabricated, making use of a reactive metal for the top electrode as it is the most likely to show switching behaviour. Figure 6.4(a) shows the current-voltage characteristics of the first device, measured using conductive AFM. This technique was chosen as a starting point due to the ease of fabricating several devices, where HfS_2 is exfoliated onto a blanket gold substrate. After identification of suitably thin flakes EBL is used to pattern small disc-type top electrode pads. For these devices the top electrode consists of Ti/Au (5/50 nm), deposited by electron beam evaporation. Measurements are performed using a DLC-tip in a Bruker Innova system. For application of a positive voltage to the bottom gold electrode, a switch at $\sim$ 2 V from the HRS to LRS, followed by a switch back from LRS to HRS for $\sim$ -2 V is observed. The sharp SET and gradual RESET are typical of formation/rupture of conducting filaments. We also note that the device shown in Figure 6.4(a) required no forming step and was observed on a native-oxide region (not laser-assisted), suggesting the resistive switching effect may occur in a very thin portion of material. Next, cross-bar devices are fabricated using graphite as a bottom electrode as the first step towards Van der Waals ReRAM. Here the top electrode consists of Cr/Au (5/50 nm). Both titanium and chromium are chosen due to their reactivity and high number of oxidation states, which has been shown to enhance switching performance by stripping oxygen from the HFO_x [14]. Figure 6.4(b) shows the current-voltage characteristics over 100 cycles (plotting every 10 for clarity). For the same voltage polarity as the first device, the SET process is observed for $\sim$ 1.3 V and the RESET process for $\sim$ -1 V. For this device the stability of the LRS and HRS are measured (as current) for a constant voltage = 250 mV over several hours, as plotted in Figure 6.4(c). Both states are stable over 10^5 seconds, showing no observable change in resistance. However, the memory window in such devices is very low (< 2), likely due to overly-large SET compliance or fewer oxidation states available in chromium compared to titanium. Both for titanium and chromium top metal electrodes reversible resistive switching is observed, both for native oxidise and laser-assisted oxide HfS_2. Devices with reactive metal top electrodes show bipolar switching with current-voltage characteristics typical of the formation and rupture of conductive filaments. Cross-sectional TEM of the switched area would no doubt add to the picture

of the switching mechanism.

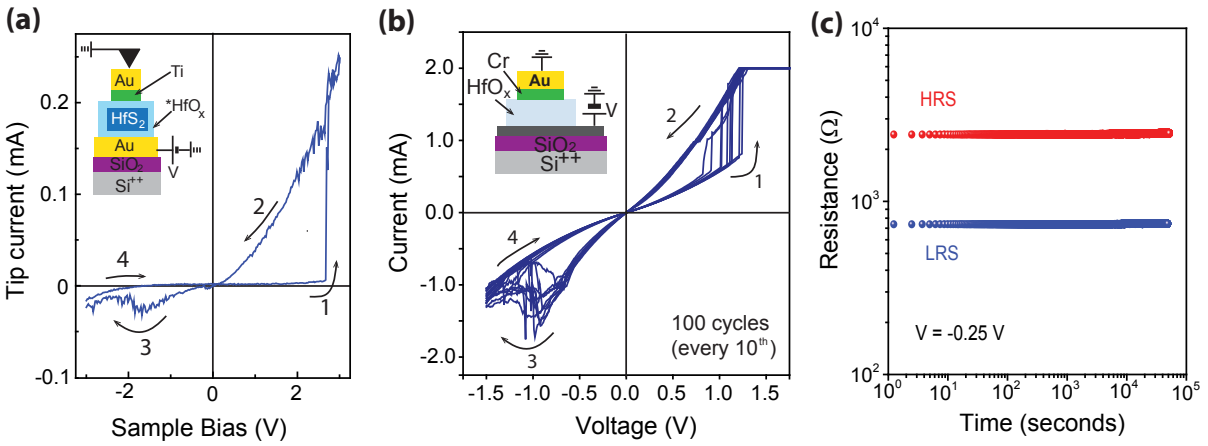

Figure 6.4: Typical current-voltage curves for (a) Au-Ti-HfS_2-Au devices measured with C-AFM and (b) 100 switching cycles of a Au-Cr-HfO_x-graphene measured in ^{4}He atmosphere. (c) Time stability of resistance levels for the device shown in panel (b) at fixed drain bias, V = 250 mV.

Finally, resistive switching in oxidised VdW-heterostructures is investigated. Here, devices are fabricated in much the same way as those in Figure 6.4(b) but instead using a graphite or graphene top electrode which is then contacted with Cr/Au electrodes. For all devices measured resistive switching, however for devices based on graphene electrodes the switching does not appear as robust as for a metal top electrode. Figure 6.5(a) shows several current-voltage curves of the graphene-HfS_2-graphene device (same as the device used to measure dual-gating of graphene earlier in the chapter after a forming step was used to initiate switching). Several current-voltage sweeps are plotted which show several uncontrolled jumps between a HRS and LRS within $\pm$ 1V, exhibiting a memory window of $\sim 10^3$. Such unreliable behaviour can be attributed to unstable filament formation due to the missing electrode asymmetry, specifically the lack of a highly oxidising electrode material to act as an oxygen reservoir between cycles. Figure 6.5(b) shows the current-voltage characteristics of a graphene-HfO_x-graphite stack, typical of a write-once-read-many (WORM) device, where switch from HRS to LRS was observed at $\sim$ -1.25 V. The resistance levels for this device are stable over 10^4 seconds for the HRS and LRS shown in panel (b), where the three resistance levels correspond to the HRS, LRS (soft-set) and LRS (hard-set).

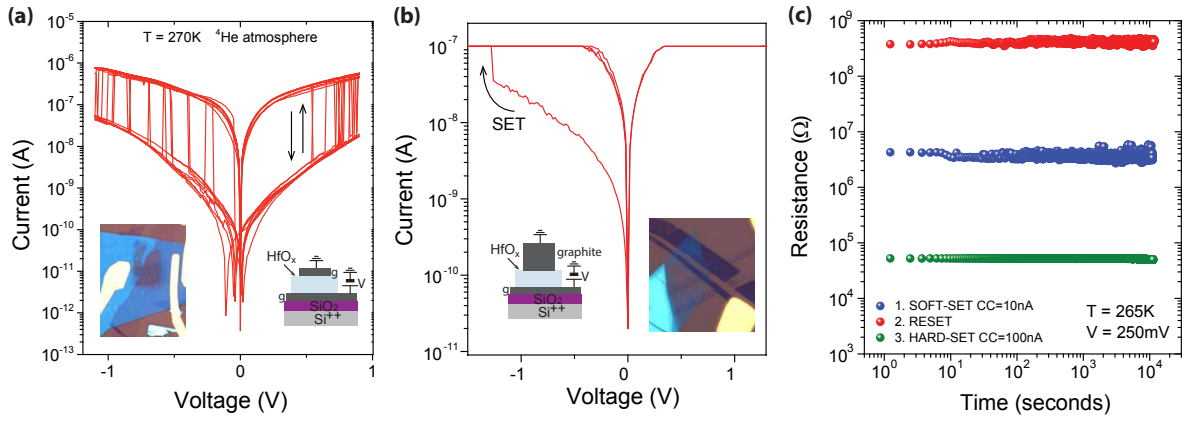

Figure 6.5: Current-voltage characteristics of VdW ReRAM showing (a) unstable filament formation/rupture measured and (b) Write-once memory operation. (c) Resistance levels for the device shown in panel (b)

6.6 CONCLUSIONS

In this chapter the controlled oxidation of HfS_2 is developed for incorporating as a dielectric layer FETs and ReRAM devices based on 2D-materials and VdW heterostructures. The controlled oxidation of material is found to occur in ambient conditions as previously reported[11] and may be accelerated with exposure to high intensity laser-light. The oxidised material is then incorporated into FET devices based on graphene and MoS_2. For both devices we are able to achieve electrostatic gating over a small gate voltage range ($<$ 5V). Devices based on few-layer MoS_2 show an ON/OFF ratio of 10^3 and sub-threshold swing approaching 60 mV decade^{-1}. ReRAM devices based on oxidised HfS_2 show bipolar switching when used in combination with a reactive metal top electrode, with resistance levels stable over 10^5 seconds. Finally we investigate the resistive switching in VdW heterostructures with graphene/graphite electrodes. Resistive switching in such devices is less robust than for the reactive metal counterparts, with no clear observation of bipolar behaviour. We ascribe this to the lack of asymmetry in the electrodes, specifically the lack of an oxygen reservoir resulting in permanent removal of oxygen from the HfO_x. To the best of our knowledge this is the first demonstration of using oxidised HfS_2 in VdW heterostructures for a dielectric and switching material.

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7

FLEXIBLE GRAPHENE-BASED SENSING ELEMENTS

7.1 INTRODUCTION

Graphene-based sensors have several advantages for over currently available technology, including optical transparency, tunable sensitivity and mechanical flexibility which make them ideally suited for imperceptible wearable electronic components for consumer electronics and medical applications[1]. The growing field of robotics and functional prosthetics will no doubt drive demand for combined touch, pressure, temperature and humidity sensitive artificial skins mimicking that of the human body[2] and when considered with the forecast market-share increase for flexible electronics[3], the requirement for flexible and transparent sensing elements is clear. Current technologies for health monitoring systems are often not appropriate for developing non-invasive wearable sensors for soft interfaces such as the skin. The mechanical properties of the skin is unlike those of conventional

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[††]Parts of this chapter have been published in: A.M. Alexeev, M.D. Barnes, V.K. Nagareddy, M.F.Craciun & C.D. Wright, *A simple process for the fabrication of large-area CVD graphene based devices via selective in situ functionalization and patterning.* 2D Materials 4 (1), 011010

[‡]XPS measurements and analysis presented in this chapter was perform by Dr. V.K. Nagareddy and included with his permission

electronic devices based on rigid silicon wafer substrates. Development of silicon membranes and/or chips embedded in flexible polymers show progress[4;5], however there is still a mismatch between such devices and the skin. The use of graphene and other two-dimensional materials with intrinsic flexibility may allow for the development of multifunctional, wearable devices with a closer match in mechanical properties allowing for imperceptible health monitoring devices.

In this experimental chapter the selective patterning/processing of sensing elements based on graphene grown by chemical vapour deposition (CVD) directly on the CVD growth substrate is developed. As discussed in chapter 4, the most commonly use growth substrates for CVD graphene are copper and nickel. Direct patterning the CVD graphene on the copper/nickel provides a solution to the problem of incompatibility between flexible plastic substrates and organic solvents commonly used in processing. Using this technique a flexible graphene-based touch sensor and oxygen-functionalised graphene humidity sensor are demonstrated. This novel process offers a versatile tool for the fabrication of graphene-based sensing elements. Such a technique could expanded upon to fabricate multiple sensing elements based on a common CVD graphene-backbone.

7.2 FABRICATION OF DEVICES

When considering the possible fabrication platform for graphene sensor elements I developed a method to process devices entirely on the CVD-growth substrate, such a processing technique could be implemented in roll-to-roll manufacturing, where the graphene on copper foil could be passed from one process to the next via mechanical roller[6]. Figure 7.1 outlines the fabrication process for devices on the copper growth substrate. First, graphene grown by cold-walled CVD on copper is covered with a 200 nm thick polymethyl-methacrate (PMMA) resist followed by electron beam lithograpy for definition of contact pads or etch/functionalisation masks, shown in (a). For contact pads, thermal evaporation of Au (5/50 nm) is used followed by the subsequent lift-off procedure in warm acetone then iso-propyl alcohol (IPA) shown in (b). Unlike SiO_2, it is found that gold wets well directly on CVD graphene, and yields low contact resistance. For graphene etching/functionalisation a JLS reactive ion etching system is used. For etching graphene the sample is placed directly in the stream of a 30 W oxygen/argon plasma. For functionalisation a significantly milder oxygen plasma (5 W) was used and the sample is placed

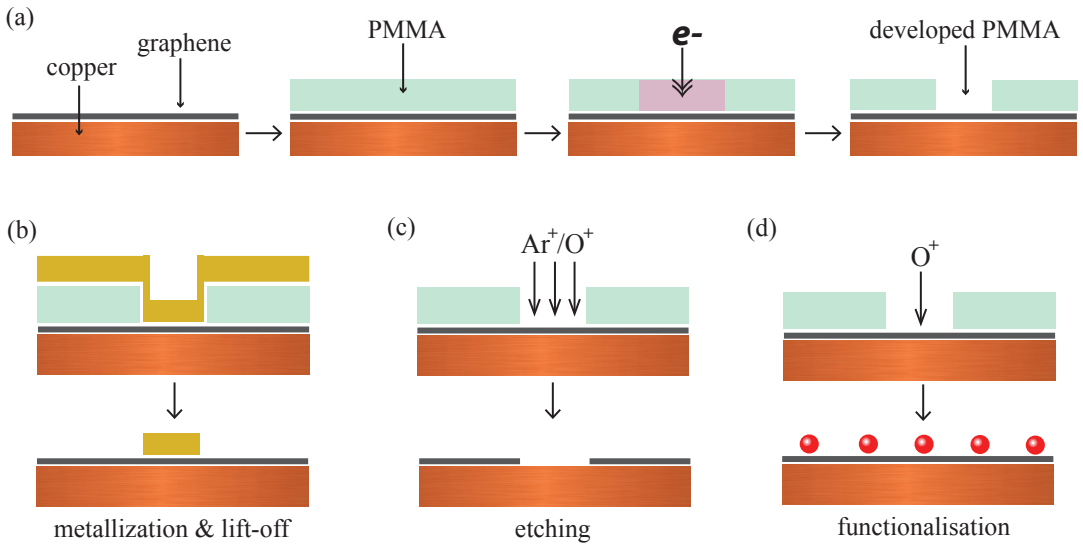

Figure 7.1: Process flow diagram for on-copper fabrication of CVD-graphene devices. (a) shows standard electron beam lithography procedure with positive PMMA resistive followed by developing in (15:5) MIBK:IPA mixture. Following lithography, 3 subsequent processes are used depending on the specific device including (b) metallisation of contact pads, (c) etching of graphene structures and (d) selective plasma-functionalisation of graphene.

out of the plasma stream where oxygen radicals have significantly lower energy, reducing damage by ion bombardment[7]. After device processing, the graphene device is transferred to a flexible substrate using PMMA-supported wet etching of the copper substrate with ammonium persulphate (APS).

7.3 TOUCH SENSOR

7.3.1 *Introduction*

Electronic detection of human touch is becoming increasingly a part of modern day-to-day life. Smart phones, tablets and laptops rely on optically transparent sensors to determine the position and strength of the interaction with the human hand[8]. With this in mind a novel capacitive graphene-based touch sensor is presented, made up of an array of touch sensitive elements on a flexible and transparent plastic substrate.

Common to all touch screen technologies are optically transparent and conductive elec-

trodes. For such applications the conventionally preferred material is indium tin-oxide (ITO) owing to its ∼90% optical transparency and low sheet resistance (∼50 Ω/□)[9]. However, for use in cheap, flexible electronics ITO is limited by poor mechanical flexibility[10] and costly deposition processes[11]. Graphene offers a convenient solution with comparable transparency (∼ 97% for single-layer graphene (SLG))[12], high mechanical flexibility[13] and comparable conductivity for highly doped samples (∼8 Ω/□)[14]. For design of a flexible graphene touch sensor the principle of operation for conventional touch sensors can be considered. Touch sensing arrays in mobile phones and tablets are most commonly projected-capacitive (e.g. Apple iPhone) and rely on the electric field of the human body to play the role of counter electrode. In such devices the electric field generated by a finger acts to disrupt the electric field of the system (as an additional ground) that is measured as a change in capacitance between two conductive electrodes (mutual capacitance) or between one electrode and ground (self-capacitance) Advantages of capacitive touch sensors include speed of operation, durability, optical transparency and multi-touch capability. Disadvantages include high cost (ITO) and reliance on conducting pointer (finger/stylus) for operation.

Incorporation of carbon materials into touch sensing arrays presents a route to potentially low-cost, low-impact flexible devices. Previous demonstrations include resistive pressure sensors based on CVD graphene[15;16] and graphene oxide[17;18], resistive strain sensors based on graphene foams[19] and nano-platelets[20] and more recently planar capacitive touch sensors[21]. Here, CVD-graphene is used as an electrode for an array of individually selectable graphene-polymer-graphene capacitor elements. It combines optical transparency, mechanical flexibility and position sensitive touch sensing for both insulating and conductive loads, making it potentially viable for integration into touch screens.

7.3.2 *Experimental*

The device consists of an array of graphene/polymer/graphene capacitor structures fabricated on the copper foil as outlined above. Each element consists of two CVD graphene electrodes separated by a thin polymer (PMMA) dielectric (∼ 500 nm). The system is modelled as a parallel plate capacitor, with two conductive plates separated by a thin layer of dielectric. The capacitance of each element is given by;

$$C = \frac{\epsilon_r \epsilon_0 A}{d} \rightarrow \Delta C = \frac{\epsilon_r \epsilon_0 A}{\Delta d} \tag{7.1}$$

where C is the capacitance, ϵ_r is the relative permittivity, A is electrode area and d is the separation of the conductive plates. For the devices fabricated, with ϵ_r=$\sim$ 2.8-4 for PMMA, A = 1 mm^2 and d$\sim$ 500 nm the capacitance is calculated to be $\sim$ 80 pF. Measurement of the capacitance between the two graphene layers makes this analogous to a mutually capacitive device, but the addition of a compressible polymer also allows for sensitivity to insulating loads. To test this an insulating load is applied ($\sim$36 g) to one element while the change in capacitance is measured at each element in the array. For response to touch, the device operates in purely mutually capacitive mode, where touching the device results provides additional ground, leading to a decrease in the capacitance between the separate graphene electrodes. It should be noted that the device did not show a reponse when touched (but not pressed) with a gloved finger, indicating the requirement of a conductive load for such operation. For measurements of capacitance a Hameg LCR meter is used, which operates on the principle of an automatic balance bridge. All devices were measured in two-terminal configuration, with 1 V AC voltage at 1 KHz. The low contact resistance (68 Ω)[22] of the devices mitigates this potential source of error in the measurement of impedance.

7.3.3 *Results & discussion*

Figure 7.2(a) shows an interpolated map of the change in capacitance of each element upon the application of an insulating 36 gram load on a single element (white arrow) resulting in an increase of the capacitance of around 4% for the loaded area. The observed increase in capacitance is consistent with compression of the PMMA dielectric upon loading. The measured value of capacitance was lower than predicted ($\sim$ 20 pF) and can be explained by the 'leaky' PMMA dielectric causing devices to operate as non-ideal capacitors (parallel RC). The repeatability of this change was low, likely due to the poor mechanical properties of the PMMA dielectric for subsequent loading cycles. A simple improvement would be through the use of an elastic polymer spacer (e.g. silicone elastomer). Next, the mutually capacitive response of the device is tested. Figure 7.2(b) shows the measured change in capacitance with time while periodically touching the device manually. Upon touching the sensing element a conductive finger acts an additional ground resulting in a reduction

in capacitance across the graphene-polymer-graphene capacitor. The measured change in capacitance was $\sim$ 6 pF and was highly repeatable with a fast response time of <500 ms, limited only by the measurement speed. Finally, the flexibility of the touch sensor is investigated, shown in Figure 7.2(c), by measuring the line resistance of the graphene electrodes for 2000 bending cycles. The device was repeatedly flexed over a plastic pipe of radius 2.5 cm. After 2000 bends a <2.7 % change in line resistance is observed, demonstrating the suitability of graphene as a flexible electrode material.

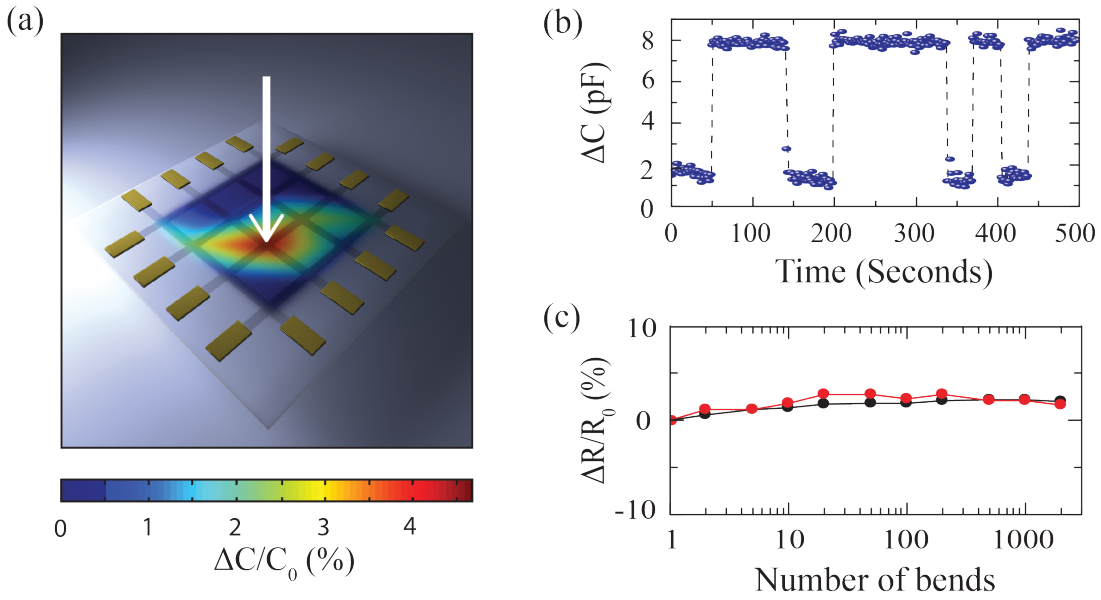

Figure 7.2: Characterisation of a capacitive graphene touch sensor array. (a) Interpolated map of the measured change in capacitance upon loading a single element (white arrow) with an insulating load of 36 g (b) Mutual capacitance of the two graphene layers, for periodically touch one element of the array (c) Relative change in line resistance for 2000 bending cycles with 2.5 cm bending radius. Adapted from[22].

In conclusion a flexible and transparent touch sensor is fabricated and characterised, enabled by a novel on-copper processing technique. The mutually capacitive response shows a measurable change for both insulating and conductive loads. Flexibility measurements show negligible degradation of electrode performance for 2000 bending cycles. The results suggest that graphene is a suitable alternative transparent conductive electrode for flexible touch screen applications.

7.4 HUMIDITY SENSOR

7.4.1 *Introduction*

Sensing and control of the surrounding environment is important in a number of applications. Many industrial processes rely on controlled environment for reproducible and reliable manufacture, due to humidity affecting many physical and chemical processes. Other applications include weather stations/balloons, personal comfort and medical equipment such as respiratory systems and incubators. Similar to touch sensors the future of artificial skins will also drive demand for imperceptible devices with high sensitivity and mechanical robustness. The interaction between graphene and moisture has been studied extensively from several perspectives not only for molecular sensing, but for chemical doping, improving FET performance, water desalination[23] and liquid-phase preparation[24].

7.4.2 *Mechanisms of humidity sensing in graphene devices*

The mechanism of operation for graphene-based humidity sensing is strongly dependent on the type of graphene used, as the interaction with water is strongly dependent on thickness and density of defects in the material. For clarity these are grouped into either surface or bulk effects. Graphene produced using mechanical exfoliation or CVD are very thin (<10 layers) and as such are dominated by surface interactions. Contrary to this, for graphene derived from wet chemical processes (graphene oxide, reduced graphene oxide, liquid-phase exfoliated graphene), films are substantially thicker increasing the contribution of bulk effects, often resulting in stronger interaction between graphene and moisture due simply to a larger effective surface area. In general the interaction with moisture results in charge transfer from/to the graphene causing a change in conductivity for resistive devices or a change in dielectric constant for capacitive devices. Such charge transfer may arise through protonation of water or through substrate impurity screening.

The dominant surface effects associated with thin samples make them very sensitive to the substrate. CVD graphene shows significant p-type doping when transferred to SiO_2 due the presence of charge traps in the oxide[25]. Upon p-doping of the graphene channel the Fermi level moves deeper into the valence band and causes an increase in conductivity due the increased (hole) carrier density. Shim et al. report screening of graphene-substrate charge transfer for a thin layer of adsorbed water, where supression of substrate effects

reduce the p-doping of the graphene layer as characterised by Raman spectroscopy[26]. Smith et al. present a CVD graphene humidity sensor that shows increased conductivity upon exposure to moisture due to charge transfer, where the interaction occurs between defects in the SiO_2 substrate and polar water molecules[27]. Lastly, Shehzad et al. engineer a graphene/silicon heterostructure sensitive to humidity and atmospheric gas species that operates through modification of the Schottky junction upon adsorption of molecular species[28]. For mechanically exfoliated graphene, Schedin et al. showed detection of single molecules an FET structure, where the high sensitivity relies on careful tuning of the chemical potential to around the charge-neutrality point where the density of charge carriers is low ($\sim 10^{11}$)[29]. Further, the authors observe suppression of scattering for a thin layer of water on the graphene, suggesting the water acts to screen charged impurities in the SiO_2 and reduce p-doping.

Lastly, for wet-chemically derived graphene materials including GO, rGO and LPE-flakes, films tend to be substantially thicker with higher density of defects. Such films are typically less sensitive to substrate effects with larger variations in flake thickness and more dangling bond defects. The mechanism of charge transfer from water to graphene oxide occurs when protonation of water results in increased charge densities in the graphene oxide[30] which has been shown to increase conductivity of resistive sensors[31] or reduce the dielectric constant in capacitive sensors[32]. Santra et al. use a graphene-polymer composite ink (LPE graphene with polyvinyl pyrrolidone) to form a membrane that swells upon absorption of moisture, increasing the conductivity of the graphene flakes[33].

Most commerically available humidity sensors consist of two separated planar metal electrodes on top of which a thin layer of polymer is deposited. Finally a thin micro-porous metal film is deposited on top. Upon exposure to humidity, moisture is absorbed by the polymer resulting in a decreased dielectric constant and thus reduced capacitance. This speed of recovery know to be slow and is limited by the time taken for desorption of water from the polymer.

7.4.3 *Experimental*

CVD graphene grown on copper by cold-walled CVD again provided the backbone for the sensor. The graphene was selectively functionalised as outlined in figure 7.1(d) through exposure to oxygen radicals down-stream of the main plasma. Following oxygen plasma

treatment the graphene membrane was transferred using standard APS wet etching of the copper substrate to both SiO_2 and plastic (PEN) for further characterisation and device fabrication. A combination of X-ray photo-electron spectroscopy and Raman spectroscopy was used to characterise the degree of functionalisation. Both techniques were performed with the graphene still on the copper growth substrate. Also it is important to note that an untreated graphene sheet was used as a reference sample. Raman spectroscopy was performed using a Horiba system with 532 nm excitation wavelength with $\sim$1 μm spot diameter and 5 mW power. For humidity sensor measurements a sealed probe station was used to measure the two-terminal AC resistance of the device while inducing a change in relative humidity using warm water. To eliminate the possible temperature effects the chamber temperature is monitored throughout the measurements, noting a temperature variation of $<$1°C. Likewise the relative humidity of the chamber is measured using a calibrated commercial sensor (Honeywell HIH-4000) at a distance of $\sim$1 cm from the device. The AC resistivity of the device was measured while simultaneously monitoring the calibrated sensor output at 500 ms intervals. The total impedance of the device was found to be dominated by the resistive component ($\theta$$<$0.5) throughout the measurements. For reference, measurements are performed on both a pristine CVD graphene film transferred to PEN and a fully functionalised graphene film. Both devices showed some change in impedance with humidity, however the response fluctuated and was compared to the selectively functionalised device and non-reproducible.

7.4.4 *Results & Discussion*

XPS is used to probe the chemical modification of monolayer graphene layer upon exposure to mild oxygen plasma. Panel 7.3a shows the C1s spectra for pristine graphene on copper, where the distribution of bonding is dominated by the sp^2 hybridisation of carbon atoms forming the graphene lattice (peak at 284.4 eV) with smaller contribution from sp^3 bonds (peak at 285.4 eV) and several small shoulder peaks corresponding to epoxide (C-O-C), carbonyl (C=O) and carboxyl (O-C=O) bonds. The significant sp^3 and functional group fraction is likely due to the intrinsic defects in the as-grown graphene sheet serving as binding sites for oxygen functional groups upon exposure to ambient conditions[35;36]. Figure 7.3b shows the C1s spectra after 20 seconds exposure to mild oxygen plasma, showing a significant increase in oxygen content. A clear reduction in sp^2 fraction

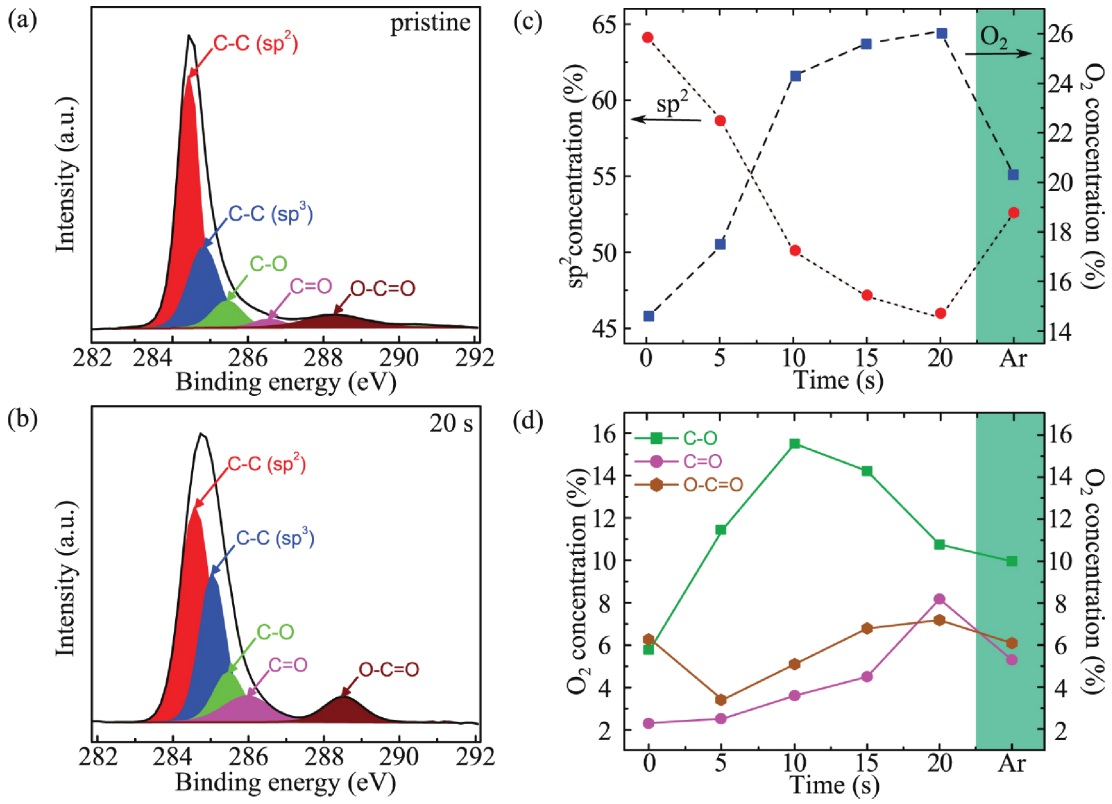

Figure 7.3: XPS C1s spectra for (a) pristine CVD graphene on copper and (b) after 20s exposure to oxygen plasma (c) relative sp^2 and oxygen concentrations measured for increasing exposure to oxygen-plasma and then after annealing in an argon atmosphere (d) relative contribution of several functional groups with increasing time and for thermal annealing in argon. Adapted from[34].

is observed as presented in 7.3(c), showing a reduction from 65% to 45% for 20s exposure. This is complimented by a substantial increase in oxygen content from 14% to 26% for the same exposure. Increased fraction of epoxide, carbonyl and carboxyl is observed for increasing time from 0-10 seconds, where the relative concentration of epoxide bonds decreases, due to the epoxide bond serving as an intermediary for increased carbonyl and carboxyl groups on graphene edge sites. To further understand the chemical composition of the films, a sample is annealed in argon at 220°C following exposure to O_2 plasma. The green panels in Figure 7.3(c) and (d) show the relative sp^2 concentration recovers somewhat upon annealing while the oxygen concentration is reduced. This can be interpreted as thermally activated removal of oxygen functional groups from the basal plane of graphene leading to partially recovered sp^2 fraction[37]. The oxygen content not returning to its original value can be attributed to insufficient annealing temperature/time or a additional disorder induced by the plasma.

To assess the uniformity of selective functionalisation Raman mapping spectroscopy is used. Figure 7.4(a) shows an electron-beam lithography design opened up in a PMMA mask on graphene/copper substrate where the brightly coloured region is the exposed graphene. When placed down-stream of the mild O_2 plasma the exposed regions are functionalised with oxygen groups and the masked areas remain pristine. Following plasma treatment the PMMA-graphene membrane is transferred to a rigid SiO_2/Si^{++} substrate as shown in Figure 7.4(b). After removing the PMMA the treated regions are indistinguishable from the pristine graphene with optical microscopy, however the functionalised regions are visible with SEM as shown in Figure 7.4(c) where they appear darker, due to reduced electrical conductivity, typical of functionalised graphene. The Raman spectra of CVD graphene on SiO_2 for masked and exposed graphene are shown in Figure 7.4(d). As previously stated, the position and relative intensity of the D, G and D'-bands can be used to learn about the degree of functionalisation in the sample. For masked areas a spectra typical of pristine monolayer CVD graphene is observed. with small D-band at $\sim$ 1350 cm^{-1}, a ratio of $I_D/I_G \sim 0.1$ and absence of the D'-band at $\sim$ 1620 cm^{-1}. Further, the ratio of $I_{2D}/I_G \sim 2$ is characteristic of monolayer graphene. Unmasked areas show a markedly different Raman spectra typical of functionalised graphene, with substantial D-band and the emergence of a D'-band at 1620cm^{-1}. For quantitative analysis of the crystal structure, the Tuinstra-Koenig relation is used to estimate crystallite size;

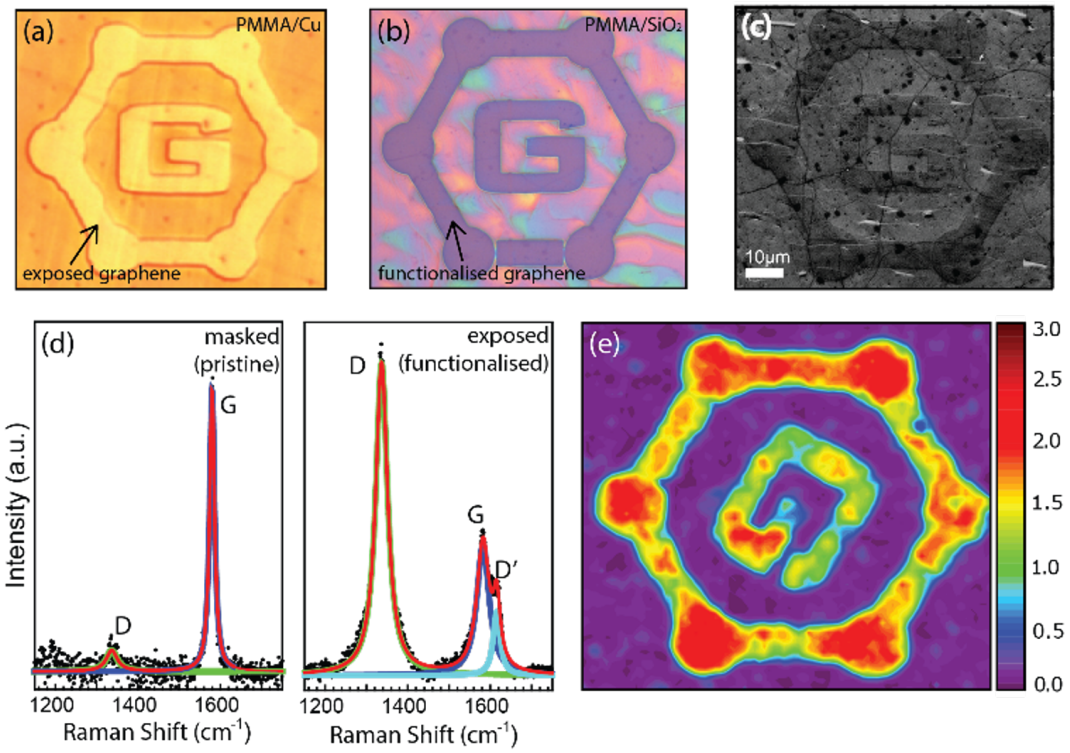

Figure 7.4: Selective on-copper functionalisation of CVD graphene. Panel (a) shows the area selected to be functionalised following lithography of PMMA mask. (b) Selectively functionalised graphene with PMMA mask after etching of the coppper growth substrate and transfer to SiO_2/Si^{++}. (c) SEM image of the sample in (b) after removing the PMMA mask. (d) representative Raman spectra for pristine (left) and functionalised (right) graphene and (e) mapping Raman spectrocopy for I(D)/I(G) of selectively functionalised graphene.

$$L_d^2(nm^2) = \frac{4.3 \times 10^3}{E_L^4(eV^4)}(I_D/I_G) \tag{7.2}$$

where L_d^2 is the inter-defect distance and E_L is the excitation wavelength, a decreasing distance between defects is observed for increasing treatment time from 17 nm to 8 nm for 10 seconds treatment which is consistent with attachment of oxygen functional groups. Upon annealing the inter-defect distance increases (crystallite size) to 10 nm, showing partial recovery of the sp^2 hybridised graphene lattice. Figure 7.4(e) shows Raman mapping spectroscopy of a the selectively functionalised area, where the relative intensity I_D/I_G is plotted as a function of position. For each position the Raman spectra is measured followed by Lorentz fitting to extract peak information. The treated areas show markedly higher relative intensity of I_D/I_G. For these areas there is some variation between points, which is likely due to some under-developed mask resulting in lower degree of functionalisation. The combination of XPS and Raman spectroscopy show that patterning and exposure to low power oxygen plasma results in successful selective functionalisation of graphene with oxygen functional groups, where the masked areas remain of pristine quality.

Lastly, a graphene-based humidity sensor is fabricated where CVD graphene forms the backbone and selective regions are functionalised to increase the interaction with moisture. The device consists of a 1 $\times$ 1 cm graphene channel with 100 $\times$ 100 μm functionalised areas and silver-paint contacts. The device is fabricated on copper and subsequently transferred to a flexible plastic (PEN) substrate. The impedance of the device is measured while modulating the relative humidity (RH%). Figure 7.5(a) shows the response of the device (red) with time while controlling the humidity (blue). Unlike devices based on wet-chemically derived graphene/GO, a near linear increase in the device conductance is observed for increasing humidity across nearly the entire measured range of 30 - 85 %RH that is repeatable over several cycles of increasing/decreasing humidity. For quantitative analysis of the performance the device conductance is plotted as a function of RH, shown in figure 7.5 and calculate the sensitivity of the device using;

$$S = \frac{R_x - R_{30}}{RH_x - RH_{30}} \tag{7.3}$$

where R_x and R_{30} are the device conductances at x % and 30 % relative humidity.

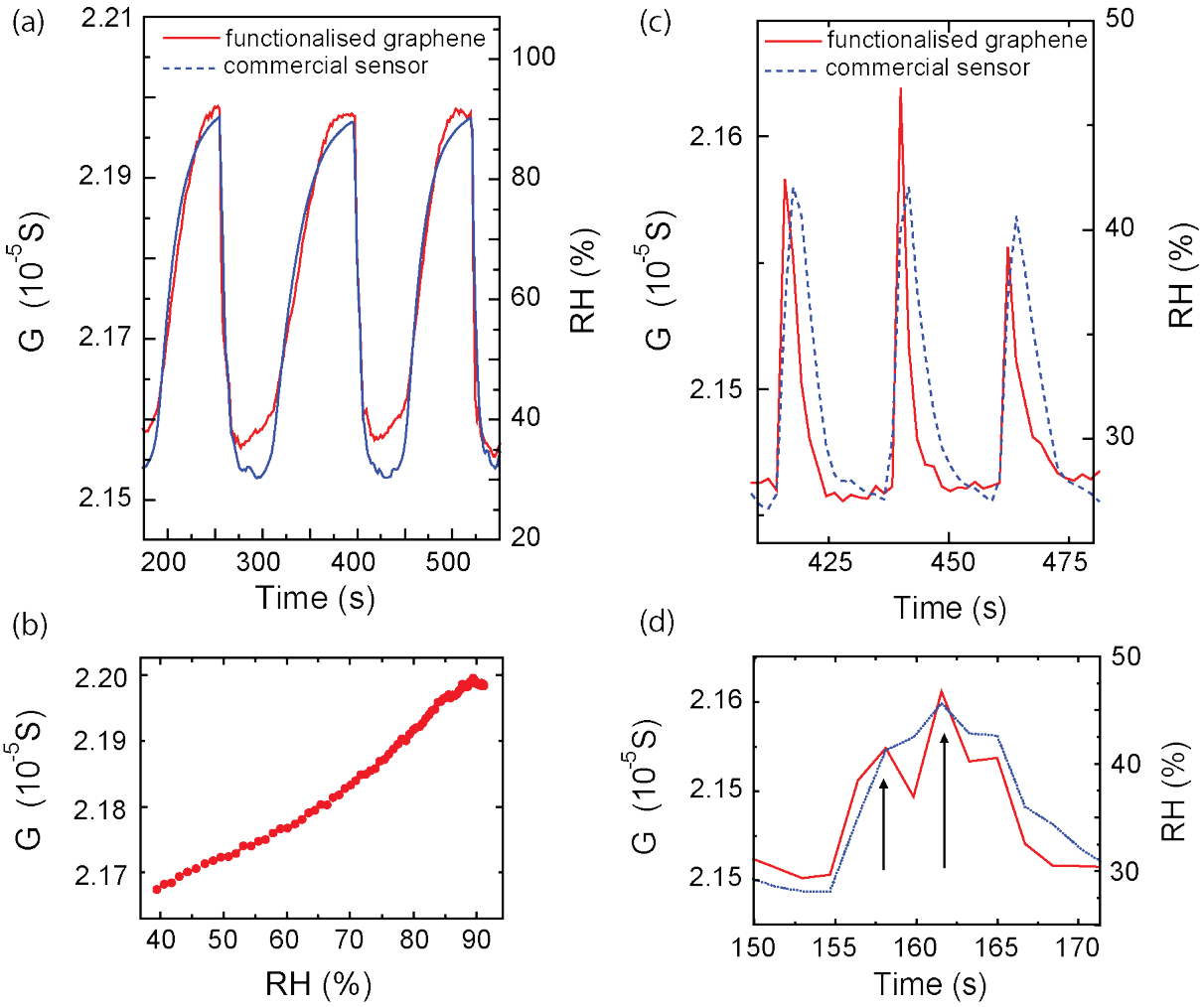

Figure 7.5: Characterisation of humidity sensor performance; (a) Conductance vs. time for humidity cycles, (b) Conductance plotted as function of RH for extraction of sensitivity, (c) conductance response to 3 subsequent breaths on the sample and (d) conductance of two fast breaths in quick succession.

For x = 90% a corresponding sensitivity of 17 Ω/RH(%) is extracted. While this absolute change in resistance is easily measurable, the proportional change in resistance given by;

$$\frac{R_{90} - R_{30}}{R_{30}} \times 100 \tag{7.4}$$

shows a 2.27% change in the total device resistance which is relatively low and one aspect that may be improved in future device geometries. With human-machine interactions in mind the response of the device to the human breath is investigated. Figure 7.5(c) shows the change in conductance and relative change in humidity induced when the sample is breathed on. Moisture in the breath raises the humidity by 10-15% (blue) as measured using the commercial sensor. The graphene sensor shows fast response to breath, with a time response faster than that of the commercial sensor. The rise and fall times of the graphene device both out-perform the commercial sensor which is illustrated in figure 7.5(d) where the sample exposed to two breaths in quick succession as indicated by the black arrows. The graphene device shows some recovery between breaths, while the commercial sensor fails to recover. This represents one clear advantage of the graphene humidity sensor and may be explained when considering the principle of operation of most commercial humidity sensors. Unlike commonly used commercial sensors, the graphene-based sensor shows highly linear response and fast response times. Regarding the mechanism for operation the sensor behaves somewhat similarly to the pristine CVD field-effect transistor sensor previously reported[27] although with a significantly higher device resistance, likely due to functionalisation process. Contrary, the response of our pristine graphene sensor was poor but may be explained by small amounts of disorder relative to the partially functionalised sample. Considering the sensor is based on a single graphene layer, the substrate is likely playing a role in the interaction with moisture, taking this into account the most likely mechanism of operation is a combination of attachment of water molecules to oxygen functional groups, dangling bonds created during functionalisation and dangling bonds present at grain boundaries in the graphene film, enhanced by the substrate. The effect of the functional groups likely plays a role, however further experiments may be needed to pin down the origin, which are outside the scope of this study.

7.5 CONCLUSIONS

In conclusion this chapter presents a novel method for processing graphene-based sensing elements on the copper growth substrate. I demonstrate successful lithography, metallisation, etching and functionalisation and use the technique to fabricate a transparent, flexible touch sensing array and transparent humidity sensor with fast response to human breath. The touch sensor shows fast response to human touch, as well as a measurable reponse to insulating loads. The humidity sensor shows highly linear response across the measured range with sensitivity of 17 Ω/RH(%) and fast response to human breath. The use of graphene as a backbone for multi-functional sensing elements is demonstrated, with an emphasis on the human-machine interactions of future technologies. Future studies may include engineering multiple sensors on the same graphene sheet for combination sensor. Futhermore, through selective functionalisation of CVD grphene, the water-graphene interaction may be studied further by tuning the functional group/defect density (cm^{-2}).

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8

CONCLUSIONS AND OUTLOOK

In this thesis I investigate the growth and oxidation of graphene and later HfS_2 for use as electrode and insulating materials for resistive memory devices, FETs and sensors. Beginning with CVD growth of the material using atmospheric pressure CVD the growth of large hexagonal graphene domains is investigated and the optical and electrical properties characterised for use as an electrode in the subsequent chapters. It is found that growth temperature affects nucleation density, growth-rate and layer number. Raman spectroscopy reveals high quality of the domains after transfer to SiO_2 and hBN substrates and FETs are fabricated to measure the electrical properties. On atomically flat hBN substrates mobilities of upto 10,000 $cm^2\ V^{-1}\ s^{-1}$ are measured at room temperature with negligible residual doping suggesting clean transfer. Bilayer formation is observed for non-isothermal growths and the as-grown domains show a variety of stacking orientations both well aligned AB stacking as well as twisted by upto 30 degrees. While an excellent electrode material, pristine graphene is unsuitable for use in resistive memory (ReRAM) devices and as a channel material in FETs owing to the low ON/OFF ratio. Chemical functionalisation is one solution to this problem and allows for band-gap opening. Oxidation by Hummers method yields graphene oxide - an industrially suitable, highly resistive switching material. Optimised ReRAM devices based on a hybrid titanium-GO are developed to investigate the ultimate performance showing high speed, endurance,

and retention time as well as high flexibility and multibit operation, where switching is ascribed to redox reactions within interface layer between titanium and oxide. Following this, a few-layer graphene electrode is incorporated into a GO ReRAM device showing bipolar reversible switching. These experiments improve improve the understanding of the ultimate performance of GO-based ReRAM when combined with a reactive metal and provide a key step towards all-graphene memory devices. Next, continuing with the exploring oxidation of 2D materials. The laser-assisted oxidation of hafnium disulphide, discovered in our group, is utilized to write insulating oxides in stacks of 2D materials. An inherently unstable material in ambient conditions the oxidised material is employed as a gate dielectric and resistive switching material, finding that it exhibits properties akin to that of hafnium dioxide - a high-κ dielectric with high potential for a range of devices, including atomically thin resistive memory devices. Finally, with a thought to industrial production of graphene devices, a novel technique for the patterning of flexible CVD graphene devices directly on copper foils is developed and demonstrated by a flexible and transparent touch sensor array and a transparent plasma oxidised graphene humidity sensor on flexible plastic substrate. Both the touch sensor and humidity sensor show fast response times, and it is suggested that such processing techniques may be applied to graphene grown on a number of substrates. In summary the growth and oxidation of graphene and 2D materials is explored and found to enable multiple additional functionalities in devices for flexible electronic applications.

A

APPENDIX A - DEVICE FABRICATION

A.1 DEVICE FABRICATION

Throughout this thesis several device geometries are fabricated for electrical characterisation including FETs, resistive switching stacks and Van der Waals heterostructures. This appendix briefly outlines the standard fabrication procedure.

Unlike conventional thin copper foils, CVD graphene grown on melted/re-solidified copper is not compatible with etching transfer due to the large amount of metal (∼500 um total thickness). As such, it is transferred from copper substrates to SiO_2 or hBN using a home-built electrochemical delamination setup. For the transfer a thin (150 nm) PMMA support layer is spin-coated onto the graphene/copper and subsequently cured in vacuum. Next a 0.5 M NaOH electrolyte solution is prepared and added to a small 100 ml Borosilicate beaker. For the delamination the graphene-copper substrate plays the role of the cathode (V-) and a 25 μm Pt foil the anode (V+). A DC current source is used to pass a current (∼ 500 mA across 2-3 cm) between the graphene-copper and Pt foil causing in hydrogen evolution at the copper graphene interface resulting in peeling off of the graphene as the copper is gently lowered into the electrolyte. Such a transfer procedure roughly follows that of Wang *et. al.*[1]. After rinsing in de-ionised water the graphene is transferred to the substrate of choice, dried in ambient conditions. Once

dry the samples are baked at 140 °C for increase the adhesion between graphene and the substrate. Lastly, the PMMA support layer is removed using standard acetone/IPA cleaning.

Heterostructures are fabricated using a home-built stacking setup, similar to that described by Castellanos-Gomez *et. al*[2]. First, marked SiO_2 substrates are cleaned in acetone/IPA and then treated with oxygen plasma followed immediately with exfoliation of Flaggy graphite using scotch tape. Treatment with oxygen plasma increases the number of silanol surface groups[3] which gives better density of graphene flakes. Care is taken not to over expose the substrate to plasma as this results in highly doped graphene samples. After identification of the target graphene flake, the sample is aligned in the stacking microscope. Next bulk hafnium disulphide crystals (HQ Graphene) are exfoliated using commercially available PDMS films (TelTec X4). Upon choosing the desired HfS_2 flake the PDMS film is loaded into the stacking setup, aligned to the bottom graphene and then gently lowered into place on top of the graphene. Deposition of the top graphene/graphite electrode is achieved using a similar approach and electrode patterning/deposition follows the standard route outlined below.

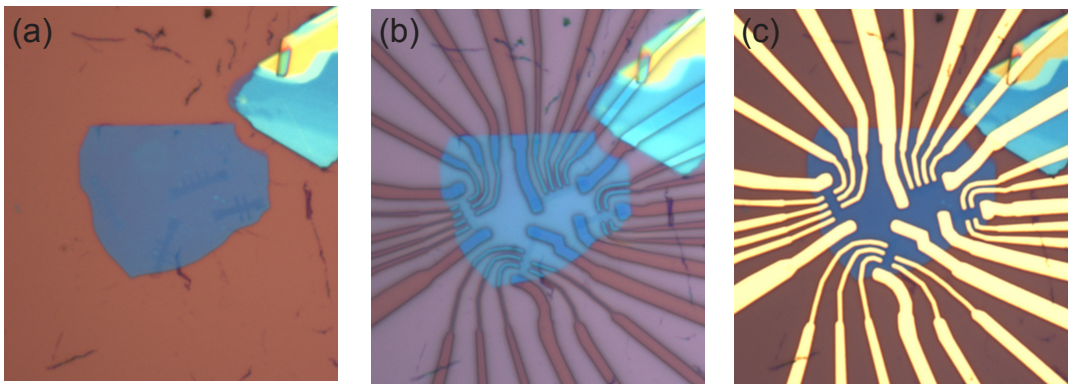

Figure A.1: CVD graphene FET device process flow beginning with (a) definition of etch etch mask followed by reactive-ion etching (b) removal of etch mask and patterning of contact leads and pads and (c) metallisation and lift-off

Electron beam lithography is performed on a Nanobeam NB4 machine. For features larger than 1 μm a conventional positive resistive (Microchem PMMA A4 950K) is spin coated onto the substrate with 200-300 nm thickness and baked on the hot-plate for 5 minutes at 150 °C. For insulating substrates (e.g. glass & PET) a thin conducting

layer (5 nm of Al) is thermally evaporated on the surface of the PMMA resist before lithography. Several steps of device fabrication are shown in Figure A.1. Exposure is performed using an 80 kV acceleration voltage, beam current of 10-40 nA and dose of 10-20 μC cm^{-2}. The sample is developed using two-part developer comprised of IPA and MIBK (3:1) for 30 seconds and then rinsed in IPA and dried with nitrogen. Gold electrode deposition is performed using thermal or electron-beam evaporation, using either titanium or chrome as a sticking layer. After metallisation the undeveloped resist can be removed with warm acetone/IPA. Finally devices are wire-bonded into a 5 $\times$ 5 mm lead-less chip carrier (LCC) before being mounted into the measurement probe. For preparation of high mobility graphene FETs based on CVD graphene an annealing step is also performed to remove processing residues. Following fabrication the sample is loaded into a 2-inch quartz tube furnace through which a reducing gas (10% H_2 in Ar) is flowed. The temperature is gradually ramped to 350 °C and held there for several hours before cooling to room temperature.

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PUBLICATIONS

The ideas and data presented in this thesis are subject of the following publications:

1. Peimyoo, N.P **Barnes, M. D.**, De Sanctis, A.D. Russo, S. Craciun, M.F. Withers, F. - Multipurpose dielectrics for VdW heterostructures and resistive switching devices based on oxidised HfS_2 **in preparation** (2018). **Contribution:** device fabrication, transport measurements, data analysis, AFM, writing of manuscript

2. Craciun, M. F. Kraphach, I. **Barnes M. D.** Russo, S Properties and applications of chemically functionalized graphene, **Journal of Physics: Condensed Matter**, (2013). **Contribution:** Review paper text

3. Bointon, T. H. **Barnes, M. D.** Russo, S. Craciun, M. F. High quality monolayer graphene synthesized by resistive heating cold wall chemical vapour deposition, **Advanced Materials** (2015) **Contribution:** Sensor design & fabrication, Raman spectroscopy, AFM, electrical characterisation

4. Nagareddy, V. K. **Barnes, M. D.** Zipoli, F. Khue-Tian, L. Alexeev, A. Craciun, M. F. Wright, C. D. Multilevel ultra-small ultra-fast flexible non-volatile graphene oxide memories, **ACS Nano** (2016) **Contribution:** Sample fabrication, data analysis

5. Alexeev, A. M. **Barnes, M. D.** Nagareddy, V. K. Craciun M. F. Wright, C. D. A simple process for the fabrication of large-area CVD graphene based devices via

selective in-situ functionalization and patterning, **2D materials** (2016) **Contribution:** Sample fabrication, Raman spectroscopy, electrical characterisation, data analysis

6. De Sanctis, A. **Barnes M. D.** Amit, I. Craciun, M. F. Russo, S. Functionalised hexagonal-domain graphene for position-sensitive photodetectors, **Nanotechnology** (2016) **Contribution:** CVD graphene growth & transfer

7. Dimov, D. Amit, I. **Barnes M. D.** Russo, S. Craciun, M. F. Graphene reinforced concrete, **submitted** (2017). **Contribution:** Raman spectroscopy

8. Mehew, J. **Barnes M. D.**, Craciun, M. F. Russo S. Role of defect states in functionalized graphene photodetectors, **Society of Photo-optical Instrumentation Engineers** (2017) **Contribution:** CVD growth & transfer