Modeling a three-terminal, phase-change based logic device

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ABSTRACT

The write, read and erase cycles of a vertical three-terminal, phase-change (3-T PCM) based logic device were investigated using multiphysics finite-element modeling and simulation. A model of a practical device structure is proposed, and includes the interaction of the electrical, thermal and phase-change dynamics during switching in the device. Parametric simulations were carried out to determine the operating currents and pulse widths, and to determine the resistance threshold levels for logic operation. The operation a number of logic gates is demonstrated.

Key words: *phase-change memory, digital logic, three-terminal, vertical structure*.

1. INTRODUCTION

Conventional methods of implementing logic gate functionality using phase-change material involve the application of logic inputs in sequence [1-3]. Three-terminal phase-change based memory cells provide the opportunity of applying two logic inputs simultaneously between any pair of the three terminals to implement different logic functions, in the same manner as semiconductor logic gates [4, 5]. These articles focus on the design of a practical 3-T PCM vertical logic device structure through multi-physics modeling and simulation.

2. Methodology

A proposed vertical device structure (shown in Fig. 1) was constructed in Comsol Multiphysics, with two terminals connected to two current sources to provide the logic inputs, and the third terminal grounded. The initial state of the phase-change material is the crystalline phase, and application of writing currents leads to melting following by rapid quenching to the amorphous phase in the region adjacent to the grounded (side) terminal. Controlling the size of the amorphous region controls the resistance across the phase-change layer, measured during readout between the grounded terminal and another terminal. Electrical modeling involves solution of Laplace's equation for the potential and electric fields, which provides the heat source for the solution of the heat diffusion equation. A simple rate-equation type model is used to model crystallisation. The coupling between the electrical, thermal and phase-change models is illustrated in Fig. 1.

3. Results

Parametric simulations were carried out to determine the appropriate current source levels and pulse widths. Fig. 2 (a) shows the calculated temperature profile and corresponding amorphous region (inset) during writing by application of current pulses simultaneously. The corresponding resistance change as a function of write currents is shown in Fig. 2(b). The NAND logic gate implementation using simultaneous current sources is shown in Fig. 2(c).

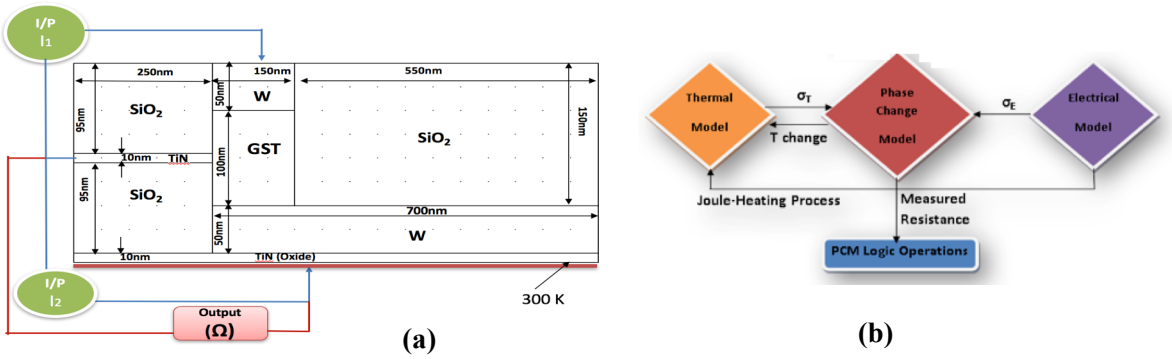

Figure 1: single 3-T PCM: (a) Vertical Structure, and (b) block diagram of physical model.

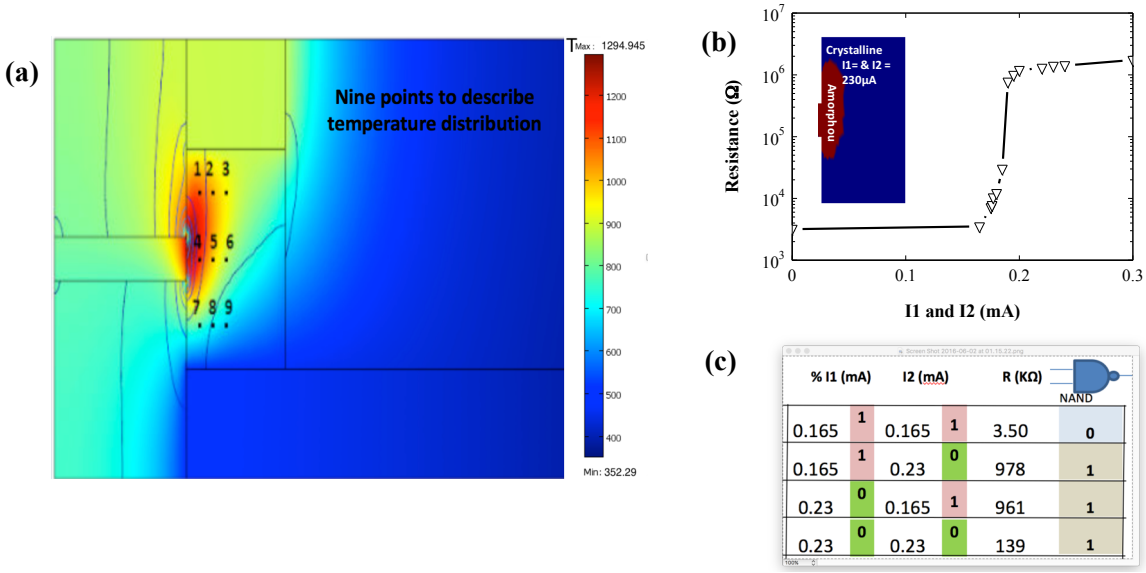

Fig. 2 (a) Temperature distribution in vertical cell structure, and (b) calculated resistance change as function of write currents. Inset in (b) shows amorphous region near the side (grounded) terminal after writing. (c) NAND gate implementation.

Conclusions

The write, read and erase cycles of a three-terminal, phase-change based logic device were investigated using multiphysics finite-element modeling and simulation. A model of a practical vertical device structure is proposed, and includes the interaction of the electrical, thermal and phase-change dynamics during switching in the device. Parametric simulations were carried out to determine the resistance threshold levels for logic operation according to the operating input currents and pulse widths through changing the amorphous-crystalline portions of the active region in the PCM layer. The operation of some logic gates is demonstrated through the simulations.

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