Exploitation of MOSFET Based AC Switches in Capacitive Impedance Matching Networks in Inductive Wireless Power Transfer Systems

C.A. Alexandru [1], D. Zhu [1*],

[1] College of Engineering, Mathematics and Physical Sciences, University of Exeter, Exeter, EX4 4QF, UK
[*]d.zhu@exeter.ac.uk

This paper investigates the exploitation of MOSFET based AC switches in capacitive impedance matching networks (IMN) for inductive wireless power transfer (WPT). The IMN optimum capacitance has been chosen for a 200 kHz resonant frequency. The activation of tuning capacitor on the tuning branch is achieved with the use of MOSFET AC switches in order for the WPT system to achieve maximum power transfer efficiency. The MOSFET AC switch is modelled as an internal parasitic resistor and capacitor connected in parallel. A WPT analytical model is developed to study the effects of the MOSFET's parasitic elements on the WPT system's efficiency and is verified experimentally. Various MOSFET switches and relays have been implemented as the IMN switching elements and compared when tested under the same conditions. It is concluded that MOSFET AC switches which have low on-resistances and small parasitic capacitances are desirable as they have a smaller impact on the efficiency. Additionally, parasitic capacitances of MOSFET AC switches need careful consideration for different resonant frequencies as they can affect the overall IMN tuning capacitance especially when they are turned off. Comparing to commonly used relay switches, MOSFET based AC switches have similar switching performance but are significantly smaller in size.

1. Introduction

Inductive wireless power transfer (WPT) systems for low power applications has been evolving in the last decade and is now implemented in more and more commercial mobile devices [1]. A typical WPT system consists of a transmitter coil and a receiver coil that are coupled inductively as shown in Fig 1(a). In applications where the system's effectiveness is a key element, improving the power transfer efficiency is one of the aspects investigated. This can be of great importance for applications such as commercial gadgets (i.e: wireless mobile phone charging). In inductive WPT, lower power transfer efficiency can be caused by multiple factors. One of them is the variation in load impedance due to misalignment between the transmitter and receiver coils thus change of coupling factors [2].

Such low efficiency can be compensated by implementing impedance matching networks (IMN) in the WPT system [2]-[6]. Research studies in [7] concluded that implementing additional circuits consisting of inductive and capacitive components is a valid possibility to compensate for impedance mismatch which leads to low efficiency. It is also highlighted that the negative effects of using an impedance matching network consists of the difficulty in creating a smooth signal due to the use of discrete block switching [7]. Therefore, to avoid jeopardizing the WPT performance, fixed IMN are usually used [4].

Generally, the IMN architecture consists of capacitive components connected in various configurations such as series-parallel (SP) and parallel-series (PS) [2]-[8] illustrated in Fig.1.(b)-(c).

The main advantage of implementing IMN is matching the system to the optimum impedance with the purpose of maximising the overall power transfer efficiency. This is achieved through the implementation of switches in the IMN's capacitive tuning branches, which enables the network to be adaptive and adjust its impedance accordingly. This is regarded as a viable solution to tackling transmitter and receiver coils misalignment and handling simultaneous charging of multiple devices.

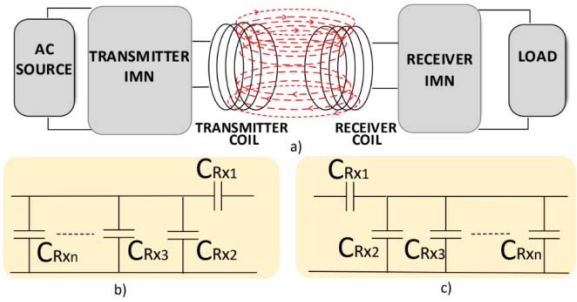

Fig. 1. General inductive WPT circuit model (a) and IMN with a PS (b) or SP (c) configuration

Existing literature involving the development of impedance matching networks, have implemented mainly mechanical switches or relays as the switching element. For example, studies undertaken in [5]-[6] and [9]-[10] have focused on developing a capacitive matrix, having relays to perform the switching.

Additionally, in [2], an array of parallel capacitors was developed. Each parallel branch of the IMN integrated the capacitors in the system through a switch, with the purpose of achieving maximum power efficiency irrespective of the number of load devices. The IMN used a slide-style dual in-line package switch which was operated manually.

In multiple designs, such as the ones presented in [10] and [11], an automated algorithm has been developed to pair the most suitable capacitor to the system through the use of an electromechanical relay (EMR) switch (Panasonic ARE10A06). In the case of such complex designs [10], the implementation of multiple relays can present a disadvantage in terms of the overall IMN size which is considerably

increased if compared to non-switchable IMN due to the size of the relay switches. Solid state relays (SSR) and electromechanical relays provide the same switching capabilities through complete electrical isolation mechanically between their input and output contacts. SSR offers a quicker response of a few milli-seconds compared to EMR which typically has between 5 to 50 milli-seconds [12]. However, EMR is less expensive than SSR and has a low conduct loss due to its excitation and mechanical movement [12]. SSR are mainly used in applications such as converters [13], distribution transformers [14] and power systems [15]. An alternative to the relay switch is the use of MOSFET transistors as the switching element. Compared to the relay switches, the MOSFET offers the advantage of reducing the overall IMN size due to their small dimensions and is therefore, a potential choice as an AC switch in adaptive impedance networks and WPT systems.

Using MOSFET as DC switches is a common practice in electronic systems. However, the MOSFET based AC switches have not been thoroughly investigated, especially as a viable option for the IMN in WPT systems. Additionally, the importance of the switch configuration and its effect on the IMN performance caused by internal parasitic properties has not been discussed.

In this paper, a PS configuration IMN consisting of MOSFET AC switches is implemented at the receiver of a WPT system with an operating frequency of 200 kHz. The focus of this paper is on the suitability of MOSFET switches for the IMN and not on optimising the IMN network itself.

The WPT performance using MOSFET switches will be compared to that using the electromechanical relay switches which is referred to as relay switches for the remaining of this paper. Section 1 covers the development of the circuit model as well as an analysis of the MOSFET switch, determining the impact of each parasitic element. Section 2 illustrates the comparison between the theoretical and experimental results for four pairs of MOSFET switches and a mechanical relay. The results are compared and discussed in Section 3.

2. WPT MATHEMATICAL MODEL CONFIGURATION WITH IMN

2.1 PS- IMN CIRCUIT MODEL

A typical inductive wireless power transfer system consists of a power source transmitting electromagnetic energy wirelessly from a transmitter coil to a receiver coil [1]-[2] as presented in Fig. 1(a).

The equivalent circuit model of a WPT system studied in this research includes a switchable PS capacitive IMN on the receiver side as shown in Fig. 2. The transmitter, T_x , constitutes of an AC voltage source, V_s and a corresponding input impedance, Z_s. C_{Tx} is the matching capacitor at the transmitter. The transmitter coil is characterized by L_{Tx} and R_{Tx} which denote its self-inductance and self-resistance respectively. Similarly, L_{Rx} and R_{Rx} correspond to self-inductance and self-resistance of the receiver coil respectively and R_L represents the load resistance. The two coils inductively coupled with the mutual inductance, M_{LTx-Rx} determined by a coupling factor, k.

The receiver IMN design was established by taking into considering the research in [8] which focused on comparing the performance of SP and PS-IMN. It has been established that using a PS-IMN at the receiver is more effective than an SP-IMN in order to reduce cross-coupling. Therefore, the capacitive IMN has been developed using the PS model with three tuning capacitors, C_{Rx1}, C_{Rx2} and C_{Rx3} in which C_{Rx2} constitutes the switchable parallel branch.

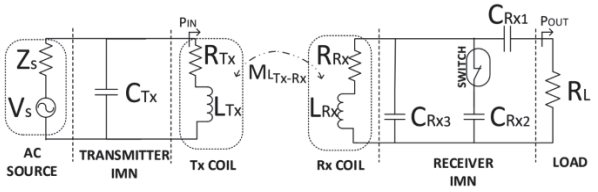

Fig. 2. WPT system equivalent circuit with the transmitter, T_x and a PS capacitive IMN at the receiver, R_x

2.2 SWITCH MODEL

When using MOSFETs as AC switches, two n-type MOSFETs are required and connected as shown in Fig. 3(a). Both source terminals are connected to the ground while both gate terminals are connected to a DC control voltage. The switch is turned on by applying a DC voltage greater than the threshold voltage of the MOSFET, V_{TH}, across the gate and the source. The switch is turned off when the applied voltage is lower than V_{TH}. The two drain terminals are the two terminals of the AC switch.

The MOSFET switch is modelled by its equivalent impedance, Z_{switch}, which consists of a parasitic resistor, R_p, and a parasitic capacitor, C_p, connected in parallel as shown in Fig. 3(b). When the switch is turned on, R_p is the total drain-to-source on-resistance of the two serially connected MOSFETs. When the switch is turned off, R_p is open-circuit.

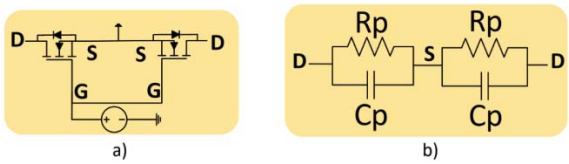

Fig. 3. MOSFET AC switch circuit connections (a) and simplified equivalent model (b)

2.3 MATHEMATICAL MODEL

The overall equivalent circuit of a WPT system with IMN in PS configuration is shown in Fig. 4. The MOSFET switch connects the C_{Rx2} capacitor in the tuning branch.

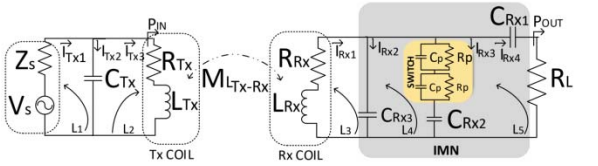

Fig. 4. WPT system mathematical equivalent circuit–with the transmitter, T_x and a PS capacitive IMN at the receiver, R_x with MOSFET switch on

The mathematical model was developed using Kirchhoff's voltage and current laws based on the five loops highlighted in Fig. 4 and were analysed using the Equivalent circuit method (ECM) [5],[11] and [16]-[17].

$L1: I_{Tx1}Z_s + I_{Tx2}Z_{CTx} = V_s$ (1)

$L2: I_{Tx2}Z_{CTx} - I_{Tx3}(Z_{RTx} + Z_{LTx}) + I_{Rx1}Z_{MLTx-Rx} = 0$ (2)

$L3: I_{Rx2}Z_{CRx3} + I_{Rx1}(Z_{RRx} + Z_{LRx}) - I_{Tx3}Z_{MLTx-Rx} = 0$ (3)

$L4: I_{Rx3}(Z_{CRx2} + Z_{switch}) - I_{Rx2}Z_{CRx3} = 0$ (4)

$L5: I_{Rx4}(Z_{CRx1} + Z_{RL}) - I_{Rx3}(Z_{CRx2} + Z_{switch}) = 0$ (5)

where $Z_C = \frac{1}{j\omega C}$, $Z_R = R$, $Z_L = j\omega L$ and $Z_{switch} = \frac{Z_{Rp} * Z_{Cp}}{Z_{Rp} + Z_{Cp}}$.

In order to derive the efficiency formula, all circuit currents will be expressed in terms of the load current, I_{Rx4}. Rearranging Eq.(5) and expressing I_{Rx3} in terms of I_{Rx4} lead to:

$$I_{Rx3} = I_{Rx4}\frac{Z_{CRx1} + Z_{RL}}{Z_{CRx2} + Z_{switch}} \quad (6)$$

Substituting Eqs. (6) and (4) and writing the expression in terms of I_{Rx4} leads to:

$$I_{Rx2} = I_{Rx4}\frac{Z_{CRx1} + Z_{RL}}{Z_{CRx3}} \quad (7)$$

Substituting Eqs. (6) and (7) in Eq. (3) and expressing I_{Tx3} in terms of I_{Rx4} leads to Eq. (12) via steps detailed in Eqs. (8) to (11):

$$I_{Rx4}\frac{Z_{CRx1} + Z_{RL}}{Z_{CRx3}}Z_{CRx3} + (I_{Rx2} + I_{Rx3} + I_{Rx4})(Z_{RRx} + Z_{LRx}) - I_{Tx3}Z_{MLTx-Rx} = 0 \quad (8)$$

$$I_{Rx4}(Z_{CRx1} + Z_{RL}) + I_{Rx4}\left(1 + \frac{Z_{CRx1} + Z_{RL}}{Z_{CRx2} + Z_{switch}} + \frac{Z_{CRx1} + Z_{RL}}{Z_{CRx3}}\right)(Z_{RRx} + Z_{LRx}) - I_{Tx3}Z_{MLTx-Rx} = 0 \quad (9)$$

$$I_{Rx4}\left[Z_{CRx1} + Z_{RL} + \left(1 + \frac{Z_{CRx1} + Z_{RL}}{Z_{CRx2} + Z_{switch}} + \frac{Z_{CRx1} + Z_{RL}}{Z_{CRx3}}\right)(Z_{RRx} + Z_{LRx})\right] - I_{Tx3}Z_{MLTx-Rx} = 0 \quad (10)$$

Labelling $\Gamma = \left(1 + \frac{Z_{CRx1} + Z_{RL}}{Z_{CRx2} + Z_{switch}} + \frac{Z_{CRx1} + Z_{RL}}{Z_{CRx3}}\right)$

$$\Upsilon = Z_{CRx1} + Z_{RL} + \Gamma(Z_{RRx} + Z_{LRx})$$

Eq. (10) can be rearranged as:

$$I_{Rx4}\Upsilon - I_{Tx3}Z_{MLTx-Rx} = 0 \quad (11)$$

$$I_{Tx3} = I_{Rx4}\frac{\Upsilon}{Z_{MLTx-Rx}} \quad (12)$$

Substituting Eq. (12) in Eq. (2) and expressing I_{Tx2} in terms of I_{Rx4} leads to:

$$I_{Tx2}Z_{CTx} - I_{Rx4}\left[\frac{\Upsilon(Z_{RTx} + Z_{LTx})}{Z_{MLTx-Rx}} + \Gamma Z_{MLTx-Rx}\right] = 0 \quad (13)$$

Labelling $\Upsilon = \frac{\Upsilon}{Z_{MLTx-Rx}}(Z_{RTx} + Z_{LTx}) + \Gamma Z_{MLTx-Rx}$ and Eq. (13) can be rearranged as:

$$I_{Tx2} = I_{Rx4}\frac{\Upsilon}{Z_{CTx}} \quad (14)$$

Substituting Eq. (14) in Eq. (1) and expressing V_s in terms of I_{Rx4} leads to:

$$\left(I_{Rx4}\frac{\Upsilon}{Z_{MLTx-Rx}} + I_{Rx4}\frac{\Upsilon}{Z_{CTx}}\right)Z_s + I_{Rx4}\frac{\Upsilon}{Z_{CTx}}Z_{CTx} = V_s \quad (15)$$

$$I_{Rx4}\left[\Upsilon + Z_s\left(\frac{\Upsilon}{Z_{MLTx-Rx}} + \frac{\Upsilon}{Z_{CTx}}\right)\right] = V_s \quad (16)$$

Labelling $\Psi = \frac{\Upsilon}{Z_{MLTx-Rx}} + \frac{\Upsilon}{Z_{CTx}}$ and Eq. (16) can be rearranged as:

$$I_{Rx4} = \frac{V_s}{\Upsilon + \Psi Z_s} \quad (17)$$

According to KCL, $I_{Tx1} = I_{Tx2} + I_{Tx3}$ and substituting Eqs. (12) and (14) leads to:

$$I_{Tx1} = I_{Rx4}\left(\frac{\Upsilon}{Z_{MLTx-Rx}} + \frac{\Upsilon}{Z_{CTx}}\right) = \Psi I_{Rx4} \quad (18)$$

The power transfer efficiency, η, can be calculated as the ratio between the input and output power as:

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{{I_{Rx4}}^2 Z_{RL}}{V_S I_{Tx1}} \quad (19)$$

The final form of the efficiency formula is expressed in terms of the discrete components impedance as:

$$\eta = \frac{R_L}{\Upsilon\Psi - Z_{Rs}\Psi^2} \quad (20)$$

Scenario 1: Mathematical model – Switch on

Using the mathematical model, the efficiency response was analysed for various on-resistances, R_p and parasitic capacitances, C_p. The simulation parameters are listed in Table I.

TABLE I
WPT SYSTEM EXPERIMENTAL AND SIMULATED PARAMETERS

Symbol	Quantity	Value
Z_s	Input impedance	0.5 Ω
R_{Tx}	Transmitter coil resistance	0.3 Ω
R_{Rx}	Receiver coil resistance	0.3 Ω
L_{Tx}	Transmitter coil inductance	30 µH
L_{Rx}	Receiver coil inductance	30 µH
σ	Coils wire cross-section	0.06 mm
r_o	Coils outer-radius	3.9 cm
r_i	Coils inner-radius	3 cm
d_{air}	Transmitter-Receiver air-gap	5 mm
M_{LTx-Rx}	Mutual inductance	14.4 µH
C_{Tx}	Transmitter tuning capacitor	33 nF
C_{Rx1}	Receiver series tuning capacitor	12 nF
C_{Rx2}	Receiver switchable parallel tuning capacitor	10 nF
C_{Rx3}	Receiver parallel tuning capacitor	4.7 nF

When the MOSFET AC switch is turned on, a smaller on-resistance, R_p, shorts C_p therefore it does not affect the equivalent impedance of the IMN and thus the efficiency. However, a larger on-resistance cannot short-circuit C_p. As a result, C_p affects the overall impedance of IMN and thus reduces the efficiency.

Fig. 5 shows the parasitic capacitance, C_p effect on the efficiency for multiple cases of R_p. All results are normalised

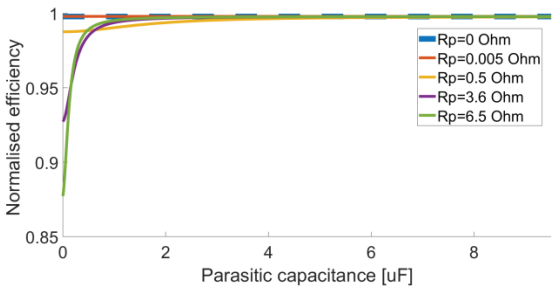

Fig. 5. Theoretical results – Normalised efficiency vs parasitic capacitance – model with switch on for multiple Rp values

to the maximum efficiency at the optimum load resistance when no switch is used.

It was found that when C_p is small, the efficiency reduces as R_p increases. As C_p increases, R_p has less impact on the efficiency.

The total impedance equation was derived based on the circuit model in Fig. 6 and is presented in Eq. (21), where Z_{switch} has been defined previously in Section 2.C. The optimum IMN impedance which leads to the maximum efficiency is 17.3 Ω.

$$Z_{IMN\ sw\ on} = \frac{Z_{CRx2\ on} * Z_{CRx3} * Z_{CRx1}}{Z_{CRx2\ on} * Z_{CRx3} + Z_{CRx2\ on} * Z_{CRx1} + Z_{CRx1} * Z_{CRx3}} \quad (21)$$

where $Z_{CRx2\ on} = 2 * Z_{switch} + Z_{CRx2}$.

Fig. 6 shows the change in the total impedance of IMN with respect to the parasitic capacitance for various R_p. It can be observed from Fig. 6 that in the cases when R_p is relatively large (0.5Ω, 3.6Ω and 6.5Ω), the total IMN impedance changes due to fact that the parasitic capacitance is connected to the tuning capacitor C_{Rx2} in series. Such change is greater when the parasitic capacitance is lower and causes the efficiency to decrease as shown in Fig. 5. When the MOSFET's parasitic capacitance is increased, its effect on the IMN total impedance becomes less significant and consequently, the WPT system efficiency increases, approaching the maximum efficiency.

Therefore, in order for the efficiency to stay maximum it is desirable to have an on-resistance, R_p as small as possible so that the total network impedance is not affected by the parasitic capacitor.

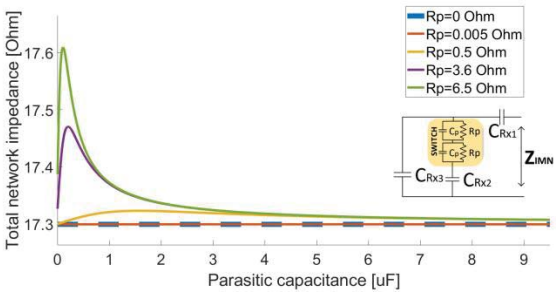

Fig. 6. Theoretical results – Total IMN impedance vs parasitic capacitance – model with switch on for multiple Rp values

Scenario 2: Mathematical model – Switch off

In contrast, when the MOSFET AC switch is turned off, the off-resistance is large and can be treated as open circuit. The equivalent circuit of IMN is as shown in Fig. 8.

The equivalent IMN impedance when the MOSFET is turned off can be derived using the same approach as mentioned previosly.

$$Z_{IMN\ sw\ off} = \frac{Z_{CRx2\ off} * Z_{CRx3} * Z_{CRx1}}{Z_{CRx2\ off} * Z_{CRx3} + Z_{CRx2\ off} * Z_{CRx1} + Z_{CRx1} * Z_{CRx3}} \quad (22)$$

where $Z_{CRx2\ off} = 2 * Z_{Cp} + Z_{CRx2}$.

Fig. 7 shows the normalised efficiency with variance of parasitic capacitance when the switch is off. It was observed that when parasitic capacitance is low, the overall efficiency

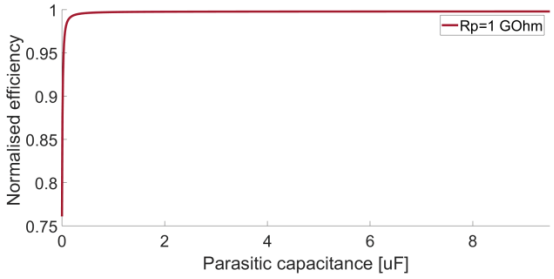

Fig. 7. Theoretical results – Normalised efficiency vs parasitic capacitance – model with switch off

is reduced. As the parasitic capacitance increases, so does the WPT system's efficiency.

Fig. 8 shows the change in the network's impedance as a function of C_p. As the parasitic capacitance increases, the total IMN impedance approaches the optimum impedance value, 17.3 Ω.

Therefore, the efficiency approaches the maximum efficiency when the parasitic capacitance is large as shown in Fig. 7. It is worth mentioning that when the switch is off, the tuning branch is supposed to be isolated from the IMN. Therefore, it is preferred for the MOSFET switch to have a small parasitic capacitance in order for the tuning branch to have little effect on the IMN when the switch in that branch is turned off.

In this case, the total network impedance without the Z_{CRx2} branch is 22.1Ω which is close to the impedance when parasitic capacitance is small as shown in Fig. 8. Therefore, in order to minimise the tuning branch effect when the switch is off, a small parasitic capacitance for the MOSFET is desirable.

However, in the experiment, it was infeasible to determine the value of C_p at the operating frequency of 200 kHz under various load conditions because it depends heavily on operating current which varies with total IMN impedance. Therefore, a small on-resistance is the main factor which determines the selection of MOSFETs.

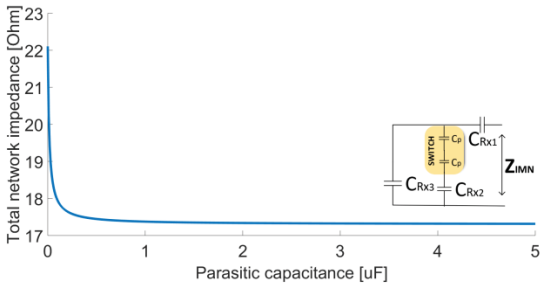

Fig. 8. Theoretical results – Total network impedance vs parasitic capacitance – model with switch off

3. AC Switch operation

To illustrate the operation of the relay and MOSFET switches, they have been implemented separately for both the on and off operation in the test circuit presented in Fig.9 and Fig.10. The test circuit illustrates a voltage divider with two resistors of equal value, R1 and R2. Firstly, when the switch is off, R2 is open-circuited therefore, V_{out} is equal to V_{in}. As illustrated in Fig.9, the relay and MOSFET operate equally as reliable compared to the case where R2 is physically removed. Secondly, when the switch is on, R2 is integrated in the branch through the switches or directly connected, with the test circuit acting like a voltage divider. Considering that the two resistors are of equal value, V_{out} is half of the V_{in} value. As shown in Fig. 10, V_{out} (either when the MOSFET or relay switch is on) is identical to the case when R2 is connected directly to R1 without any switch.. From both Fig.9 and Fig.10 it can be observed that the relay and MOSFET switches operate identically and equally as reliable to perform the switching for both on and off states.

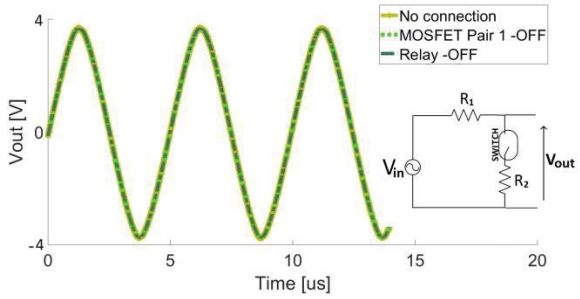

Fig. 9. Comparison of MOSFET and relay operation when turned off

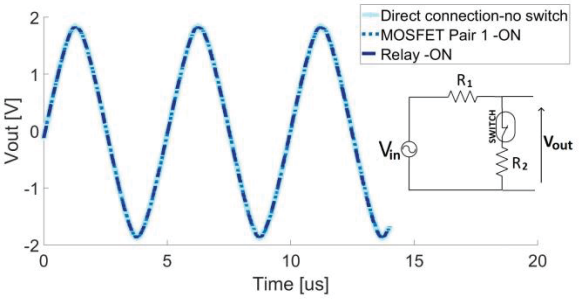

Fig.10. Comparison of MOSFET and relay operation when turned on

4. Experimental analysis of the switchable IMN

This section provides an overview on the experimental analysis of the proposed IMN. The WPT system consists of two main parts, the transmitter, T_x and receiver, R_x.The circuit diagram in Fig. 11 illustrates the system's structure.

At the transmitter, a PIC18F microcontroller is used to drive the H-bridge inverter (which is built using ZXMHC6A07T8 on a RE933-03ST adaptor) at 200 kHz. The inverter is then connected to the transmitting coil, T_x and tuning capacitor, C_{Tx}. A shunt resistor, R_{shunt}, was introduced in series with the transmitter coil for the measurement of the AC transmitting current. Further details are provided in Section 4.A. The main elements of the receiver consists of the receiving coil, R_x the IMN and receiver load, R_L. Fig. 12 shows the test setup. The transmitter and receiver coils are perfectly aligned and 5 mm apart. The two coils are identical, based on a triple-layer planar spiral model, where each layer has 8 windings.

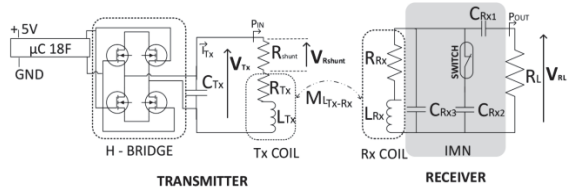

Fig. 11. WPT system -Transmitter, Tx with switchable IMN at the receiver, Rx

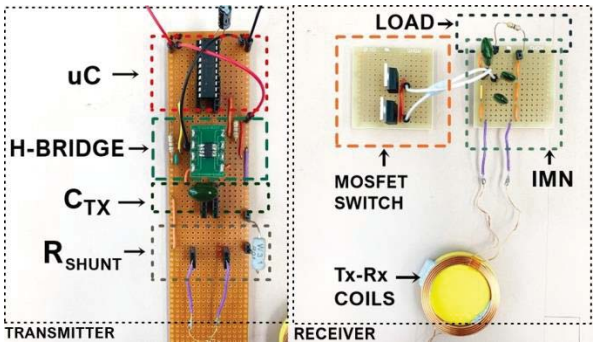

Fig. 12. WPT experimental setup – Transmitter, Tx and receiver, Rx circuits with the MOSFET switch at the IMN

TABLE II
WPT SYSTEM EXPERIMENTAL AND SIMULATED PARAMETERS
MOSFET SWITCHES

Pair No. and Name	Cp	Rp	Maximum Power
Pair I (CSD18533KCS)	2420 pF	5 mΩ	192 W
Pair II (IRF740BPBF)	520 pF	0.5 Ω	147 W
Pair III (IRFU310PBF)	170 pF	3.6 Ω	25 W
Pair IV (IRFBE20PBF)	530 pF	6.5 Ω	54 W

4.1. Test Setup

The power transfer efficiency was calculated using the efficiency formula in Eq. (23). The input power was calculated as the product between the T_x coil RMS voltage, V_{Tx} and the RMS current, I_{Tx}, which was measured using a 0.1 Ω shunt resistor in series with the T_x coil, R_{shunt}. The output power is calculated by measuring the RMS voltage across the variable load, V_{RL}.

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{\frac{V_{RL}{}^2}{R_L}}{V_{TX}\, I_{Tx}} \quad (23)$$

Under the same test conditions, the efficiency is calculated with various load resistances. The same method is used when the switch is connected on the IMN parallel branch.

All parameters listed in Table I have been tested experimentally for both T_x and R_x under a variable load condition.

The mutual inductance, M_{LTx-Rx} has been calculated by separating the coils from the WPT system without interfering with the alignment between them. A sinusoidal wave was applied at one of the coils and at the other, the received signal was analysed. By substituting the mutual inductance with its equivalent model in this type of configuration, at the frequency of 200 kHz, M_{LTx-Rx} has been determined to have the value of 14.4 µH with a coupling factor, k, of 0.48.

Following the findings presented in Section 2.C, four pairs of MOSFET switches with various on-resistances have been chosen for comparison. Considering that the parasitic resistance is a constant parameter compared to the parasitic capacitance which may vary depending on the operating frequency and current, R_p was the determining parameter which was taken into account initially. The parasitic capacitance, C_p was estimated in the experimental stage, as described in Section 2.B. The four pairs cover a wide range of values in terms of R_p starting from 5 mΩ up to 6.5Ω as presented in Table II.

4.2. WPT Transfer Efficiency

The WPT transfer efficiency was investigated for the IMN under all MOSFET pairs as well as a mechanical relay. Furthermore, the mathematical model presented in Section 2.C, was validated by simulating the WPT under the same parameters. All results are normalised to the maximum efficiency at the optimum load resistance when no switch is used. Fig. 13 compares the experimental results and the mathematical model presented in Section 2.C regarding the relationship between the normalised efficiency and load resistance, R_L. It was found that the analytical and experimental results agree. For higher load values, in the experiment, the impedance of the tuning capacitors changes depending on the current therefore justifying the discrepancy between the theoretical and experimental results. This observation applies to Fig. 14 and Fig. 15 as well. Overall, the system investigated delivers up to 1W of AC power.

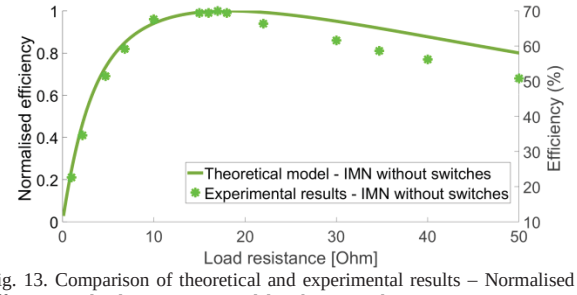

Fig. 13. Comparison of theoretical and experimental results – Normalised efficiency vs load resistance – model without switch

Secondly, the four pairs of MOSFET AC switches presented in Table II have been implemented to switch the tuning capacitor C_{Rx2} on one of the IMN parallel branches as shown in Fig. 13. Considering that the focus of this analysis is on the suitability of the MOSFET AC switches for the IMN networks and not on optimising the network itself or the circuit operation, the switches have been manually turned on and off as mentioned in Section 2.2.

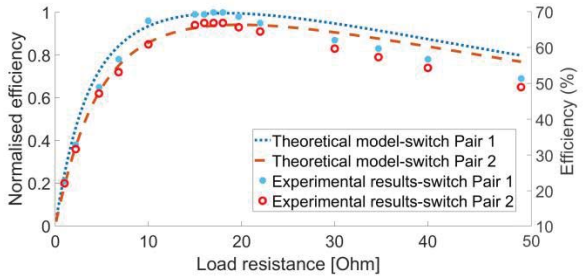

Fig. 14. Comparison of theoretical and experimental results – Normalised efficiency vs load resistance – model with Switch pair I and pair II

Comparing the results from Fig. 14 it can be observed that for the first two pairs of MOSFET switches, the experimental results agree with the mathematical model reasonably well. Between the first two pairs, the first one characterised by the smaller parasitic resistance, offers better performance as mentioned in Section 2. The mathematical model with the third and fourth pair of MOSFET switches agrees with the experimental results in Fig. 15.

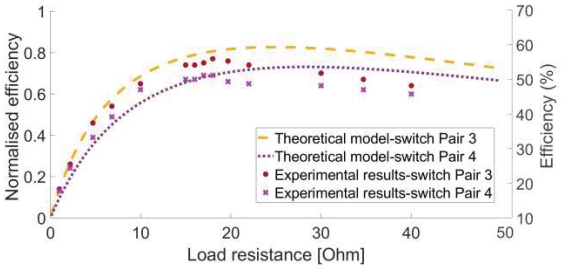

Fig. 15. Comparison of theoretical and experimental results – Normalised efficiency vs load resistance – model with Switch pair III and pair IV

Comparing the performance of the four switches, it can be noted that as R_p is increasing, it reduces WPT efficiency more and more.

Table III summarises the maximum peak of the normalised efficiency with its corresponding optimum load value. Whilst the normalised efficiency follows the same trend for both theoretical and experimental results, R_L is increasing in the theoretical simulation compared to the experiment. This is caused by the impedance change of the tuning capacitors due to the current variation.

TABLE III
WPT SYSTEM THEORETICAL AND EXPERIMENTAL MAX NORMALISED EFFICIENCY WITH THE MOSFET SWITCHES

Pair No.	Theoretical Max. Efficiency	Experimental Max. Efficiency	Theoretical Optimum R_L [Ω]	Experimental Optimum R_L [Ω]
Pair I	1.00	1.00	18.2	18
Pair II	0.96	0.95	19.5	18
Pair III	0.82	0.77	24.9	18
Pair IV	0.73	0.69	28.4	18

4.3. Comparison Between MOSFET and Relay

In this section, the IMN performance using MOSFET and relay switches is compared. Fig. 16 compares the experimental results of the normalised efficiency of the WPT using the MOSFET switch pair I, i.e. having the lowest on-resistance, compared to an electromechanical relay (OZ-SS-112LM1) used on the IMN's parallel branch. The results in Table IV outlines that the normalised efficiency of the MOSFET and relay when they are turned on is almost identical, considering that the relay used has a contact resistance of only 0.1 Ω. In the case of completely removing the C_{Rx2} tuning capacitor, the efficiency is reduced to a value

of 0.31 as shown in Table IV. Similar results are obtained when the relay is turned off. This is because the IMN is detuned and no longer has the optimum tuning capacitance.

When turning the MOSFET switch off, the normalised efficiency is 0.36 which is slightly higher than the case without the tuning capacitor C_{Rx2}. This result can be justified using the theoretical analysis from Fig. 8 by considering that when the MOSFET is turned off, R_p becomes so large that it can be treated as open-circuit. Therefore, the parasitic capacitance, C_p connects to the tuning capacitor C_{Rx2} in series. This causes a changes in the overall capacitance of that tuning branch and eventually the overall IMN tuning capacitance. In this particular case, the total IMN impedance with C_p connected to the C_{Rx2} and without the C_{Rx2} tuning branch are calculated as 21.5Ω and 22.1Ω respectively. As the former is slightly closer to the optimum total network impedance, i.e. 17.2Ω, the resulting efficiency is also slightly higher. The parasitic capacitance of the electromechanical relay is so small that it can be ignored. Therefore, the efficiency when the tuning branch is turned off by a relay is similar to the case when the branch is physically removed. Table IV compares the maximum efficiency in different cases as presented in Fig.16.

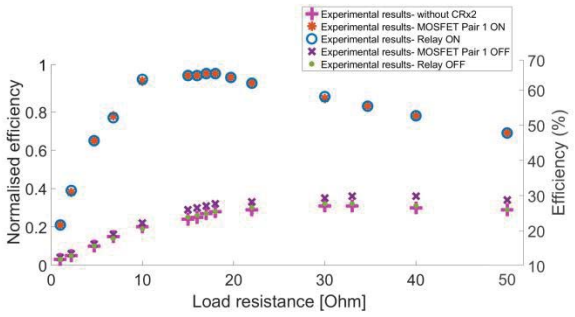

Fig. 16. Comparison of experimental results – Normalised efficiency vs load resistance – model with MOSFET pair I vs Relay (OZ-SS-112LM1)

TABLE IV
WPT SYSTEM EXPERIMENTAL MAX NORMALISED EFFICIENCY WITH MOSFET PAIR I AND RELAY (OZ-SS-112LM1)

IMN Configuration	Experimental Max. Efficiency	Experimental Optimum R_L [Ω]
Pair I – on	1.00	18
Relay - on	1.00	18
IMN without C_{Rx2}	0.31	33
Pair I – off	0.36	33
Relay – off	0.32	33

Compared to MOSFET switches, the relay switches have the disadvantage of being considerably more space-consuming. For example, each OZ-SS-112LM1 relay switch has the dimensions of 2.9 x 1.2 x 2 cm, i.e. a volume of 6.96 cm^3 (length/width/height) dimensions. Alternatively, the MOSFET offer the advantage of reducing the IMN size due to their small dimensions, for example each CSD18533KCS MOSFET has the dimensions of 0.9 x 0.4 x 1.6 cm, i.e. a volume of 0.576 cm^3. A pair of such MOSFETs have a total volume of 1.152 cm^3, which is only 16.5 % of the size of the relay switch. It is worth mentioning that the driving circuits for both switch types are identical. Therefore, the comparison of size only focuses on the switches themselves. In terms of price range, the OZ-SS-112LM1 relay is averagely priced compared to other relays, at a price point around £ 2.00 each. On the other hand, all MOSFET pairs are within a similar or lower price range compared to the relays.

5. DISCUSSION

The analysis from Section 4 concludes that under the given parameters and at a frequency of 200 kHz, the CSD18533KCS MOSFET switch performed the best due to its low on-resistance. Evaluating the results from the theoretical and experimental analysis presented above, it was found that the better efficiency is achieved when the switch is on and its on-resistance is low because the parasitic capacitor of the MOSFET switch is short-circuited and thus has little effect on the effective tuning capacitance of the IMN. As the on-resistance increases, the parasitic capacitor of the MOSFET switch becomes active and affects the total capacitance of the tuning branch it is connected to. As a consequence, the overall tuning capacitance of the IMN is drifted from the optimum tuning capacitance, thus the power transfer efficiency is reduced. Therefore, a smaller R_p is desirable.

When the tuning branch is turned off using a MOSFET switch, the efficiency is slightly higher than the case when the tuning branch is physically removed. This means that the MOSFET based switch still has an impact on the IMN even when it is turned off by introducing the parasitic capacitance to the tuning branch it is connected to. However, a parasitic capacitance that is significantly smaller than the tuning capacitance in that tuning branch can minimise such impact.

6. CONCLUSION

This paper investigates the feasibility of using MOSFET based AC switches in IMN for wireless power transfer. A mathematical model of inductive WPT system with such switches has been developed and verified for this research.

It is concluded that MOSFET AC switches are a viable option in place of relays in order to switch tuning capacitors in adaptive IMN. MOSFET switches with low on-resistance are preferred as they can short-circuit their own parasitic capacitor when they are turned on and, thus minimise the effect of the parasitic capacitance on the overall tuning capacitance.

When the MOSFET AC switch is turned off, its parasitic capacitance will change the overall capacitance of the branch it is connected to and, thus the overall capacitance of the entire IMN. It was found in the analysis that if the parasitic capacitance of the MOSFET switch is much smaller than the value of the tuning capacitor in that branch, its impact on the overall capacitance of that branch and thus the overall capacitance can be very little.

Therefore, it is recommended to use MOSFET's with low on-resistance and parasitic capacitances, for both on and off conditions, as AC switches in adaptive IMN for WPT. In addition, costs of MOSFET switches are similar to those of electromechanical relays but their physical sizes are much smaller. Hence, AC MOSFET switches are more suitable for applications where size constraints are required such as portable electronic devices.

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