

GeSbSeTe Phase-change Material for Write-once and Rewritable Flexible Non-volatile Memories

J. Pady¹, A. Nevill², J. Costa², F. Alkhalil², M. F. Craciun¹ and C. D. Wright¹

¹Department of Engineering, University of Exeter, EX4 4QF, UK

²Pragmatic Semiconductor, Cambridge, CB4 0WH, UK

jp551@exeter.ac.uk

ABSTRACT

The phase-change material $\text{Ge}_2\text{Sb}_2\text{Se}_4\text{Te}_1$ (GSST) is investigated for use in flexible non-volatile memory applications. Modified pore cell structures on polyimide substrates are fabricated using this material and their switching properties explored experimentally and via simulation. A straightforward route to the development of a write-once memory, involving a one-way switch from the amorphous to the crystalline phase, is first demonstrated. Subsequently, it is shown that GSST can support re-amorphisation in the modified pore cell structure, even with the relatively long duration pulses used in low-cost flexible systems, so demonstrating a fully rewritable flexible phase-change memory.

Key words: Flexible memory, electrical testing, selenium substituted GST.

1. INTRODUCTION

The phase-change material $\text{Ge}_2\text{Sb}_2\text{Se}_4\text{Te}_1$ (GSST) is a potential candidate for the realisation of non-volatile memory for low-cost and easy-to-fabricate flexible integrated circuits (FlexICs), with potential applications for flexible Internet-of-Things devices and wearable technologies. GSST displays an increased crystallisation temperature relative to the commonly used composition $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (GST) [1]. This is advantageous for use in the fabrication of a write-once memory where a single switch from amorphous to crystalline is used. Here, it is important that the device remains in the as-deposited amorphous phase during manufacture, therefore, an increased crystallisation temperature means a wider range of temperatures and techniques can be used during fabrication. Furthermore, GSST also displays a decreased crystal growth speed compared to GST; this should be advantageous for use in FlexIC systems, as such systems typically use relatively long pulse durations and fall times compared to conventional phase-change memory devices. This can make re-amorphisation problematic when using fast crystallisers such as GST. However, a material such as GSST, with its a decreased crystal growth speed, can suppress unwanted re-crystallisation during the RESET operation [2], thus facilitating the realisation of a fully rewritable flexible phase-change memory.

2. EXPERIMENTAL

Modified pore-cell structures were fabricated on flexible polyimide (PI) substrates. These substrates were mounted on glass, this prevents unwanted movement of the flexible polymer during fabrication. The cells were tested using both I-V sweeps and pulsed electrical measurements to explore device switching properties. The pulses used were in the μs range to closely reflect the length of pulses typically used in low-cost FlexIC systems. In addition, GSST device switching was investigated using simulations consisting of coupled finite-element electrothermal and phase-change modelling.

3. RESULTS & DISCUSSION

Fig. 1a shows an example I-V characteristic of a typical GSST device in the modified pore cell structure. The device remained in the as-deposited amorphous state throughout the (relatively high temperature) fabrication process, and I-V testing clearly reveals the expected threshold switching

from the amorphous to the crystalline state. Devices could also be switched from the post-fabricated amorphous state to the crystalline state using suitable pulses, so demonstrating suitability for use as a write-once memory. Following this, pulsed measurements were carried out to assess suitability for re-writable applications. To switch to the crystalline phase, 2 V SET pulses with durations typically around 14 μs were used. Following this, 3 V RESET pulses, again typically around 14 μs in duration, were used to re-amorphise the cell. Fig 1b shows the current and voltage response of the device during a 0.5 V, 10 μs READ pulse before and after this RESET pulse was applied. Here, it can be seen that before the pulse, a high current flows in the device indicating the crystalline phase, whereas after the RESET pulse, a low current is observed as the device has been switched back to the amorphous phase. The reversible switching of modified pore cell structures was also simulated: Fig 1c shows a 0.9 V, 10 μs pulse crystallising an initially fully amorphous cell. Fig 1d demonstrates the full rewritability of this cell. Here the starting distribution consists of a crystalline mark that was formed in an amorphous region melted into the cell. This crystalline region is successfully re-amorphised by a 2.5 V, 1.5 μs pulse.

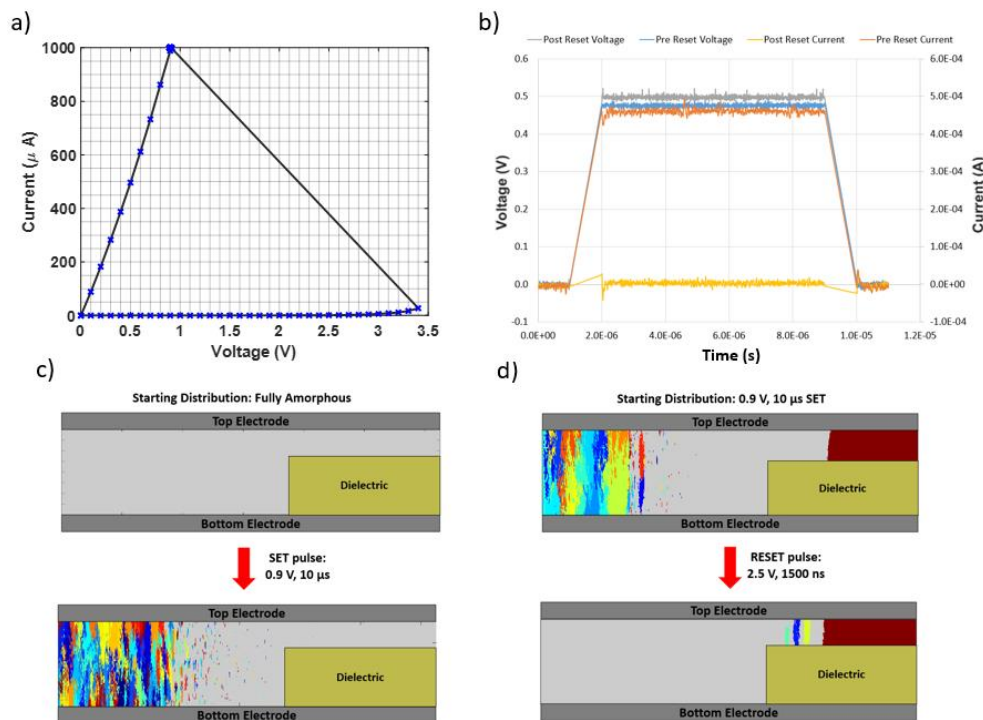


Fig 1. (a) I-V characteristic of the modified pore cell. (b) Voltage and current response when the modified pore cell is exposed to a 0.5 V, 10 μs READ pulse before and after the device is RESET by a 3 V, 14 μs pulse. (c) Simulation of a 0.9 V, 10 μs SET pulse triggering a switch from amorphous to crystalline. (d) Simulation of a 2.5 V, 1.5 μs RESET pulse switching a device in the crystalline state back to amorphous. Different colour regions represent different crystallite grain orientations.

4. CONCLUSIONS

The material GSST has an increased crystallisation temperature and decreased crystal growth speed compared to conventional GST, making it suitable for low-cost FlexIC applications. Modified pore memory cells with GSST were fabricated and simulated. Upon testing, the cells were demonstrated to be fully rewritable in both simulation and experiment.

REFERENCES

1. A. A. Burtsev et al, *Mater. Sci. Semicond. Process.* **150** (2022) 106907
2. J. Pady et al, *Phys. Status Solidi RRL*, (2024) 2300425